EE 434 Name _____
FINAL EXAM
Fall 2002

Instructions. You may bring up to 6 sheets of notes to this exam which is comprised of 6 problems and 8 questions. The weight for each question is 2 points and for each problem is 14 points. Please solve the problems and include your answers directly on the exam sheet.

Unless specified directly in a problem, if references to semiconductor processes are needed, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}$=100μA/v^2 ,$\mu_p C_{OX}$=30μA/v^2 ,V_{TNO}=0.5V, V_{TPO}= - 0.5V, C_{OX}=2fF/μ^2, λ = 0, γ = 0, Cbdbot = 0.5fF/μ^2 , and Cbdsw = 2.5fF/μ. and all npn bipolar transistors are characterized by the parameters β =100, V_{AF}=4, and J_S= 3E-19A/μ^2. If any other process parameters are needed, specify clearly what process parameter is needed and specify a typical value for that parameter.

Q1 What is the major reason a shift occurred in the mid 1980's from NMOS processes to CMOS processes?

Q2 What is the capacitance of a square of area 60μ^2 from Poly to Substrate if Poly is on top of field oxide in the process described on the last page of this exam.

Q3 If the drawn length of a transistor in a "1μ" process is 1μ, what would the effective be after the lateral diffusion takes place.

Q4 Why are contacts on top of gate oxide not permitted in many CMOS processes?

Q5 What is the major reason op amps are not realized by simply cascading 3 inverting CMOS amplifiers?

Q6 What is the major reason bipolar transistors are preferred over MOS transistors when building high-gain amplifiers?

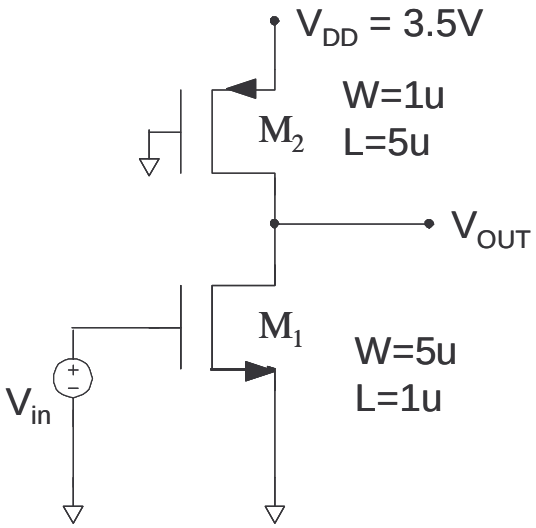
Q7 Give the circuit schematic of the basic MEM cell for an EEPROM. In this schematic, show where the row line and the column lines would be connected?

Q8 Several different methods of building logic were discussed. Sketch the circuit of the logic type that requires the fewest transistors to build a 3-input AND gate and tell what type of logic that is.

Problem 1 A pseudo-NMOS inverter is shown.

a) What is the static power dissipation when the output is low and when it is high?

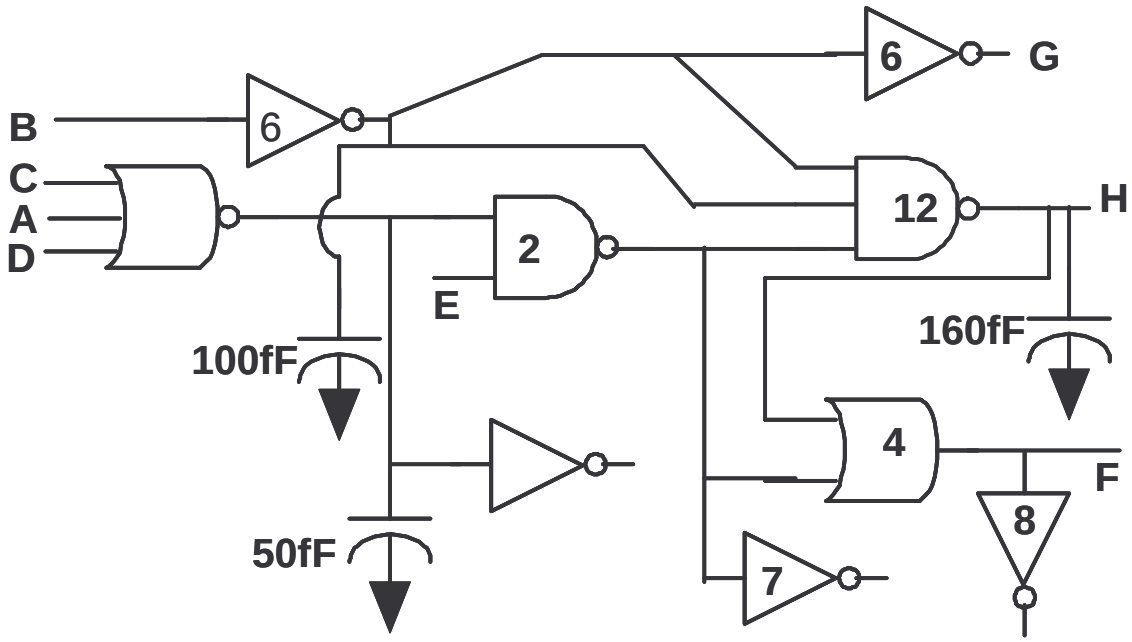
b) What is the dynamic power dissipation if the input is clocked at 15MHz and if it is driving 15 loads that are themselves identical pseudo-NMOS inverters?



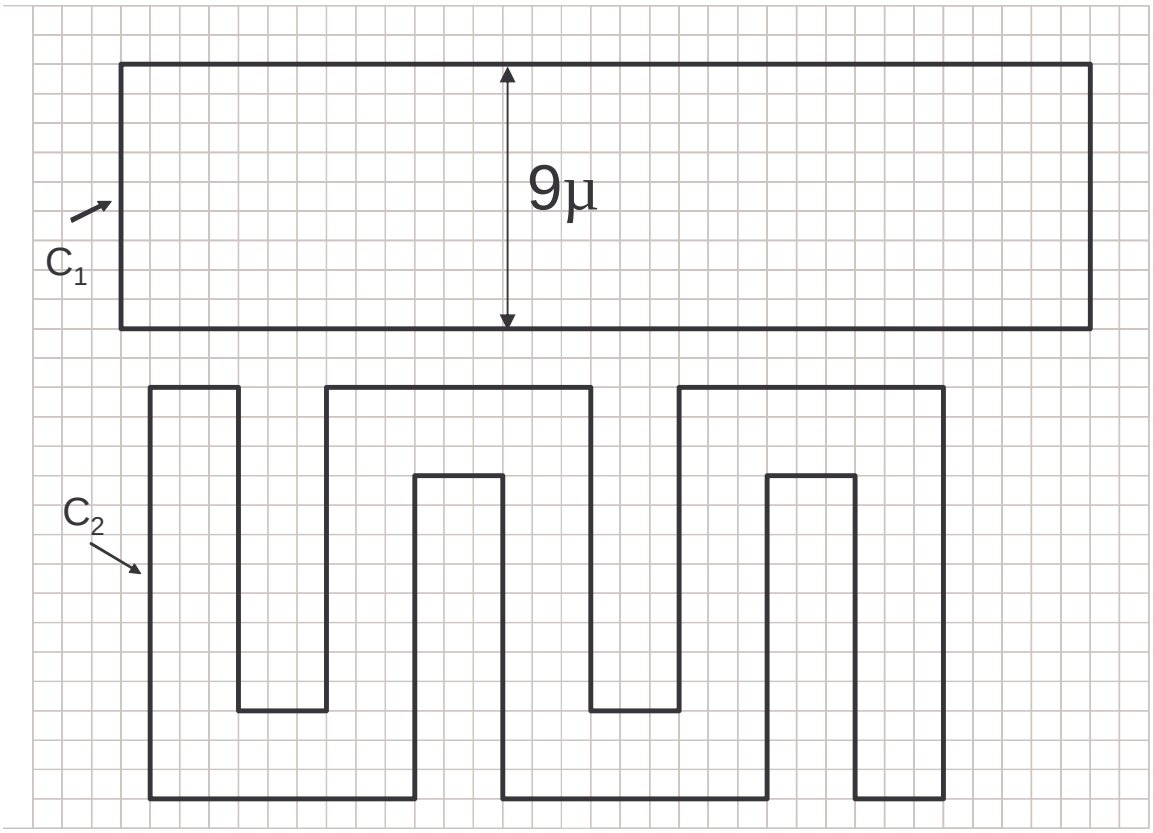
Problem 2 A logic circuit designed in conventional static CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times and that the input capacitance of an equal rise/equal fall reference inverter is 2fF and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay (T_{HL} + T_{LH}) from the C input to the F output

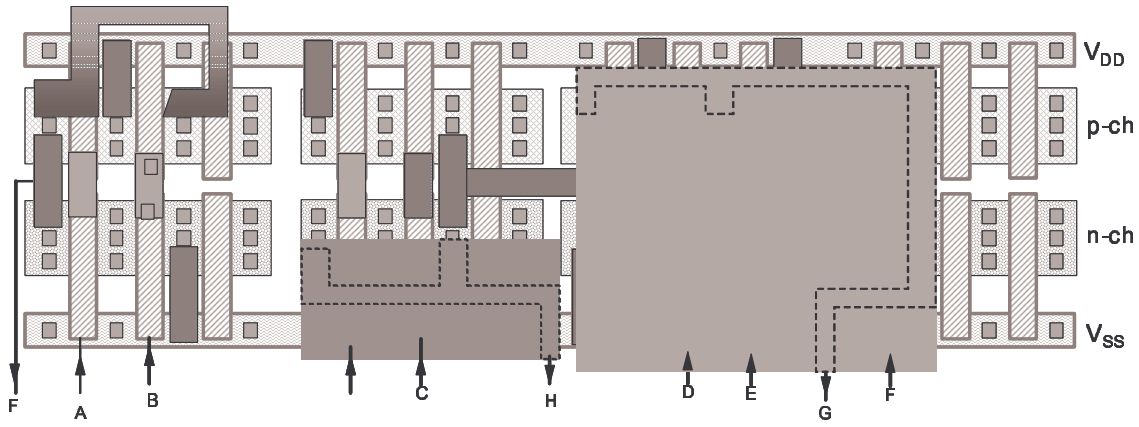
b) Repeat part a) if all gates are minimum sized.



Problem 3 Two diffusion capacitors are shown. Assume the capacitances C_1 and C_2 were measured to be 1.125pF and 970fF respectively. Determine the sidewall density, $C_{SW,}$ and the bottom density, C_{BOT}, for the process.

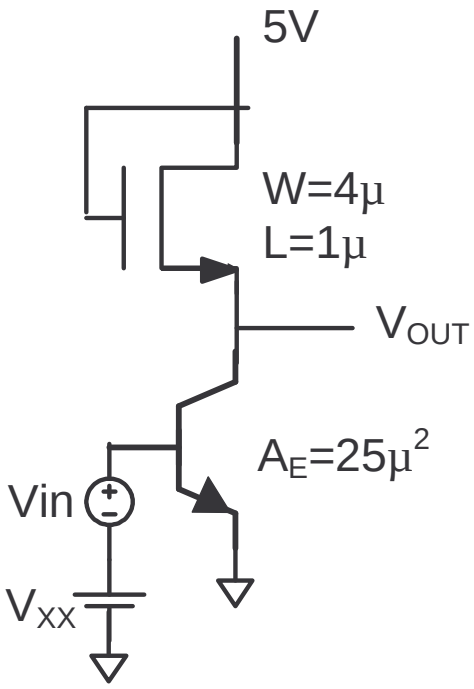


Problem 4 A type of gate array is shown. Determine the Boolean function that is programmed into this array, give the circuit schematic and give all devices sizes. Assume the minimum width of poly in this process is 0.6µ .



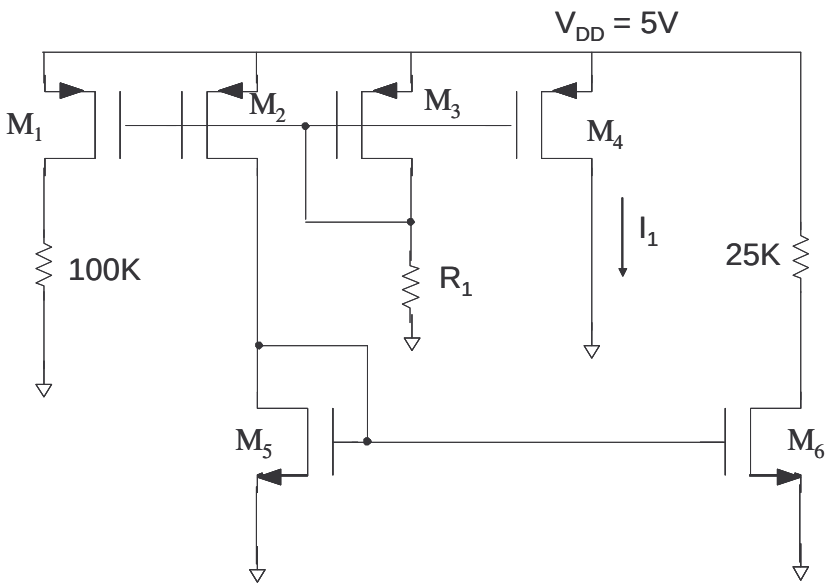
Problem 5 Assume the bias voltage V_{XX} is adjusted so that the quiescent output voltage is 3.5V.

a) Determine the quiescent drain current
b) Determine a numerical value for the small signal voltage gain.



Problem 6 Assume the voltage Drop across the 100K resistor was measured to be 2V.
a) Determine the value of R_1 needed to establish this voltage.
b) What is the current I1?
c) What is the voltage across the 25K resistor?

Assume the device sizes, in µ, are:
$W_1=W_2=40, L_1=L_2=15$
$W_3=16$, $L_3=1, W_4=20, L_4=15$
$W_5=8, L_5=4, W_6=16, L_6=4$



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um