EE 434 Name _____
FINAL EXAM
Fall 2003

Instructions. You may bring up to 6 sheets of notes to this exam which is comprised of 6 problems and 8 questions. The weight for each question is 2 points and for each problem is 14 points. Please solve the problems and include your answers directly on the exam sheet.

Unless specified directly in a problem, if references to semiconductor processes are needed, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=30\mu A/v^2$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, $\gamma = 0$, Cbdbot = $0.5fF/\mu^2$, and Cbdsw = $2.5fF/\mu$. and all npn bipolar transistors are characterized by the parameters $\beta =100$, $V_{AF}=4$, and $J_S= 3E\text{-}19A/\mu^2$. If more detailed process parameters are needed, refer to the list of parameters on the last page of this exam. If any other process parameters are needed, specify clearly what process parameter is needed and specify a typical value for that parameter.

Q1 What is the major purpose of the field oxide in a CMOS process?

Q2 How does the mobility of a p-channel transistor compare to that of an n-channel transistor?

Q3 What two regions of operation do most transistors operate in when used to build logic circuits?

Q4 In the AMI 0.5u CMOS process discussed in class, what is the difference between transistors used to build logic circuits and transistors used to build linear circuits?

Q5 What is the major reason the gain of a bipolar amplifier is typically larger than that of a MOS amplifier if the same amplifier structures are used?

Q6 If is often stated that the analog designer would prefer the bipolar process over the CMOS process yet many analog designs are done in the CMOS process. What is the major reason the technology of choice of the analog designer is not used to do analog designs?

Q7 What is the two major advantages of dynamic logic over static CMOS logic in the applications where it is generally used?

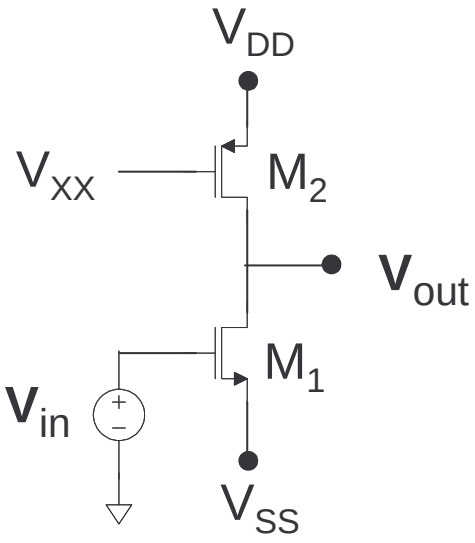
Q8 Dynamic power dissipation was the major source of power dissipation in high speed CMOS circuits with minimum gate lengths at the 0.35µ range and above. As processes move to minimum gate lengths of 0.12µ and below, two other sources of power dissipation are becoming dominant. What are they?

Problem 1 Two amplifier circuits are shown.

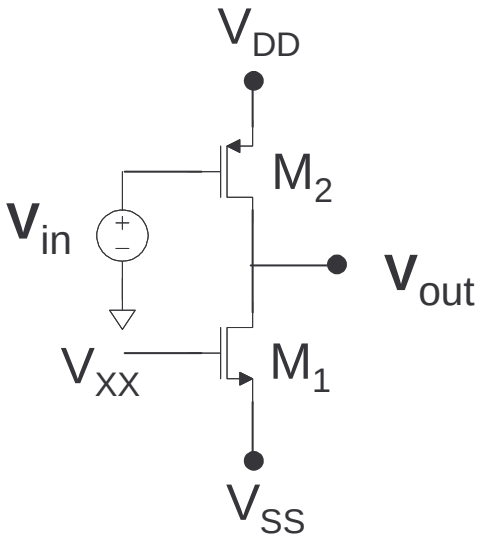
a) Determine the voltage gain for each in terms of the small signal parameters

b) Compare the small signal voltage gains of the two circuits if both are biased at the same quiescent current level.

Assume the widths and lengths of all transistors are the same, that all transistors are biased to operate in the saturation region, and that the process is the same as described on the first page of this exam except that $\lambda_n = \lambda_p = .01V^{-1}$



(a)



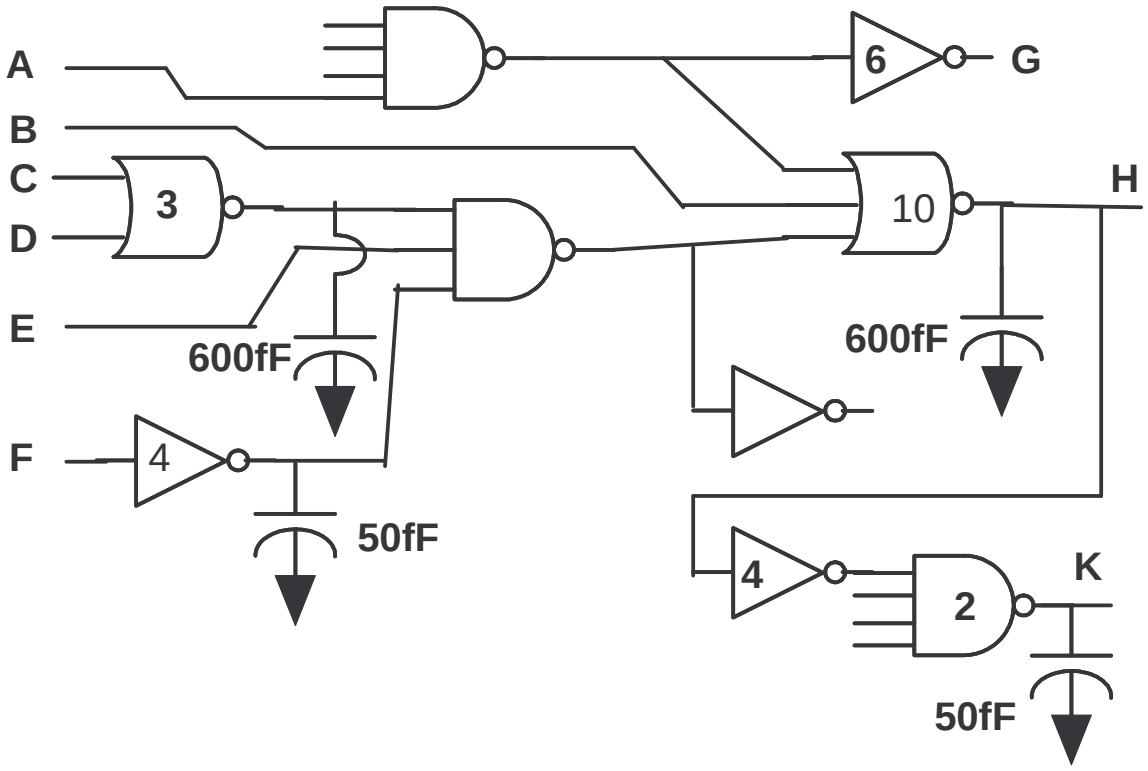
(b)

Problem 2 A digital circuit fabricated in a 0.5µ CMOS process has a total die area of $4mm^2$. If the defect density is $4/cm^2$, determine the approximate cost per good die if the die are fabricated on 8 inch wafers and if the wafer costs are $1600 each.

Problem 3 A logic circuit designed in conventional static CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times and that the input capacitance of an equal rise/equal fall reference inverter is 2fF and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay (T_{HL} + T_{LH}) from the C input to the H output

b) Repeat part a) if all gates use all minimum sized transistors.

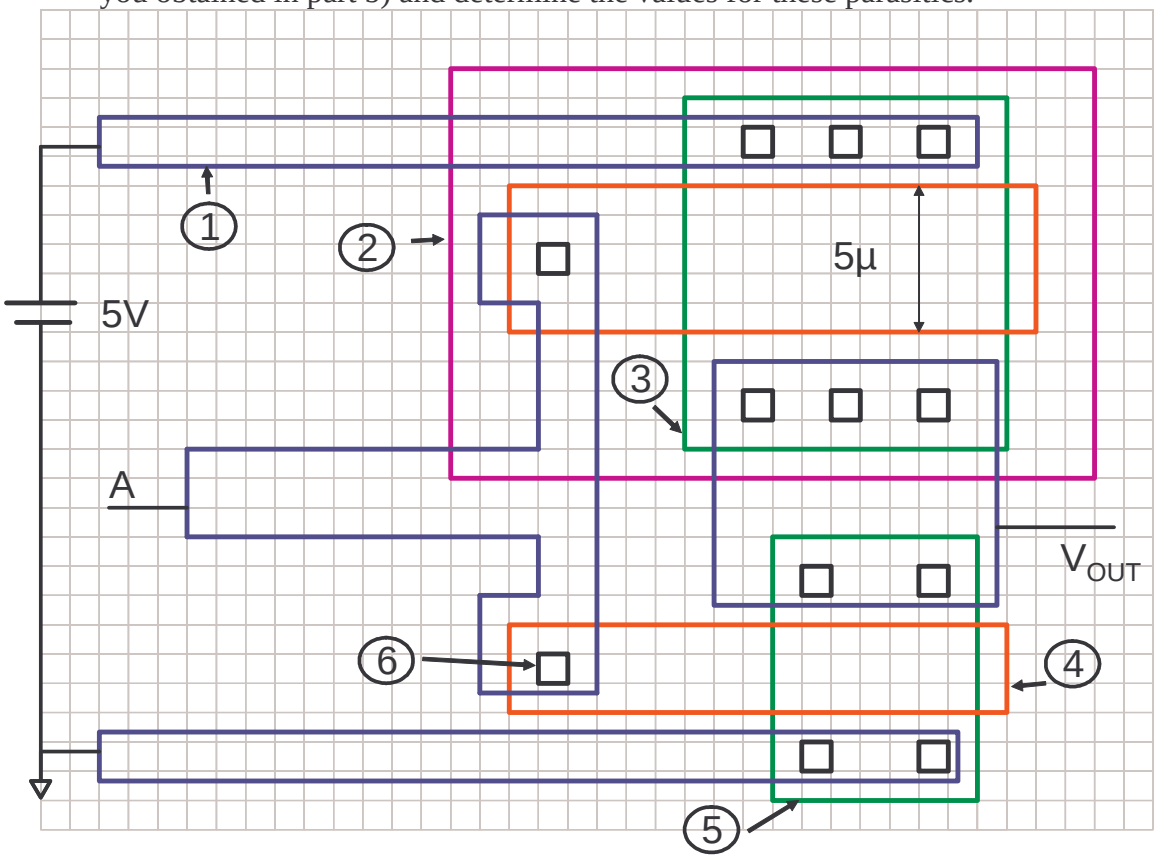


Problem 4 The layout of an inverter in a standard CMOS process is shown.

a) Identify the regions indicated by the six circled numbers

b) Give a schematic for the circuit including all device sizes

c) Identify all relevant parasitics in this layout by showing them on the schematic you obtained in part b) and determine the values for these parasitics.

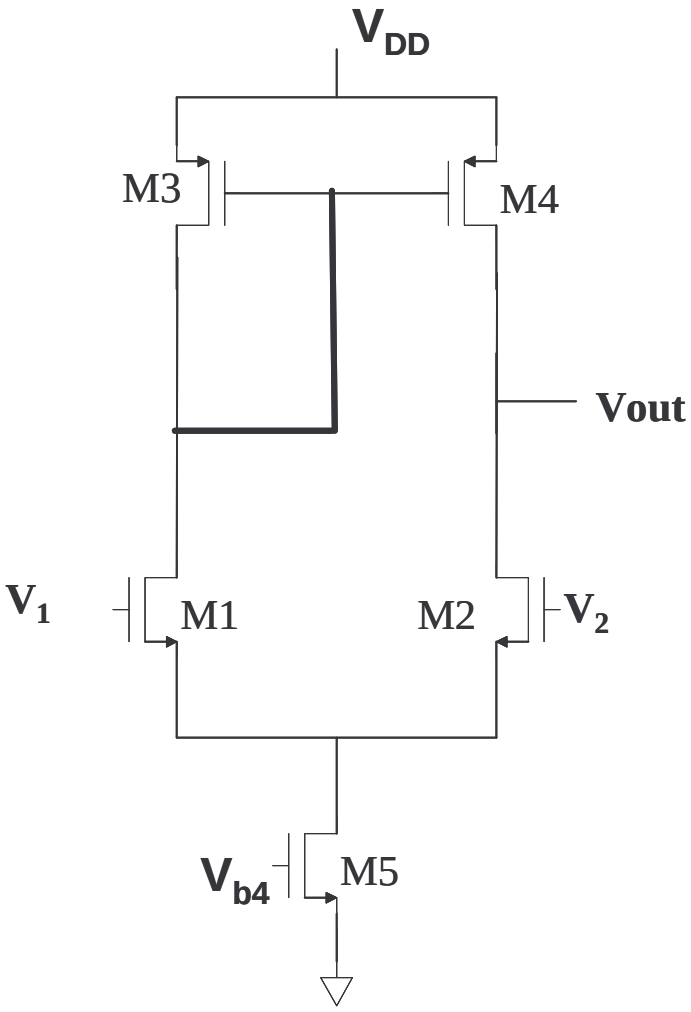


Problem 5 Design a circuit in the 0.5u AMI CMOS process that implements the following Boolean function $F = AB + \overline{A}\,\overline{B}C$ in

a) Static CMOS Logic and
b) Pass Transistor Logic

In your design, size all devices so that there are equal worst case rise and fall time for the static CMOS implementation and use minimium sizing in the PTL implementation. Assume the input variables present are A,B and C.

Probhlem 6 Determine the voltage gain $A_V = \frac{V_{out}}{V_d}$ where $V_d = V_2 - V_1$ for the amplifier shown. Assume the current in M5 is 50uA and that all transistors have W=5µ and L=1µ.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um