EE 434 Name ____________________________
FINAL EXAM
Fall 2004

Instructions. You may bring up to 6 sheets of notes to this exam which is comprised of 8 problems and 10 questions. The weight for each question is 2 points and for each problem is 10 points. Please solve the problems and include your answers directly on the exam sheet.

Unless specified directly in a problem, if references to semiconductor processes are needed, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}$=100µA/v^2 ,$\mu_p C_{OX}$=30µA/v^2 ,V_{TNO}=0.5V, V_{TPO}= - 0.5V, C_{OX}=2fF/µ^2, $\lambda = 0$, $\gamma = 0$, Cbdbot = 0.5fF/µ^2 , and Cbdsw = 2.5fF/µ. and all npn bipolar transistors are characterized by the parameters β =100, V_{AF}=4, and J_S= 3E-19A/µ^2. If more detailed process parameters are needed, refer to the list of parameters on the last page of this exam. If any other process parameters are needed, specify clearly what process parameter is needed and specify a typical value for that parameter.

Q1 What is the major purpose of the field oxide in a CMOS process?

Q2 How does the mobility of a p-channel transistor compare to that of an n-channel transistor?

Q3 What two regions of operation do most transistors operate in when used to build logic circuits?

Q4 In the AMI 0.5u CMOS process discussed in class, what is the difference between transistors used to build logic circuits and transistors used to build linear circuits?

Q5 How does the dynamic power dissipation of logic gates designed using minimum sized transistors in static CMOS implementations compare to that dissipated when the devices are sized for equal worst case rise and fall times?

Q6 If is often stated that the analog designer would prefer the bipolar process over the CMOS process yet many analog designs are done in the CMOS process. What is the major reason the technology of choice of the analog designer is not used to do analog designs?

Q7 What is the two major advantages of dynamic logic over static CMOS logic in the applications where it is generally used?

Q8 Dynamic power dissipation was the major source of power dissipation in high speed CMOS circuits with minimum gate lengths at the 0.35µ range and above. As processes move to minimum gate lengths of 0.12µ and below, two other sources of power dissipation are becoming dominant. What are they?

Q9 How do the minimum feature sizes that can be patterned in a state of the art bipolar process compare to those that can be patterned in a CMOS process?

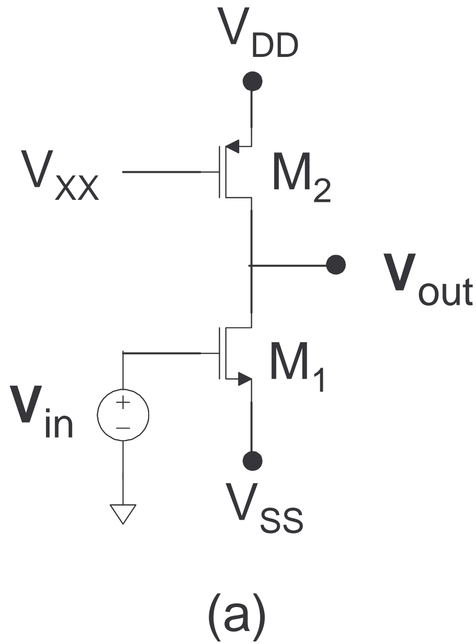
Q10 The propagation delay of minimum-sized gates driving comparable devices is in the 10 to 20 ps range which means they can be clocked at 50GHz to 100GHz rates yet the system clock on high-end microcontrollers and mircoprocessors is in the 3GHz range. Why is there such a big discrepancy?

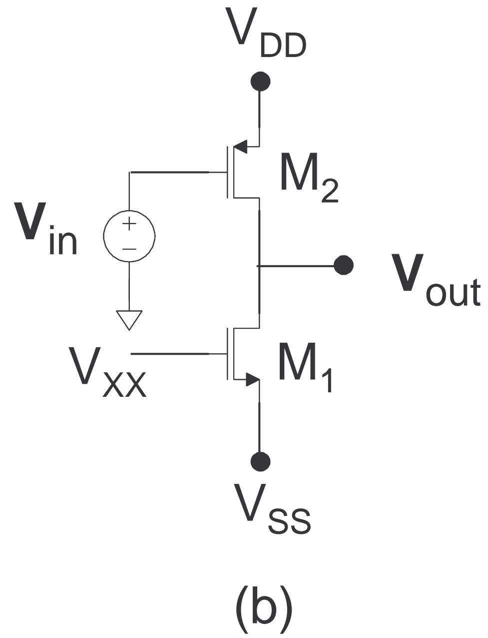
Problem 1 Two amplifier circuits are shown.

a) Determine the voltage gain for each in terms of the small signal parameters

b) Compare the small signal voltage gains of the two circuits if both are biased at the same quiescent current level.

Assume the widths and lengths of all transistors are the same, that all transistors are biased to operate in the saturation region, and that the process is the same as described on the first page of this exam except that $\lambda_n = \lambda_p = .01V^{-1}$



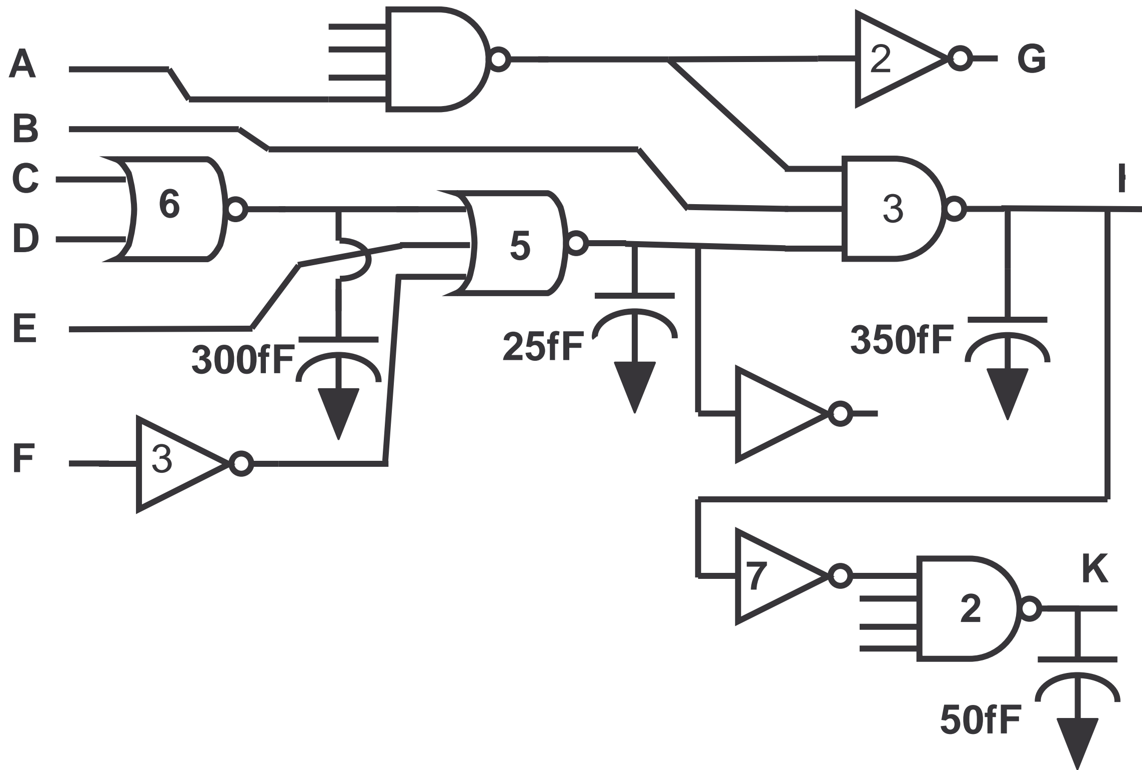


Problem 2 Assume the designer has to make a choice about whether to implement a particular function on one die or on two smaller equal-sized die. Assume the area overhead for the I/O on a chip is A_1 and the total active area for implementing the required functionality is A. (Thus, if two chips are used, each will contain an area A_1 for the I/O whereas if a single die is used, the total area for I/O will still be A_1) . Quantitatively compare the cost of producing a functional single-chip solution with that of the two-chip solution. Assume the defect density is $1/cm^2$, the die come from 8inch wafers that have a fabrication cost of $1200, the area A_1 is $0.1cm^2$ and the area A is $.25cm^2$. Neglect packaging and testing costs.

Problem 3 A logic circuit designed in conventional static CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times and that the input capacitance of an equal rise/equal fall reference inverter is 2fF and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay (T_{HL} + T_{LH}) from the E input to the K output

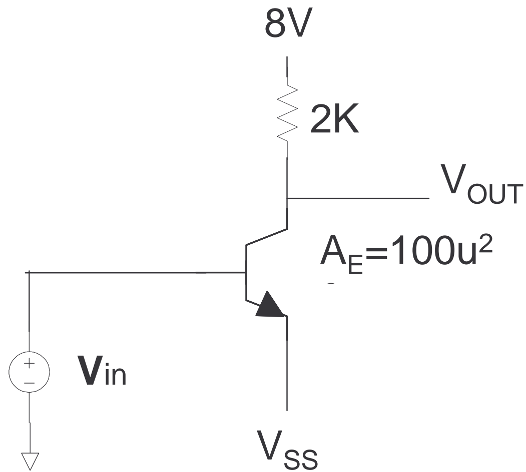
b) Repeat part a) if all gates use all minimum sized transistors.



Problem 4 Assume that the voltage V_{SS} was selected so that the quiescent output voltage of the amplifier shown was measured to be 5V.

a) Develop a small signal model for the BJT assuming it is operating in the forward active region. Use the forward active region model for the BJT introduced in the class.

b) Determine the small-signal voltage gain of the circuit from the input to the output.

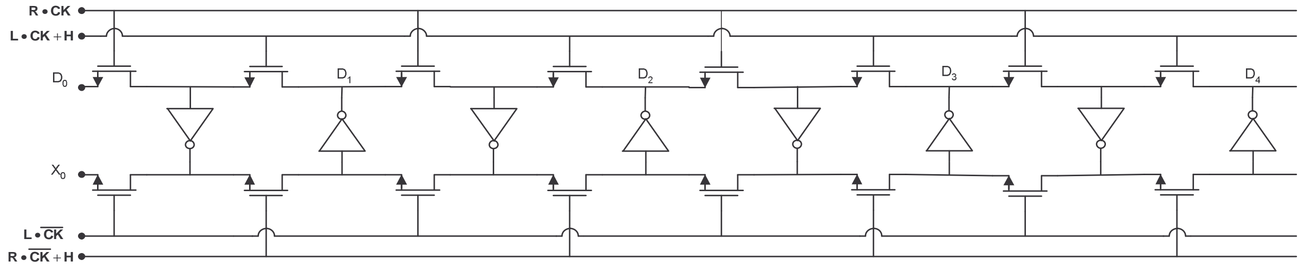


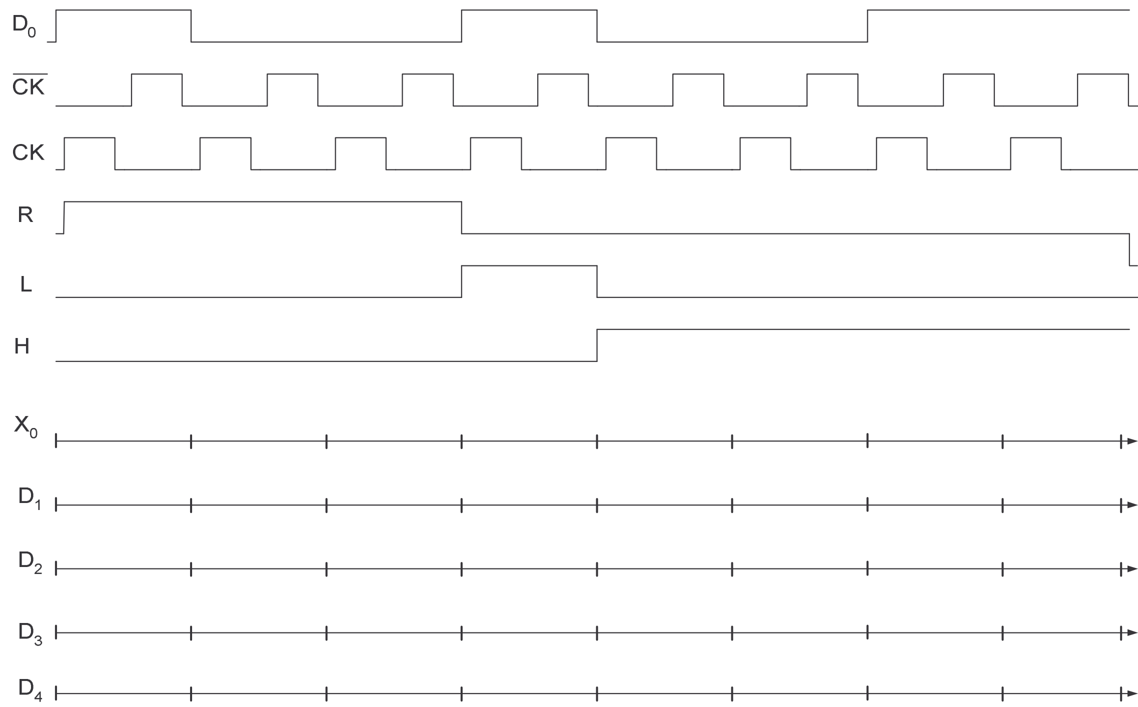
Problem 5 Design a circuit in the 0.5u AMI CMOS process that implements the following Boolean function $F = \overline{A}B + A\overline{B}C$ in

a) Static CMOS Logic and
b) Pass Transistor Logic
c) Domino Logic

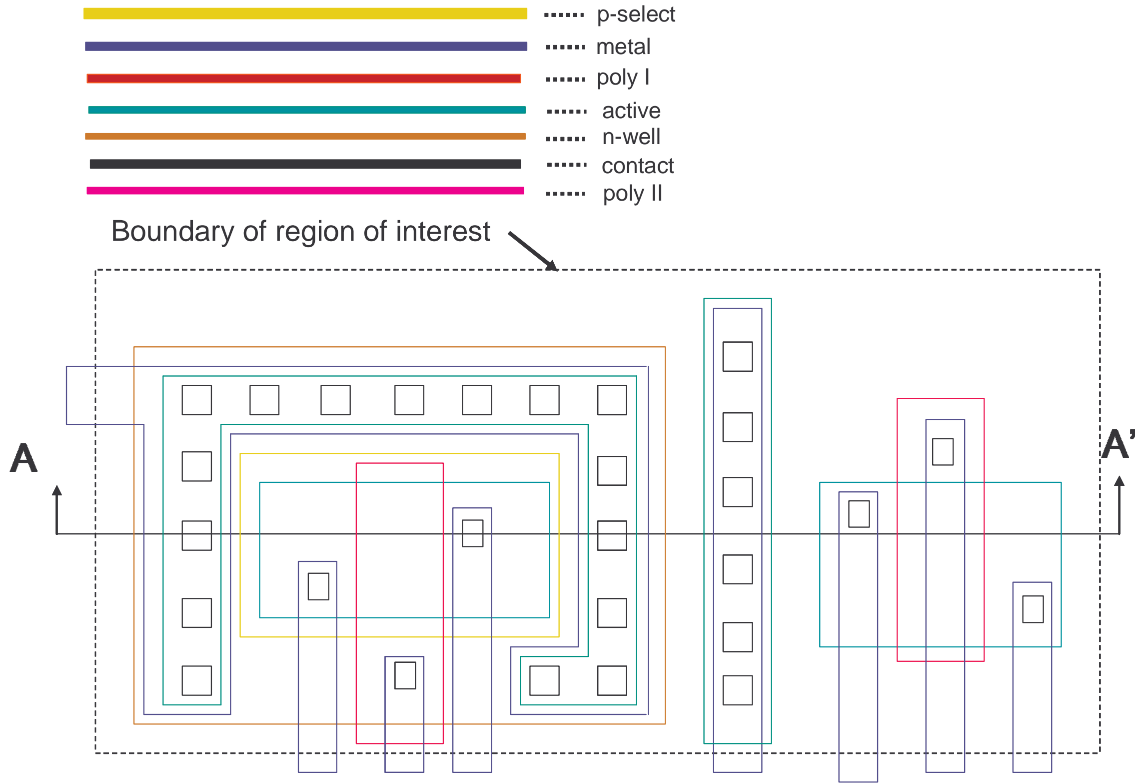
In your design, size all devices so that there are equal worst case rise and fall time for the static CMOS implementation and use minimum sizing in the PTL and Domino Logic implementations. Assume the input variables present are A,B and C.

Probhlem 6 A circuit that is fabricated in a bulk CMOS process is shown. If the control signals are as given in the following timing diagram, provide a timing diagram for the signals X_0, D_1,D_2, D_3 and D_4. Indicate, as appropriate, on the timing diagram where the signals are not defined.

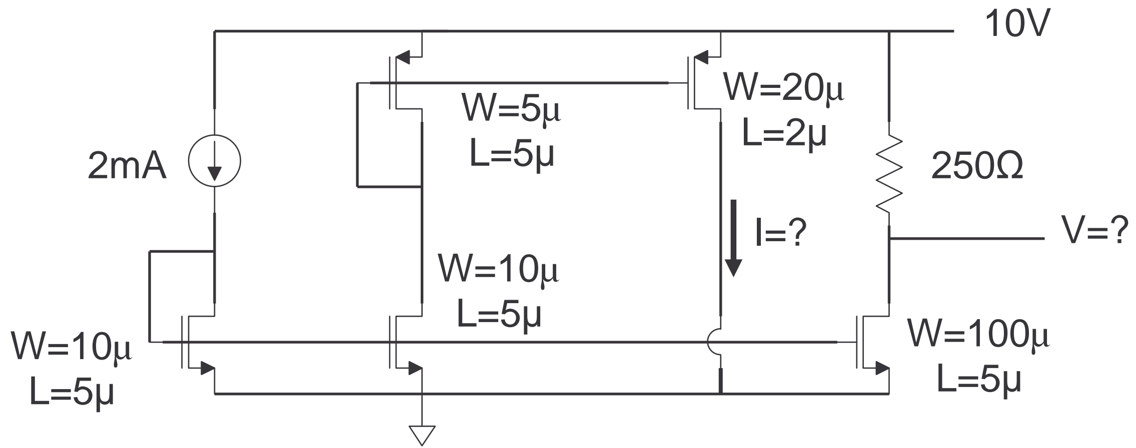




Problem 7 The top view of a section of a layout in a Bulk CMOS process is shown. Sketch a vertical cross-section view of this section along the A-A' section line.



Problem 8 Determine the current I and the voltage V for the circuit shown.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um