Instructions: This is an open-book, open-notes exam but no collaboration with anyone except the course instructor is permitted. This exam is to be returned to Rm 2133 Coover by 5:00 p.m. on Friday May 7. There are 8 problems on this exam and all are equally weighted. Note that Problems 2 and 3 are joined together. On those problems that need technology parameters, assume you are working in a 0.5μ CMOS process with 

$$\mu_{n}C_{ox} = 100\mu A/\sqrt{2}, \mu_{p}C_{ox} = 30\mu A/\sqrt{2}, V_{TNO} = 0.8V, V_{TPO} = -0.8V, C_{ox} = 2fF/\mu^2, \lambda = 0.01v^{-1}, \gamma = 0, C_{dbot} = 0.5fF/\mu^2, \text{ and } C_{ds} = 2.5fF/\mu.$$

Problem 1 In the following amplifier, assume $V_{DD}$ is 5V, $C_{L}=5pF$.

a) Determine the power required to achieve a GB of 10MHz if $V_{EB}$ on all devices is 500mV.

b) What is the voltage gain of this op amp?

c) What is the slew rate?

d) What is the common-mode input range of this op amp?

e) What is the output signal swing of this op amp?
Problem 2 and 3  Three comparator circuits are shown. They all use the same basic architecture but the load on the first circuit is cross-coupled and the latter two are not. The first two are clocked and a comparison is to be made when the clock signal $\phi$ goes high. Assume all are designed so that all transistors are the same size and operating in the saturation region when in the “ARM” state.

a)  Compare the settling time of the three structures as a function of the differential input voltage. Is one faster than the other for small differential inputs? For large differential inputs?

b)  Compare the power dissipation for the three structures as a function of the differential inputs for making a single comparison.
Problem 4  Assume \( V_{DD} = 5\text{V} \) and \( V_{b3} \) in the following circuit was adjusted so that \( V_{OUTQ} = 2.5\text{V} \).

a) Determine the dc gain \( (A_v = V_o/V_i) \) and the two poles of this amplifier in terms of the small signal parameters of the transistors. Assume all parasitic capacitances on each node are included in the values of \( C_1 \) and \( C_2 \).

b) If \( C_1 \) and \( C_2 \) represent only the parasitic capacitances in the circuit and the devices are all of approximately the same size with large gate areas, which one of the poles is dominant and why?
Problem 5 Two layouts of a pair of POLY resistors are shown in the x-y plane where the blue segments are connected in parallel to form resistor $R_1$ and the purple regions are connected in parallel to form resistor $R_2$. The units for the x and y axis are in microns. All 4 segments are made of POLY 1 and the different colors are used to distinguish the components of $R_1$ from those of $R_2$. Assume the sheet resistance in both layouts at the origin (0,0) is $50\Omega/\square$.

\begin{itemize}
  \item[a)] Determine the nominal value for the resistors $R_1$ and $R_2$ if there are no gradient effects present and if there are no local random variations in the sheet resistance.
  \item[b)] Determine the relative error (in %) between the two resistors if there is a gradient of $0.1\Omega/\square \mu$ in the +x direction. Neglect all local random variations.
  \item[c)] Repeat part b) if the gradient is at 45° in the x-y plane. Neglect all local random variations.
\end{itemize}
Problem 6

The circuit shown has been proposed as a temperature sensor.

a) Assuming a square-law model for the devices and neglecting $\gamma$ and $\lambda$ effects, derive an expression for the output voltage $V_{\text{OUT}}$.

b) If the threshold voltages of the n-channel and p-channel devices are modeled by the expressions

$$V_{TN} = V^{TN}_{NO} + n$$
$$V_{TP} = V^{TP}_{PO} + p$$

Analytically obtain the relationship between $V_{\text{OUT}}$ and $T$.

c) Based upon the results obtained in part b), comment on how useful this circuit might be as a temperature sensor.

d) Implement this temperature sensor in the ON 0.5u process and compare simulated results with those obtained in part b). Give the device sizes you used in this implementation. (Note: This circuit requires a start-up circuit to guarantee it starts up correctly. You do not need to include the start-up circuit but if not included, you may need to set initial conditions appropriately or use some other method to be sure the simulation provides the desired operating point).
Problem 7   Two switched-capacitor amplifiers are shown. Determine the output voltage and the voltage gain from $V_{IN1}$ for each. In these circuits, $C_1=200\, \text{fF}$, $C_2=50\, \text{fF}$ and $C_3=100\, \text{fF}$. Assume complimentary no overlapping clocks as shown.
Problem 8
a) Derive an expression for the output voltage of the DAC shown as a function of the Boolean inputs \( S_0, S_1, S_2 \) and \( S_3 \).

b) Determine the time it takes the output to settle to within \( \frac{1}{2} \) LSB of the final output for a code transition from 0111 to 1000 if the op amp can be modeled as a single-pole amplifier with a dc gain of 80dB and a GB of 20MHz. Assume the current sources and switches are ideal.

b) If the current source above \( S_0 \) is 10% below the nominal value and all other current sources are equal to their nominal values, determine the INL of this DAC.