Lecture 23

Data Converters
Data Converters:
ADC (analog to digital)
DAC (digital to analog)

Note: Many ADC architectures use a DAC in a feedback path

\[ \overrightarrow{x_0} \rightarrow \text{DAC} \rightarrow \text{D/A} \rightarrow x_0 \]

\[ X_{REF} \]

\[ \overrightarrow{x_0} = (b_{n-1}, b_{n-2}, \ldots, b_0) \]

- \( b_{n-1} \) is the MSB
- \( b_0 \) is the LSB
Ideally

\[
\frac{X_{\text{REF}}}{2^n}
\]

The range is \( \frac{X_{\text{REF}}}{2^n} \) less than \( X_{\text{REF}} \)

\[
X_0 \text{ ideal} = X_{\text{REF}} \sum_{i=1}^{n} \frac{b_{n-i}}{2^i}
\]

Output for each

000 is 0

... Could have \( X_0 \) for 000 or 0

\[
\ln(2n) \text{ arg}
\]
Note: The static performance of a D/A is completely characterized by the sequence

\[ < x_0(0), x_0(1), \ldots, x_0(2^n-1) > \]
DAC applications

1) Waveform Generation.

Diagram:

- Clock input
- n-bit binary counter
- D/A converter
- Output signal

Graph:

- Time intervals: $T$, $2T$, $3T$
- Output signals:
  - $11001010110$
  - $11001011010$
  - $11001011010$

Equation:

$$T_x = 2^n T$$

To generate a sine wave, the ROM (RAM) would have 
\[ \frac{\sin x + \frac{1}{2}}{2} \]
stored at address location "x".
2) Voltage Generation
3) Analog Trim
4) Control Systems
5) As a fb. element in ADC

Note: A nonlinear DAC can be built directly if needed.
ADC:

\[ x_n \xrightarrow{\text{R/D}} x_o \]
\[ x_o = \langle d_1, d_2, \ldots, d_n \rangle \]

Ideally:
\[
x_{\text{in}} = x_{\text{REF}} \left( \frac{d_1}{2} + \frac{d_2}{4} + \cdots + \frac{d_n}{2^n} \right)
\]
\[ = x_{\text{REF}} \sum_{k=1}^{n} \frac{d_k}{2^k} \]

Actually:
\[
x_{\text{in}} = x_{\text{REF}} \sum_{k=1}^{n} \frac{d_k}{2^k} + \epsilon
\]

If \( n \) is large enough, \( \epsilon \) can be made arbitrarily small.

d_1: MSB
d_n: LSB
Quiz

Assume an Ideal 4-bit DAC with a reference voltage of 5V has a Boolean input of <1 0 1 0>. What is the output?
And the number is ....

6 8 7 5 3
6 9 4 2
Quiz solution

\[ V_{\text{OUT}} \langle b_{n-1}, b_{n-2}, \ldots b_0 \rangle = V_{\text{REF}} \sum_{i=1}^{n} \frac{b_{n-i}}{2^i} \]

\[ V_{\text{OUT}} \langle 1 \ 0 \ 1 \ 0 \rangle = 5 \left( \frac{1}{2} + \frac{0}{4} + \frac{1}{8} + \frac{0}{16} \right) = \frac{25}{8} = 3.125 \]
Review from Last Time

• An Ideal DAC provides analog outputs that are linearly dependent upon the Boolean input and the reference input
• An Ideal ADC provided digital outputs that are proportional to the analog input but quantized to the resolution of the ADC
• Simple DAC structures can be readily obtained but the performance is ultimately in how detailed issues are handled
ADC:

![Diagram of ADC block diagram with inputs and outputs labeled.]

\[ X_0 = \langle d_1, d_2, \ldots, d_n \rangle \]

Ideally:

\[ X_{in} = X_{REF} \left( \frac{d_1}{2} + \frac{d_2}{4} + \cdots + \frac{d_n}{2^n} \right) \]

\[ = X_{REF} \sum_{k=1}^{n} \frac{d_k}{2^k} \]

Actually:

\[ X_{in} = X_{REF} \sum_{k=1}^{n} \frac{d_k}{2^k} + \epsilon \]

If \( n \) is large enough, \( \epsilon \) can be made arbitrarily small.

\( d_i \): MSB

\( d_n \): LSB
\[ e(\bar{x}_i) = \bar{x}_0 - x_i \]

\[ x_{LB} = \frac{X_{REF}}{2^n} \]
Data Converters

Characterization of ADC's & DACs

Static Characteristics
- LSB
- Resolution
- Offset & Gain Errors
- Absolute Accuracy
- Relative Accuracy
- Integral Nonlinearity
- Differential Nonlinearity
- Monotonicity (D/A)
- Missing Codes (A/D)

Dynamic Characteristics
- Conversion & Settling Time (A/D)
- Settling Time at Clock Rate (D/A)
- Sampling Time Uncertainty
- Dynamic Range
- Signal/Noise Ratio
- Total Harmonic Distortion (THD)
- Spurious Free Dynamic Range (SFDR)
- Effective number of bits (ENOB)
- Spurious performance
Resolution:

Number of distinct analog levels in a D/A.
Number of digital output codes in an A/D.

If a converter can "resolve" $2^N$ levels, it is generally termed an $N$-bit converter.

By design, almost all converters have ideally an integer for $N$.

If a converter can resolve $K$ levels,

$$K = 2^{N_{\text{ref}}} \quad \Rightarrow \quad N_{\text{ref}} = \log_2 K$$
Offset & Gain errors

LSB: LSB to be either one digital bit at the lowest level or

\[ X_{LSB} = \frac{X_{REF}}{2^N} \]

- Differences in slope from the desired slope are termed gain errors.
- Differences in horizontal axis crossing from the desired crossing are termed offset errors.
Integr al Nonlinearity (INL) is one widely used metric for characterizing the linearity of a DAC.