EE 435

Lecture 25

Comparators

Comparator-Based ADCs
Comparators do not have a requirement of stable linear operation when FB is applied.

Any op amp will work as a comparator but it is likely over-designed for use as a comparator.

Other architectures that are not suitable for FB applications will work as comparators as will perform better.

Desired comparator performance:
- Rail-to-Rail Output (recognizable Boolean rails at output is sufficient)
- Often wide speed
- Very high gain
- Often no hysteresis (but sometimes intentionally have hysteresis)
- Low power dissipation
- Small
- No "chatter" at transitions
Comparator Circuits

\[ V_I : V_{DD} \]

\[ V_C \]

\[ V_{TH} \text{ VERSHOLD} = V_{TR10} \]

Do-Do

High gain comparator.
Clocked Comparators.

Output depends upon condition of inputs on transition of the clock.
ADC Structure:

2^n resolutions

- Flash ADC
  - can easily be modified to be a clocked Flash ADC
  - usually operated synchronously with input \( s/t \)
Successive Approximation

- slow make $2^n$ or $n$ clock cycles

Diagram:

- DAC
- Comparator
- switches

$V_o$