EE 435

Lecture 30
R-String DAC Design
Discussion of Pelgrom 10-bit DAC
Note: This lecture is slightly out of sequence since there are two more lectures that will be given discussing quantization noise and spectral characterization. It is being included at this stage to facilitate work on the design project in this course. It is closely coupled to a seminal paper by Marcel Pelgrom that appeared in the IEEE Journal of Solid State Circuits titled “A 10-b 50MHz CMOS D/A Converter with 75-Ω Buffer”, Dec. 1990. Even though this paper is nearly 20 years old, it is an excellent example of showing how to approach the data converter design problem and the architecture introduced by Pelgrom is still used today.
Data Converter Design Strategies

- There are many different DAC and ADC architectures that have been proposed and that are in widespread use today.
- Almost all work perfectly if all components are ideal.
- Most data converter design work involves identifying the contributors to nonideal performance and finding work-arounds to these problems.
- Some architectures are more difficult to find work-arounds than others.
- All contributors to nonidealities that are problematic at a given resolution of speed level must be identified and mitigated.
- The effects of not identifying nonidealities generally fall into one of two categories:
  - Matching-critical nonidealities (degrade yield)
  - Component nonlinearities (degrade performance even if desired matching is present)
R-String DAC
R-String DAC

Basic R-String DAC including Logic to Control Switches
R-String DAC

If all components are ideal, performance of the R-string DAC is that of an ideal DAC!

Key Properties of R-String DAC
- One of the simplest DAC architectures
- R-string DAC is inherently monotone

Possible Limitations or Challenges
- Matching of resistors (will not be ideal)
- Gradient effect
- Local Random Variations
- Large registers if \( n \) is large
- Power dissipation
  \[ P_{\text{req}} = \frac{V^2}{R} \]
- Output settling time is order \( 2^n \) dependent
- Introduction distortion
- Switch nonlinearity
- Temperature (not as common with more IR drops)
- Power consumed (not a concern)
- Values in decoder (001 to 010)
- Resistor could become very large if \( n \) is large
- \( 2^n \) stands that need to be routed
- almost all area allocated to coarse string to make unruliness to coarse tips such as all the 10-50ft level.
- anti-parallel laden only and for coarse string (this mitigates to inter-tangled problem)
- added some resistors for each switch to keep RTH constant
R-String DAC

If all components are ideal, performance of the R-string DAC is that of an ideal DAC!

Key Properties of R-String DAC
- One of the simplest DAC architectures
- R-string DAC is inherently monotone

Possible Limitations or Challenges
- Binary to Thermometer Decoder (BTTD) gets large for $n$ large
- Logic delays in BTTD may degrade performance
- Matching of the resistors may not be perfect
  - Local random variations
  - Gradient effects
- How can switches be made?
R-String DAC

Typical strategy for implementing the switch

- Switch is an analog MUX
- Very simple structure
- Switch array combined with the BTTD forms a $2^n:1$ analog MUX
R-String DAC

Possible Limitations:

- Voltage can't be too large because it could turn on too many switches.
- Resistance becomes important.
- Voltage drop across MOS devices (code dependent settling).
- Switch leakage if $n$ large (in small feature size processes).
- $2^n$ diff pairs consume a lot of power from $C_L$. 

Binary to Thermometer Decoder

$V_{RFF}$

$X_{IN}$

$V_{OUT}$

$n$

$m$

$m$
R-String DAC

R-String DAC with MOS switches

Possible Limitations:

- Switch impedance is not 0
- Switch may not even turn on at all if $V_{REF}$ is large
- Switch impedance is input-code dependent
- Time constants are input-code dependent
- Transition times are previous-code dependent
- $C_L$ has $2^n$ diffusion capacitances so can get very large
- Mismatch of resistors
  - local random variation
  - gradient effects
- Decoder can get very large for $n$ large
- Routing of the $2n$ switch signals can become very long and consume lots of area
added second OEC to control $\hat{b}_{1C}$