EE 435

Lecture 35

DAC Design
DAC Architectures (Nyquist Rate)

Types

- **Voltage Scaling**
  - Resistor String DACs (string DACs)
  - Interpolating

- **Current Steering**
  - Binarily Weighted Resistors
  - R-2R Ladders
  - Current Source Steering
    - Thermometer Coded
    - Binary Weighted
    - Segmented

- **Charge Redistribution**
  - Switched Capacitor

- **Serial**
  - Algorithmic
  - Cyclic or Re-circulating
  - Pipelined

- **Integrating**

- **Resistor Switching**

- **MDACs (multiplying DACs)**
Basic R-String DAC

Latchable Boolean Signal Can Reduce/Eliminate Logic Transients which Cause Distortion
Switch Implementation Issues

n-channel

p-channel

T-gate
Switch Implementation Issues

- n-channel
- p-channel
- T-gate
Current Steering DACs

InherentlyInsensitive to Nonlinearities in Switches and Resistors
Current Steering DACs

InherentlyInsensitive to Nonlinearities in Switches and Resistors
Smaller ON resistance and less phase-shift from clock edges
Current Steering DACs

Binary to Thermometer Decoder (all ON)

Transistor Implementation of Switches
Current Steering DACs

Binary to Thermometer Decoder (all ON)

Transistor Implementation of Switches

\[ \beta = \frac{\frac{R_{\text{CELL}}}{k}}{\frac{R_{\text{CELL}}}{k} + R_F} = \frac{R_{\text{CELL}}}{R_{\text{CELL}} + kR_F} \]

If \( V_{\text{OUTFS}} = V_{\text{REF}} \)
\[ R_{\text{CELL}} = NR_F \]
\[ 0.5 < \beta \leq 1 \]
Current Steering DACs

Binary-Weighted Resistor Arrays
Current Steering DACs

Binary-Weighted Resistor Arrays

Actual layout of resistors is very important
Current Steering DACs

Segmented Resistor Arrays
Current Steering DACs

R-2R Resistor Arrays
Current Steering DACs

R-2R Resistor Arrays
Another R-2R DAC
Another R-2R DAC
Another R-2R DAC
Current Steering DAC

\[ I_{OUT} = kI \]
Current Steering DAC

\[ I_{OUT} = kI \]
Current Steering DAC
Current Steering DAC

![Diagram of a current steering DAC](image)

The diagram shows a binary-to-analog converter with a DAC designed to steer currents. The output, $V_{OUT}$, is proportional to the sum of currents $I_1, I_2, \ldots, I_{n-1}$, with $I_{OUT} = kI$, where $k$ represents the selected binary code.

The circuit includes a voltage-controlled current source (VCCS) that provides a reference current $I$ at $V_{XX}$. The decoder selects one of the $n$ current sources based on the binary input, with $d_k$ representing the decoder's output state.

The output voltage $V_{OUT}$ is then amplified by the operational amplifier (op-amp) connected to $R_f$, ensuring a linear and precise output voltage proportional to the chosen current.
Current Steering DAC

\[ \text{I} \quad \text{V}_{XX} \quad \text{V}_{SS} \quad \text{d}_k \]

\[ \text{I} \quad \text{V}_{SS} \quad \text{V}_{XX} \quad \text{d}_k \]

\[ \text{I} \quad \text{V}_{SS} \quad \text{V}_{XX} \quad \text{d}_k \quad \text{C}_p \]

\[ \text{I} \quad \text{V}_{XX} \quad \text{d}_k \quad \text{I}_{OUT} = kI \]
Current Steering DAC

- Binary to Analog Converter
- Cascode Current Source (Mirror)
- Differential Amplifier (Analog)
- \( d_k \)
- \( I \)
- \( I_{OUT} = kI \)
Current Steering DAC
Current Steering DAC

\[ \text{Current Steering DAC} \]

\[ V_{XX}, V_{YY}, V_{SS} \]

\[ M_1, M_2, M_3, M_4 \]

\[ C_{p1}, C_{p2} \]

\[ V_{OUT} \]

\[ I_{D1}, I_{D2} \]

\[ V_1, V_2 \]

\[ I_T \]

\[ I_{OUT} = kI \]

\[ R_f, V_{OUT} \]

\[ -\sqrt{2} V_{EB}, \sqrt{2} V_{EB} \]
Supply independent biasing
Dynamic Current Source Matching (Form of self calibration)
(Current Copier)
Charge Redistibtion DAC