EE 435
Lecture 36
Spring 2006

DAC Design
How can we be sure that only operate in sat/cutoff

\[ V_{gs} > \sqrt{2} V_{EB} \], one side will cut off

For set: \[ |V_{gs}| > |V_{gs} - V_{T}| \]
- Resistor usually external (50-52)
- Fully differential output
- Very high speed of operation!
Limited BW of op amp
Dump to Null or Dump to GND

Limitations of this architecture:

1) Op Amp BW will limit performance
2) Sinusoidal output likely results in large 2nd harmonic distortion
Current steering rather than current switching.


- redue Suicide on Vx
- improve quality of current source
- self-cascode effect
- `Dump to Null`  

- Difficult to perfectly synchronize \( b_c + \overline{b_k} \)

- Large signals on control of switch can cause significant feed-through from clock

- Reduce swing on controlling gates
Review from Last Time

Current Steering DACs

  – Thermometer Coded
    • Excellent DNL
    • Decoder is Large and Limits Performance

  – Binarily Weighted
    • Eliminates the need for decoder
    • Unit Cell used for Binary Weighted Elements
    • DNL can be large

  – Switches Can Cause Glitch Problems
    • Current Source Turn-Off a Problem
    • “Dump to Null” Can Help
Other DAC Architectures

- Interpolating DAC
- Current Steering DAC
- Segmented DAC
- Charge Redistribution DAC
Binarily Weighted Current-Steering DACs

Conceptual Circuit Structure

\[ I \quad 2I \quad \ldots \quad 2^{n-1}I \]
What is really used?

1) for low resolution, use thermacor cooled structure

2) for high resolution, use segmented approach
Segmented Current Steering DACs

- Large area in MSB current sources to obtain good matching
- Limit MSB bits so that decoder not problem
- Gives good DNL on MSB port

e.g. 5 bits

- Eliminates decoder on this part
- Do not get too much accumulation of mismatch to degrade DNL

e.g. 7 bits
- Clock feedthrough onto C that leads to charge

- I will choose from Ired because of output

- kT/2 noise

In floating gate processes, need for refreshing can be nearly eliminated
Add one spare current source

\[ 2^n \text{ current sources} = 2 + 1 \text{ current sources} \]

- This current source can supply current when any one source is in the precharge/calibrate state

Limitations

- charge condensation (not bad)
- over time caps (no overload - use with)
- interconnection complexity (not bad)
- speed limitation
Dynamic Current Source Matching

(Current Copier)

$\phi_1$ and $\phi_{cl}$ are non-overlapping

$\phi_{cl}$
Supply independent biasing
Switch Implementation Issues

Null Port

Dump

Null Port
R-2R Current Steering DAC
Modified R-2R DAC
Charge Redistribution DAC