EE 435
Lecture 37
Spring 2006

DAC Design
Review from Last Time

Current Steering DACs

– Op Amp removed for high-speed applications
– Differential output at minimal cost
– Current Steering
  • Steer Current with Differential Pair
  • Limit Swing so Devices Operate in Saturation/Cutoff
  • Self-Cascode Effect Improves Current Source
– Current Copier to Remove Matching Requirements
  • Still affected by output impedance of current sources
  • Clock feedthrough and sampling noise limit performance
  • Need for refreshing (can be done in background)
Calibrated Current Steering DAC

Uncalibrated Current Steering DAC
Calibrated Current Steering DAC
Generation of currents independently of $V_{DD}$

- $V_{DD}$ independent current gen.

$\mathcal{B}$ $\mathcal{E}$ $\mathcal{D}$ $\mathcal{F}$ $\mathcal{G}$ $\mathcal{H}$ $\mathcal{I}$ $\mathcal{J}$ $\mathcal{K}$ $\mathcal{L}$ $\mathcal{M}$ $\mathcal{N}$ $\mathcal{O}$ $\mathcal{P}$ $\mathcal{Q}$ $\mathcal{R}$ $\mathcal{S}$ $\mathcal{T}$ $\mathcal{U}$ $\mathcal{V}$ $\mathcal{W}$ $\mathcal{X}$ $\mathcal{Y}$ $\mathcal{Z}$

- $V_{REF}$ band select
Supply independent biasing

\[
\frac{V_{REF}}{R}
\]
DAC Architectures

• String DACs
  – Interpolating DACs

• Current Steering DACs
  – Thermometer Coded
  – Binarily Weighted
  – Segmented DACs

Resistor-Based DACs

• Charge Redistribution DACs
Thermometer coded R-based DAC
- Reduces (Eliminates code dependence on switches)
- Real resistance is $R + R_{SW}$
- Fantastic DAC
- Switch impedance may not match as well as the $R$ resistance
- B统筹 to Thermometer Decoders
- would to add 'dump' node at gnd
Binarily weighted R's
- DNL will be a problem
- eliminates decoder
- use unit cell to make R's
- adjust switch sizes (one may have code zero turn)
attractive alternative
Switch Implementation Issues

![Diagram of switch implementation issues]
- Small # resisters even when n is large
- No decoder
- INL problem
- DNL problem
- No decoder

- R-2R network must satisfy: for each code channel

\[ S_1 \rightarrow S_{n+1} ^{R-2R} \text{ resistors} \]

- Modified R-2R DAC

- R-2R network must satisfy: for each code channel

\[ S_1 \rightarrow S_{n+1} ^{R-2R} \text{ resistors} \]
DAC Architectures

• String DACs
  – Interpolating DACs

• Current Steering DACs
  – Thermometer Coded
  – Binarily Weighted
  – Segmented DACs
  – Digitally Calibrated DACs

• Resistor-Based DACs

Charge Redistribution DACs
Charge Redistribution DAC

- no decoder
- to a first order, switch impedes not of concern

\[ Q_T = Q_n \left( 2^n + \frac{Q_1}{2} + \frac{Q_2}{2^2} + \cdots + \frac{Q_n}{2^n} \right) \]

- matching or C ratios is important
- can convert to TC by making C's vertical
- segmentation is practical
EE 435

Lecture 38

ADC Design
Review from Last Time:

• Current Steering DACs are widely used
  - Current-source based
  - Resistor –based
    .. V/R structures
    .. R-2R structures
    .. Switch impedance must be managed in Resistor-Based structures

• Method of switching current significantly affects performance

• Charge Redistribution DACs can be quite energy efficient and can provide good resolution
  - Based upon switched-capacitor concept
R-2R DAC
ADC Types

**Nyquist Rate**
- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

- Can be very fast
- Moderate resolution

**Over-Sampled**
- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

- Very high resolution (24 bits)
- Slow
Nyquist Rate

One conversion completed each clock period (possible with latency)
Sampling rate limited to Nyquist-rate

\[ f_c > 2f_{sig_{max}} \]
Nyquist Rate
Over-sampling ratios of 128:1 or 64:1 are common. Dramatic reduction in quantization noise effects. Limited to relatively low frequencies.
Flash ADC

- Very fast

- Comparators are often clocked

- Input S/H is used

- Clockless comparators often more power efficient

- Offset of comparators is of major concern

- Limited to low resolution, e.g. 4, 5, 6, 7, 8...
Flash ADC

$V_{REF}$ $V_{IN}$

$R$ $R$ $R$ $R$

$2^n : n$ Encoder

$d_k$

$X_{OUT}$

$n$

CL
Flash ADC Summary

Flash ADC
Very fast
Usually Clocked
Bubble Removal Important
Seldom over 6 or 7 bits of resolution

Force everything below highest "1" to be a "1"
Clocked Comparator
Clocked Comparator
Pipelined ADC

\[ X_{OUT} = n_1 : n_2 : ... : n_m \]
Pipelined ADC
Pipelined ADC Stage $k$
Pipelined ADC Stage $k$

$X_{IN_k}$ → $ADC_k$ → $DAC_k$ → $A_k$ → $S/H_k$ → $X_{OUT_k}$

- Pipeline Stage:
  - $n_k$
  - $d_k$
  - $V_{REF}$
  - $C_{LK}$

Usually Realized as Single SC Block
Pipelined ADC Stage $k$

Pipeline Stage

$X_{INk}$

$A_k$

$S/H_k$

$X_{OUTk}$

Usually Realized as Flash ADC

(often simple comparator if $n_k = 1$)
Pipelined ADC Stage $k$

Pipeline Stage for 1 bit/stage

$X_{IN_k}$

$X_{OUT_k}$

$V_{REF}$

$C_{LK}$

$V_{IN}$

$V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & V_{IN} < 0
\end{cases}$
Transfer Characteristics for 1 bit/stage

\[ V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & \text{if } V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & \text{if } V_{IN} < 0 
\end{cases} \]
Consider the following circuit
Consider the following circuit

During $\Phi_1$

During $\Phi_2$
Consider the following circuit

\[ Q_1 = C_1 \left( V_{IN} - V^+ \right) \]
\[ Q_2 = C_2 \left( V_{IN} - V^+ \right) \]
Consider the following circuit

During $\Phi_2$

During $\Phi_1$
Consider the following circuit

\[
Q_1 = C_1 (V_{\text{IN}} - V^+) \\
Q_2 = C_2 (V_{\text{IN}} - V^+)
\]

During \( \Phi_2 \)

\[
Q_{1T} = C_1 (V_{\text{IN}} - V^+) - C_1 (V_X - V^+) = C_1 (V_{\text{IN}} - V_X)
\]

\[
Q_{2F} = Q_2 + Q_{1T} = C_2 (V_{\text{IN}} - V^+) + C_1 (V_{\text{IN}} - V_X) = (C_1 + C_2) V_{\text{IN}} - C_2 V^+ - C_1 V_X
\]
Consider the following circuit

During $\Phi_2$

\[ Q_{2F} = Q_2 + Q_{IT} = C_2 \left( V_{IN} - V^+ \right) + C_1 \left( V_{IN} - V_X \right) = \left( C_1 + C_2 \right) V_{IN} - C_2 V^+ - C_1 V_X \]

\[ V_{C2F} = \frac{Q_{2F}}{C_2} = \left( 1 + \frac{C_1}{C_2} \right) V_{IN} - V^+ - \frac{C_1}{C_2} V_X \]

\[ V_{OUTF} = V_{C2F} + V^+ = \left( 1 + \frac{C_1}{C_2} \right) V_{IN} - \frac{C_1}{C_2} V_X \]
Consider the following circuit

\[ V_{OUTF} = V_{C2F} + V^+ = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2} V_X \]

If \( C_1 = C_2 = C \) and \( V_X = -\frac{V_{REF}}{2} \)

\[ V_{OUTF} = V_{C2F} + V^+ = 2V_{IN} + \frac{V_{REF}}{2} \]
Consider the following circuit

\[
V_{\text{OUTF}} = V_{\text{C2F}} + V^+ = \left(1 + \frac{C_1}{C_2}\right)V_{\text{IN}} - \frac{C_1}{C_2}V_X
\]

If \(C_1 = C_2 = C\) and \(V_X = \frac{V_{\text{REF}}}{2}\)

\[
V_{\text{OUTF}} = V_{\text{C2F}} + V^+ = 2V_{\text{IN}} - \frac{V_{\text{REF}}}{2}
\]
Observe

\[
V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & V_{IN} < 0 
\end{cases}
\]
Pipelined ADC Stage $k$

- $X_{IN_k}$
- $ADC_k$
- $n_k$
- $d_k$
- $DAC_k$
- $A_k$
- $S/H_k$
- $X_{OUT_k}$
- $V_{REF}$
- $C_{LK}$

Usually Realized as Single SC Block
1-bit/Stage Pipeline Implementation

\[
V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & V_{IN} < 0 
\end{cases}
\]
Pipelined ADC Stage $k$

Usually Realized as Flash ADC
(often simple comparator if $n_k=1$)
1-bit/Stage Pipeline Implementation

\[ V_{INk} \]

\[ V_{REF} \quad \xrightarrow{ADC_k} \quad 1 \]

\[ d_k \]

\[ V_{INk} \quad \xrightarrow{+} \quad d_k \]