EE 435
Lecture 39
ADC Design
Clocked Comparator

Regenerative Comparators

Differential

Single-Ended

Regenerative Feedback

Large offset voltage (100mV or more)
Flash ADC with Front-End S/H
Two-Step Flash ADC

\[ X_{IN} \rightarrow S/H \rightarrow \text{Flash ADC}_1 \rightarrow \text{DAC} \rightarrow \text{Flash ADC}_2 \rightarrow \text{Digital Assembler} \rightarrow X_{OUT} \]
Two-Step Flash ADC with Interstage Gain

\[ X_{IN} \rightarrow S/H \rightarrow \text{Flash ADC}_1 \rightarrow DAC \rightarrow A \rightarrow \text{Flash ADC}_2 \rightarrow X_{OUT} \]

- \( C_{LK1} \)
- \( n_1 \) (MSB)
- \( C_{LK2} \)
- \( n_2 \) (LSB)
- Digital Assembler

\( n \) (Digital Representations)
Three-Step Flash ADC with Interstage Gain and S/H
Three-Step Flash ADC with Interstage Gain
Pipelined ADC

\[ X_{\text{OUT}} = \langle n_1:n_2: \ldots :n_m \rangle \]
Pipelined ADC

\[ S/H \xrightarrow{r_1} \text{Stage 1} \xrightarrow{r_2} \cdots \xrightarrow{r_k} \text{Stage m} \xrightarrow{r_m} \text{Shift Register} \]

Input: \( X_{IN} \)

Clock: \( C_{LK} \)

Output: \( X_{OUT} \)
Pipelined ADC Stage $k$
Pipelined ADC Stage $k$

Pipeline Stage

$X_{IN_k}$ → ADC$_k$ → DAC$_k$ → $A_k$ → $S/H_k$ → $X_{OUT_k}$

$V_{REF}$

$X_{IN_k}$ → $d_k$ → $n_k$ → $C_{LK}$

Usually Realized as Single SC Block
Pipelined ADC Stage $k$

Usually Realized as Flash ADC
(often simple comparator if $n_k=1$)
Pipelined ADC Stage $k$

Pipeline Stage for 1 bit/stage

\[ V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & V_{IN} > 0 
\end{cases} \]
Transfer Characteristics for 1 bit/stage

\[ V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & V_{IN} > 0 
\end{cases} \]
Consider the following circuit
Consider the following circuit:

During $\Phi_1$:

$V_{IN}$, $C_1$, $C_2$, $V_+'$, $V_{OUT}$, $\Phi_1$, $\Phi_2$.

$V_X$.
Consider the following circuit

During $\Phi_1$

$$Q_1 = C_1(V_{IN} - V^+)$$
$$Q_2 = C_2(V_{IN} - V^+)$$
Consider the following circuit

During $\Phi_2$
Consider the following circuit

During $\Phi_2$

Define $Q_{1T}$ to be the charge transferred from $C_1$ during phase $\Phi_2$

$$Q_{1T} = C_1 (V_{IN} - V^+) - C_1 (V_X - V^+) = C_1 (V_{IN} - V_X)$$

Define $Q_{2F}$ to be the total charge on $C_2$ during phase $\Phi_2$

$$Q_{2F} = Q_2 + Q_{1T} = C_2 (V_{IN} - V^+) + C_1 (V_{IN} - V_X) = (C_1 + C_2) V_{IN} - C_2 V^+ - C_1 V_X$$
Consider the following circuit

During $\Phi_2$

$$Q_{2F} = (C_1 + C_2)V_{IN} - C_2V^+ - C_1V_X$$

$$V_{C2F} = \frac{Q_{2F}}{C_2} = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - V^+ - \frac{C_1}{C_2}V_X$$

$$V_{OUTF} = V_{C2F} + V^+ = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2}V_X$$
Consider the following circuit

![Circuit Diagram]

\[
V_{\text{OUTF}} = \left(1 + \frac{C_1}{C_2}\right)V_{\text{IN}} - \frac{C_1}{C_2}V_X
\]

If \(C_1 = C_2 = C\) and \(V_X = -\frac{V_{\text{REF}}}{2}\)

\[
V_{\text{OUTF}} = 2V_{\text{IN}} + \frac{V_{\text{REF}}}{2}
\]
Consider the following circuit

\[
V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2} V_X
\]

Likewise

If \(C_1 = C_2 = C\) and \(V_X = \frac{V_{REF}}{2}\)

\[
V_{OUTF} = 2V_{IN} - \frac{V_{REF}}{2}
\]
Observe

\[ V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & \text{if } V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & \text{if } V_{IN} > 0 
\end{cases} \]
1-bit/Stage Pipeline Implementation

\[
V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & V_{IN} > 0 
\end{cases}
\]
1-bit/Stage Pipeline Implementation
Cyclic (Algorithmic) ADC

- Re-use Pipelined Stage
- Small amount of hardware
- Effective thru-put decreases
Interpolating ADC

- Amplifiers are finite-gain saturating
- Shown for 4-bit
- Clocked comparators usually regenerative
- Reduces Offset Requirements for Comparators
SAR ADC

- DAC Controller may be simply U/D counter
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small