Due Monday April 2

Problem 1  15.1 of Martin and Johns
Problem 2  15.2 of Martin and Johns
Problem 3  15.3 of Martin and Johns
Problem 4  15.5 of Martin and Johns
Problem 5  15.11 or Martin and Johns (the values given in the problem are the 8 DAC outputs)
Problem 6  15.13 of Martin and Johns
Problem 7  15.16 or Martin and Johns (when solving this problem, assume that the ADC is ideal and that the sampling uncertainty is to introduce an instantaneous error of at most ½ LSB beyond the quantization error).

Problem 8  The following theorem was given in class:

Theorem: If the INL of a DAC is less than ½ LSB, then the DAC is monotone.

a) Prove this theorem.

b) This theorem was sufficient but not necessary. Give an example of a DAC that is monotone but has an INL that is greater than ½ LSB.

Problem 9  16.1 of Johns and Martin (question is asking for the number of switches in the tree decoder)
Problem 10-12  (Weighted as three problems)  Assume a 5-bit DAC has the outputs shown and that $V_{\text{REF}}=5\text{V}$. See Appendix A below discussing ENOB.

a) Plot the transfer characteristics of the DAC and compare with that of an ideal DAC
b) Determine the gain error and the offset of the DAC
c) Determine the DNL of the DAC
d) Determine the INL of the DAC
e) Determine the ENOB of the DAC based upon its INL performance, denoted as $\text{ENOB}_{\text{INL}}$.

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Appendix A  ENOB for a DAC based upon INL

The ENOB for a DAC can be defined in different ways depending upon which characteristics are of most interest. If only linearity or specifically the INL is of concern, an ENOB definition based upon the linearity (INL) of a DAC is of interest. If we assume that a good n-bit DAC is designed for an INL of ½ LSB, we can define the effective number of bits, $n_{\text{EFF}}$, by the expression

$$ \frac{\text{INL}}{V_{\text{REF}}} = \frac{1}{2} \cdot \frac{1}{2^n_{\text{EFF}}} = \frac{1}{2^{n_{\text{EFF}} + 1}} $$

Or, equivalently

$$ n_{\text{EFF}} = \text{ENOB}_{\text{INL}} = \log_2 \left( \frac{V_{\text{REF}}}{\text{INL}} \right) - 1 $$

Observe that if an n-bit DAC has an INL of ½ LSB, then

$$ \text{ENOB}_{\text{INL}} = \log_2 \left( \frac{V_{\text{REF}}}{\text{INL}} \right) - 1 = \log_2 \left( \frac{2^n V_{\text{LSB}}}{V_{\text{LSB}}} \right) - 1 = \log_2 \left( 2^{n+1} \right) - 1 = n $$

So this is consistent with the premise that a good n-bit DAC with an INL of ½ LSB has an ENOB$_{\text{INL}}$ of $n$.

With this definition, the ENOB of an n-bit DAC can be larger than $n$ if the INL is smaller than $V_{\text{LSB}}$ or less than $n$ if the INL is larger than $V_{\text{LSB}}$. 