Lecture 16

Two-Stage Op Amp with LHP Zero Loop Gain - “Breaking the Loop”
Nyquist and Gain-Phase Plots convey identical information but gain-phase plots often easier to work with.

Note: The two plots do not correspond to the same system in this slide.
Review from last lecture

Gain and Phase Margin Examples

\[ T(s) = \frac{1581}{(s + 1)^2(s + 20)} \]
In general, the relationship between the phase margin and the pole Q is dependent upon the order of the transfer function and on the location of the zeros.

In the special case that the open loop amplifier is second-order low-pass, a closed form analytical relationship between pole Q and phase margin exists and this is independent of $A_0$ and $\beta$.

$$Q = \frac{\sqrt{\cos(\varphi_M)}}{\sin(\varphi_M)}$$

$$\varphi_M = \cos^{-1}\left(\sqrt{1 + \frac{1}{4Q^4}} - \frac{1}{2Q^2}\right)$$

The region of interest is invariable only for $0.5 < Q < 0.7$. Larger Q introduces unacceptable ringing and settling, smaller Q slows the amplifier down too much.
Phase Margin vs Q

Second-order low-pass Amplifier

Review from last lecture
Phase Margin vs Q

Second-order low-pass Amplifier

Review from last lecture
Review from last lecture: Magnitude Response of 2\textsuperscript{nd}-order Lowpass Function

\[ G(\Omega) = 20 \log |A_{cl}| (\text{dB}) \]

\[ \zeta = \frac{1}{2Q} \]

\[ Q_{\text{MAX}} \text{ for no peaking} = \frac{1}{\sqrt{2}} = 0.707 \]

From Laker-Sansen Text
Review from last lecture

Step Response of 2\textsuperscript{nd}-order Lowpass Function

\[ Q = \frac{1}{2\xi} \]

From Laker-Sansen Text

\( Q_{\text{MAX}} \) for no overshoot = 1/2
Compensation Summary

- Gain and phase margin performance often strongly dependent upon architecture
- Relationship between overshoot and ringing and phase margin were developed only for 2nd-order lowpass gain characteristics and differ dramatically for higher-order structures
- Absolute gain and phase margin criteria are not robust to changes in architecture or order
- It is often difficult to correctly “break the loop” to determine the loop gain $A\beta$ with the correct loading on the loop (will discuss this more later)
Design of Two-Stage Op Amps

- Compensation is critical in two-stage op amps

- General approach to designing two-stage op amps is common even though significant differences in performance for different architectures

- Will consider initially the most basic two-stage op amp with internal compensation
Natural Parameter Space for the Two-Stage Amplifier Design

\[ S_{\text{NATURAL}} = \{W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, I_T, I_{D6}, C_c\} \]
Design Degrees of Freedom

Total independent variables: 13

Degrees of Freedom: 13

If phase margin is considered a constraint

13 independent variables
1 constraint

12 degrees of freedom
Observation:
\( W, L \) appear as \( W/L \) ratio in almost all characterizing equations

Implication:
Degrees of Freedom are Reduced

\[ S_{\text{NATURAL-REDUCED}} = \{ (W/L)_1, (W/L)_3, (W/L)_5, (W/L)_6, (W/L)_7, I_{D6}, I_T, C_C \} \]

With phase margin constraint,

Degrees of freedom: 7
Common Performance Parameters of Operational Amplifiers

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ao</td>
<td>Open-loop DC Gain</td>
</tr>
<tr>
<td>GB</td>
<td>Gain-Bandwidth Product</td>
</tr>
<tr>
<td>$\Phi_m$ (or $Q$)</td>
<td>Phase Margin (or pole $Q$)</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
</tr>
<tr>
<td>$T_{SETTLE}$</td>
<td>Settling Time</td>
</tr>
<tr>
<td>$A_T$</td>
<td>Total Area</td>
</tr>
<tr>
<td>$A_A$</td>
<td>Total Active Area</td>
</tr>
<tr>
<td>$P$</td>
<td>Power Dissipation</td>
</tr>
<tr>
<td>$\sigma_{VOS}$</td>
<td>Standard Deviation of Input Referred Offset Voltage (often termed the input offset voltage)</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
</tr>
<tr>
<td>$V_{imax}$</td>
<td>Maximum Common Mode Input Voltage</td>
</tr>
<tr>
<td>$V_{imin}$</td>
<td>Minimum Common Mode Output Voltage</td>
</tr>
<tr>
<td>$V_{omax}$</td>
<td>Maximum Output Voltage Swing</td>
</tr>
<tr>
<td>$V_{omin}$</td>
<td>Minimum Output Voltage Swing</td>
</tr>
<tr>
<td>$V_{noise}$</td>
<td>Input Referred RMS Noise Voltage</td>
</tr>
<tr>
<td>$S_{v}$</td>
<td>Input Referred Noise Spectral Density</td>
</tr>
</tbody>
</table>
Performance Parameters

Total: 17
System is Generally Highly Over Constrained!

Performance parameters: 17

Degrees of freedom: 7
Typical Parameter Space for a Two-Stage Amplifier

Small signal model of the two-stage operational amplifier

Small signal design parameters:

\[ S_{\text{SMALL SIGNAL}} = \{ g_{oo}, g_{od}, g_{mo}, g_{md}, C_C, g_{o2}, g_{o4}, g_{o5}, g_{o6} \} \]
Signal Swing of Two-Stage Op Amp

\[ V_{\text{OUT}} > V_{\text{SS}} + V_{\text{EB6}} \]

\[ V_{\text{OUT}} < V_{\text{DD}} - |V_{\text{EB5}}| \]

\[ V_{iC} < V_{\text{DD}} + V_{T1} - |V_{T3}| - |V_{\text{EB3}}| \]

\[ V_{iC} < V_{\text{DD}} + V_{T1} - |V_{T5}| - |V_{\text{EB5}}| \]

\[ V_{iC} > V_{T1} + V_{\text{EB1}} + V_{\text{EB7}} + V_{\text{SS}} \]

\[ S_{\text{swing/Bias Related}} = \{ C_C, V_{\text{EB1Q}}, V_{\text{EB3Q}}, V_{\text{EB5Q}}, V_{\text{EB6Q}}, V_{\text{EB7Q}}, I_T \} \]
Signal Swing of Two-Stage Op Amp

\[ V_{OUT} < V_{DD} - |V_{EB5}| \]

\[ V_{OUT} > V_{SS} + V_{EB6} \]

\[ V_{ic} > V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]

\[ V_{ic} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}| \]

\[ V_{ic} < V_{DD} + V_{T1} - |V_{T5}| - |V_{EB5}| \]
Signal Swing of Two-Stage Op Amp

\[ V_{OUT} \]

\[ V_{DD} \]

\[ |V_{EB5}| \]

\[ V_{T1} + V_{EB1} + V_{EB7} \]

\[ V_{SS} \]

\[ V_{EB6} \]

\[ V_{SS} \]

\[ \max\{(|V_{EB3}| + |V_{T3}| - V_{T1}), (|V_{EB5}| + |V_{T5}| - V_{T2})\} \]
Augmented set of design parameters:

\[ S_{AUGMENTED} = \{ g_{oo}, g_{od}, g_{mo}, g_{md}, C_C, V_{EB1Q}, V_{EB3Q}, V_{EB5Q}, V_{EB6Q}, V_{EB7Q}, I_T, g_{o2}, g_{o4}, g_{o5}, g_{o6} \} \]

Parameters in this set are highly inter-related
Common Expressions for the Performance Parameters

\[ A_O \approx \frac{g_{md}g_{mo}}{g_{oo}g_{od}} \]

\[ GB \approx \frac{g_{md}}{C_C} \]

\[ SR \approx \frac{I_T}{C_C} \]
Common Expressions for the Performance Parameters (cont)

\[
V_{O\text{MAX}} = V_{DD} - |V_{EB5}|
\]

\[
V_{O\text{MIN}} = V_{SS} + V_{EB6}
\]

\[
V_{in\text{MIN}} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS}
\]

\[
V_{in\text{MAX}} = V_{DD} - \max\{(|V_{EB3}| + |V_{T3}| - V_{T1}), (|V_{EB5}| + |V_{T5}| - V_{T2})\}
\]
Parameter Inter-dependence

\[ A_o \approx \frac{g_{md}g_{mo}}{g_{oo}g_{od}} \]

\[ GB \approx \frac{g_{md}}{C_C} \]

\[ SR \approx \frac{I_T}{C_C} \]

\[ g_{md} \approx \frac{1}{2} \sqrt{\mu C_{OX} \frac{W_1}{L_1}} \sqrt{I_T} \]

\[ I_T \text{ affects} \]
A Set of Independent Design Parameters is Needed

Consider the Natural Reduced Parameter Set

\[
\begin{align*}
\{ & W_1, W_3, W_5, W_6, W_7, L_1, L_3, L_5, L_6, L_7, I_T, \theta \} \\
& \\
& \theta = I_{D6Q} / I_T \\
& \\
& A_O \approx \frac{g_{md} g_{mo}}{g_{oo} g_{od}} \\
& \\
& A_O = \frac{2 \sqrt{2} c_{OX} \sqrt{\mu_n \mu_p} \sqrt{W_1 W_5} \sqrt{W_6 W_7}}{(\lambda_n + \lambda_p)^2 \theta T} \sqrt{L_1 L_5 L_6 L_7}
\end{align*}
\]
\[ GB \approx \frac{g_{md}}{C_C} \]

\[
GB = \sqrt{\frac{\mu_n C_{OX} W_1}{L_1}} \sqrt{\gamma T}
\]

For a given pole \( Q \) and a feedback factor \( \beta \), it can be shown that:

\[
C_C = \frac{C_L \beta}{Q^2} \sqrt{\frac{\mu_n \mu_p}{2}} \sqrt{\frac{W_1 W_5 W_6 L_7}{L_1 L_5 L_6 L_7}} \left( \sqrt{\frac{2 \mu_p W_5 W_6 W_7}{L_5 L_6 L_7}} - \beta \sqrt{\frac{\mu_n}{L_1}} \right)^2
\]
\[ V_{\text{inMIN}} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]

\[ V_{\text{imin}} = V_{T1} + \sqrt{\frac{I_{TL1}}{\mu_n C_{OX} W_1}} + \sqrt{\frac{2I_{TL7}}{\mu_n C_{OX} W_7}} + V_{SS} \]

Expressions for signal swings are particularly complicated!
Observation

• Even the most elementary performance parameters require very complicated expressions when the natural design parameter space is used

• Strong simultaneous dependence on multiple natural design parameters

• Interdependence and notational complexity obscures insight into performance and optimization
Practical Set of Design Parameters

\[ S_{\text{PRACTICAL}} = \{ P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7} \} \]

7 degrees of freedom!

- \( P \) : total power dissipation
- \( q = I_{DQ5}/I_T \), current split factor
- \( V_{EBK} = V_{GSQK} - V_{TK} \), excess bias voltage for the \( k^{th} \) transistor
- Phase margin constraint assumed (so \( C_C \) not shown in DoF)
Basic Two-Stage Op Amp

7 Degrees of Freedom

\[
\{ P, \theta, V_{\text{EB1}}, V_{\text{EB3}}, V_{\text{EB5}}, V_{\text{EB6}}, V_{\text{EB7}} \}
\]

\[
\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}
\]
Relationship Between the Practical Parameters and the Natural Design Parameters

\[
\{ P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7} \} \]

\[
\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}
\]

\[
I_T \approx \frac{P}{V_{DD} (1+\theta)}
\]

\[
I_{DQi} \in \left\{ I_T, \frac{I_T}{2}, \theta I_T \right\}
\]

\[
\left( \frac{W}{L} \right)_i \approx \frac{2I_{DQi}}{\mu_i C_{OX} V_{EBi}^2}
\]
Relationship Between the Practical Design Parameters and the Performance Parameters

\[
A_O = \frac{4}{\left(\lambda_n + \lambda_p\right)^2 V_{EB1} \mid V_{EB5} \mid}
\]

\[
GB = \frac{P}{V_{DD} (1 + \theta) V_{EB1} C_C} = \frac{P(2\theta V_{EB1} - \beta \mid V_{EB5} \mid)^2}{4C_L \theta \beta V_{DD} (1 + \theta) V_{EB1}^2 \mid V_{EB5} \mid}
\]

\[
SR = V_{EB1} GB = \frac{P(2\theta V_{EB1} - \beta \mid V_{EB5} \mid)^2}{4C_L \theta \beta V_{DD} (1 + \theta) V_{EB1} \mid V_{EB5} \mid}
\]

\[
C_C = 4C_L \theta \beta \frac{V_{EB1} \mid V_{EB5} \mid}{\left(2\theta V_{EB1} - \beta \mid V_{EB5} \mid\right)^2}
\]

(Assuming \( Q = \frac{1}{\sqrt{2}} \))
Relationship Between the Proposed Design Parameters and the Performance Parameters

\[
V_{OMAX} = V_{DD} - |V_{EB5}|
\]

\[
V_{OMIN} = V_{SS} + V_{EB6}
\]

\[
V_{inMIN} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS}
\]

\[
V_{inMAX} = V_{DD} - \max\{(|V_{EB3}| + |V_{T3}| - V_{T1}), (|V_{EB5}| + |V_{T5}| - V_{T2})\}
\]
Characteristics of the Practical Design Parameter Space

- Minimum set of independent parameters
- Results in major simplification of the key performance parameters
- Provides valuable insight which makes performance optimization more practical
Design Assumptions

- Assume the following system parameters:
  \[ V_{DD} = 3.3 \text{ V} \]
  \[ C_L = 1 \text{ pF} \]
- Typical 0.35um CMOS process
- Simulation corner: typ/55°C/3.3V
Given specifications:

\[ A_0 : 66 \text{dB} \]
\[ \text{GB: 5MHz} \]
\[ V_{\text{OMIN}} = 0.25 \text{V} \]
\[ V_{\text{OMAX}} = 3.1 \text{V} \]
\[ V_{\text{INMIN}} = 1.1 \text{V} \]
\[ V_{\text{INMAX}} = 3 \text{V} \]

\[ P = 0.17 \text{mw} \]
\[ \beta = 1 \]

Assume: \[ V_{TN} = 0.6, \ V_{TP} = -0.7, \ \lambda_n = 0.04, \ \lambda_p = 0.18 \]

7 constraints (in addition to \( \varphi_m \)) and 7 degrees of freedom
Example for Design Procedure

1. Choose channel length
2. $V_{EB3}, V_{EB5}, V_{EB6}$
   
   \[ V_{imax} = V_{DD} + V_{EB3} + V_{T1} + V_{T3} \]
   \[ V_{omax} = V_{DD} + V_{EB5} \]
   \[ V_{omin} = V_{EB6} \]
3. $V_{EB1}$
   \[ A_O = \frac{4}{\left(\lambda_n + \lambda_p\right)^2 V_{EB1} |V_{EB5}|} \]
4. $V_{EB7}$
   \[ V_{imin} = V_{EB1} + V_{EB7} + V_{T1} \]
5. Choose $P$ to satisfy power constraint
   \[ I_T \approx \frac{P}{V_{DD} (1+\theta)} \]
Example for Design Procedure

6. Choose $\theta$ to meet GB constraint

$$GB = \frac{P}{V_{DD}(1+\theta)V_{EB1}C_C}$$

7. Compensation capacitance $C_C$

$$C_C = 4C_L\theta\beta \frac{|V_{EB1}| |V_{EB5}|}{(2\theta V_{EB1} - \beta |V_{EB5}|)^2}$$

(Assuming $Q = \frac{1}{\sqrt{2}}$)

8. Calculate all transistor sizes

$$I_T = \frac{P}{V_{DD}(1+\theta)}$$

$$\frac{W_k}{L_k} = \frac{2I_{Dk}}{\mu_k C_{OX} V_{EBk}^2}$$

9. Implement structure, simulate, and make modifications if necessary guided by where deviations may occur.

Note: It may be necessary or preferable to make some constraints an inequality

Note: Specifications may be over-constrained or have no solution
Example for Design Procedure

Design results:

<table>
<thead>
<tr>
<th>M_1,2 W/L</th>
<th>M_3,4 W/L</th>
<th>M_5 W/L</th>
<th>M_6 W/L</th>
<th>M_7 W/L</th>
<th>P</th>
<th>( \theta )</th>
<th>C_C</th>
</tr>
</thead>
<tbody>
<tr>
<td>13/2</td>
<td>24.5/2</td>
<td>54/2</td>
<td>17.4/2</td>
<td>17.4/2</td>
<td>0.17mW</td>
<td>1.06</td>
<td>3.7pF</td>
</tr>
</tbody>
</table>

Simulation results:

<table>
<thead>
<tr>
<th>A_0</th>
<th>GB</th>
<th>P</th>
<th>Phase margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>65dB</td>
<td>5.2MHz</td>
<td>0.17mW</td>
<td>45.4 degrees</td>
</tr>
</tbody>
</table>
## Spreadsheet for Design Space Exploration

### Settling Characteristics of Two-Stage Operational Amplifier

<table>
<thead>
<tr>
<th>Process Parameters</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$u_{Coxn}$</td>
<td>9E-05</td>
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<td>$u_{Coxp}$</td>
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<tr>
<td>$V_{tn}$</td>
<td>0.768</td>
</tr>
<tr>
<td>$V_{tp}$</td>
<td>0.774</td>
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</tbody>
</table>

### Design Parameters

<table>
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<tr>
<th>VEB1</th>
<th>VEB2</th>
<th>VEB5</th>
<th>VEB6</th>
<th>VEB7</th>
<th>$n$</th>
<th>Performance Characteristics</th>
<th>Input Range</th>
<th>Output Range</th>
<th>Device Sizing</th>
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<td>1.52 4.27 0.25 3.5</td>
<td>72.5 148.1</td>
<td>148.1 289.9 579.7</td>
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Summary

1. Determination of Design Space and Degrees of Freedom
   Often Useful for Understanding the Design Problem

2. Analytical Expressions for Key Performance Parameters
   give Considerable Insight Into Design Potential

3. Natural Design Parameters Often Not Most Useful
   for Providing Insight or Facilitating Optimization

4. Concepts Readily Extend to other Widely Used Structures
Basic Two-Stage Op Amp

$$A_{FB}(s) \approx \frac{g_{md}(g_{m0} - sC_c)}{s^2C_cC_L + sC_c(g_{mo} - \beta g_{md}) + \beta g_{md}g_{mo}}$$

Right Half-Plane Zero Limits Performance

Why does the RHP zero limit performance?
Can anything be done about this problem?
Why does the RHP zero limit performance?

In this example:
- accumulate phase shift and slow gain drop with RHP zeros
- effects are dramatic

$p_1=1, p_2=1000, z_x=\{\text{none, 250}\}$
Why does the RHP zero limit performance?

- Accumulate phase shift and slow gain drop with RHP zeros
- Loose phase shift and slow gain drop with RHP zeros
- Effects are dramatic

In this example:

- $p_1 = 1$, $p_2 = 1000$, $z_x = \{\text{none, 250, -250}\}$
Two-stage amplifier
(with RHP Zero Compensation)

What causes the Miller compensation capacitor to create a RHP zero?

\[ A_V = \left( A_0 p_p \right) \frac{1}{(s+p_1)(s+p_2)} \]

\[ A_V = \left( A_0 \frac{p_p}{z} \right) \frac{-s+z}{(s+p_1)(s+p_2)} \]

with Miller Compensation

\[ V_d = V_{IN^-} - V_{IN^+} \]

At low frequencies, \( V_{OUT}/V_d \) is negative but at high frequencies it becomes positive.

Alternately, \( C_C \) provides a feed-forward noninverting signal from the output of the first stage to the output of the second stage.
Two-stage amplifier
(with RHP Zero Compensation)

What can be done to remove the RHP zero?

Alternately, $C_C$ provides a feed-forward noninverting signal from the output of the first stage to the output of the second stage

Break the feed-forward path from the output of the first stage to the output of the second stage at high frequencies
Two-stage amplifier with LHP Zero Compensation

Right Half-Plane Zero Limits Performance

Zero can be moved to Left Half-Plane

$R_C$ realized with single triode region device
Two-stage amplifier with LHP Zero Compensation

\[ A(s) = \frac{g_{md} \left( g_{m5} + sC_c \left[ \frac{g_{m5}}{g_c} - 1 \right] \right)}{s^2 C_c C_L + sC_c g_{m5} + g_{oo} g_{od}} \]

\[ z_1 = \frac{-g_{m5}}{C_c \left[ \frac{g_{m5}}{g_c} - 1 \right]} \]

\( z_1 \) location can be programmed by \( R_C \)

If \( g_c > g_{m5} \), \( z_1 \) in RHP and if \( g_c < g_{m5} \), \( z_1 \) in LHP

\( R_C \) has almost no effect on \( p_1 \) and \( p_2 \)
Two-stage amplifier with LHP Zero Compensation

\[
A(s) = \frac{g_{md}\left(g_{m5} + sC_c\left[\frac{g_{m5}}{g_c} - 1\right]\right)}{s^2C_cC_L + sC_c g_{m5} + g_{oo} g_{od}}
\]

\[
z_1 = \frac{-g_{m5}}{C_c\left[\frac{g_{m5}}{g_c} - 1\right]}
\]

\[
p_1 = -\frac{g_{o1} + g_{o5}}{C_c\left[\frac{g_{m5}}{g_{o5} + g_{o6}}\right]}
\]

\[
p_2 = -\frac{g_{m5}}{C_L}
\]

where should \(z_1\) be placed?
Two-stage amplifier with LHP Zero Compensation

where should $z_1$ be placed?

$z_1 = \frac{-g_{m5}}{C_C \left[ \frac{g_{m5}}{g_C} - 1 \right]}$

$p_1 = -\frac{g_{o1} + g_{o5}}{C_C \left( \frac{g_{m5}}{g_{o5} + g_{o6}} \right)}$

$p_2 = -\frac{g_{m5}}{C_L}$

Would make situation worse (because ratio between two dominant poles would be reduced!)
Two-stage amplifier with LHP Zero Compensation

where should $z_1$ be placed?

Would make situation worse (because ratio between two dominant poles would be reduced!

Other parasitic poles, at higher frequencies are present and not too much larger than $p_2$!
Two-stage amplifier with LHP Zero Compensation

\[ z_1 = \frac{-g_{m5}}{C_C \left[ \frac{g_{m5}}{g_C} - 1 \right]} \]

\[ z_1 \] often used to cancel \( p_2 \)

Can reduce size of required compensation capacitor
  a) eliminates RHP zero
  b) increases spread between \( p_1 \) and \( p_3 \)

Improves phase margin

Design formulations easily extend to this structure
Two-stage amplifier with LHP Zero Compensation

Analytical formulation for compensation requirements not easy to obtain
(must consider at least 3rd –order poles and both T(s) and poles not mathematically tractable)

$C_C \left[ \frac{g_{m5}}{g_C} - 1 \right]$

$z_1 = -\frac{g_{m5}}{g_{m5} - 1}$

$C_C$ often chosen to meet phase margin (or settling/overshoot) requirements after all other degrees of freedom used with computer simulation from magnitude and phase plots
Basic Two-Stage Op Amp with LHP zero

8 Degrees of Freedom

\[ \{ P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}, R_C, C_C \} \]

1 constraint (phase margin)

with zero cancellation of \( p_2 \)

7 Degrees of Freedom

\[ \{ P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}, R_C, C_C \} \]

2 constraints (phase margin), \( z_1 = p_2 = \frac{-g_{m5}}{C_C \left[ \frac{g_{m5}}{g_C} - 1 \right]} \)
Basic Two-Stage Op Amp with LHP zero with zero cancellation of $p_2$

$$\begin{bmatrix} \mathbf{P} \\ \theta \\ V_{EB1} \\ V_{EB3} \\ V_{EB5} \\ V_{EB6} \\ V_{EB7} \\ R_C, C_C \end{bmatrix}$$

7 Degrees of Freedom

2 constraints (phase margin), $z_1 = p_2 = \frac{-g_{m5}}{C_C \left[ \frac{g_{m5}}{g_C} - 1 \right]}$

Design Flow:

1. Ignore $R_C$ and design as if RHP zero is present
2. Pick $R_C$ to cancel $p_2$
3. Adjust $p_1$ (i.e. change/reduce $C_C$) to achieve desired phase margin
Realization of $R_C$

$$R_C = \frac{L}{\mu C_{OX} W V_{EB}}$$

Transistors in triode region
Very little current will flow through transistors (and no dc current)
$V_{DD}$ or GND often used for $V_{XX}$ or $V_{YY}$
$V_{BQ}$ well-established since it determines $I_{Q5}$
Using an actual resistor not a good idea (will not track $gm5$ over process and temp)
Two-Stage Amplifiers
Practical Considerations

• Loop Gain
  – Loading of A and β networks
  – Breaking the Loop (with appropriate terminations)
  – Biasing of Loop
  – Simulation of Loop Gain

• Open-loop gain simulations
  – Systematic Offset
  – Embedding in closed loop
End of Lecture 16