Two-Stage Op Amp with LHP Zero Loop Gain - “Breaking the Loop”
Nyquist and Gain-Phase Plots convey identical information but gain-phase plots often easier to work with.

Note: The two plots do not correspond to the same system in this slide.
Review from last lecture

Gain and Phase Margin Examples

\[ T(s) = \frac{1581}{(s + 1)^2(s + 20)} \]
In general, the relationship between the phase margin and the pole $Q$ is dependent upon the order of the transfer function and on the location of the zeros.

In the special case that the open loop amplifier is second-order lowpass, a closed form analytical relationship between pole $Q$ and phase margin exists and this is independent of $A_0$ and $\beta$.

$$Q = \frac{\sqrt{\cos(\varphi_M)}}{\sin(\varphi_M)} \quad \varphi_M = \cos^{-1}\left(\sqrt{1 + \frac{1}{4Q^4}} - \frac{1}{2Q^2}\right)$$

The region of interest is invariable only for $0.5 < Q < 0.7$; larger $Q$ introduces unacceptable ringing and settling; smaller $Q$ slows the amplifier down too much.
Review from last lecture

Phase Margin vs $Q$

Second-order low-pass Amplifier
Phase Margin vs Q

Second-order low-pass Amplifier

Review from last lecture
Magnitude Response of 2\textsuperscript{nd}-order Lowpass Function

\[ G(\Omega) = 20 \log |A_{cl}| \text{ (dB)} \]

\[ \zeta = \frac{1}{2Q} \]

\[ Q_{\text{MAX}} \text{ for no peaking} = \frac{1}{\sqrt{2}} = .707 \]

Normalized Frequency \( (\Omega = \omega/\omega_p) \)

From Laker-Sansen Text
Review from last lecture

Step Response of 2\textsuperscript{nd}-order Lowpass Function

\[ Q_{\text{MAX}} \text{ for no overshoot } = \frac{1}{2} \]

From Laker-Sansen Text

\[ \xi = \frac{1}{2Q} \]
Compensation Summary

- Gain and phase margin performance often strongly dependent upon architecture.
- Relationship between overshoot and ringing and phase margin were developed only for 2nd-order lowpass gain characteristics and differ dramatically for higher-order structures.
- Absolute gain and phase margin criteria are not robust to changes in architecture or order.
- It is often difficult to correctly “break the loop” to determine the loop gain $A\beta$ with the correct loading on the loop (will discuss this more later).
Design of Two-Stage Op Amps

- Compensation is critical on two-stage op amps
- General approach to designing two-stage op amps is common even though significant differences in performance for different architectures
- Will consider initially the most basic two-stage op amp with internal compensation
Natural Parameter Space for the Two-Stage Amplifier Design

\[ S_{\text{NATURAL}} = \{ W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, I_T, I_{D6}, C_c \} \]
Design Degrees of Freedom

Total independent variables: 13

Degrees of Freedom: 13

If phase margin is considered a constraint, 13 independent Variables, 1 constraint and thus 12 degrees of freedom
Observation: W,L appear as W/L ratio in almost all characterizing equations

Implication: Degrees of Freedom are Reduced

$S_{\text{Natural-Reduced}} = \{(W/L)_1,(W/L)_3,(W/L)_5,(W/L)_6,(W/L)_7,I_{D6},I_T,C_C\}$

With phase margin constraint,

Degrees of freedom: 7
Common Performance Parameters of Operational Amplifiers

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_o$</td>
<td>Open-loop DC Gain</td>
</tr>
<tr>
<td>$G_B$</td>
<td>Gain-Bandwidth Product</td>
</tr>
<tr>
<td>$\Phi_m$</td>
<td>Phase Margin (or pole Q)</td>
</tr>
<tr>
<td>$S_R$</td>
<td>Slew Rate</td>
</tr>
<tr>
<td>$T_{SETTLE}$</td>
<td>Settling Time</td>
</tr>
<tr>
<td>$A_T$</td>
<td>Total Area</td>
</tr>
<tr>
<td>$A_A$</td>
<td>Total Active Area</td>
</tr>
<tr>
<td>$P$</td>
<td>Power Dissipation</td>
</tr>
<tr>
<td>$\sigma_{VOS}$</td>
<td>Standard Deviation of Input Referred Offset Voltage (often termed the input offset voltage)</td>
</tr>
<tr>
<td>$C_MRR$</td>
<td>Common Mode Rejection Ratio</td>
</tr>
<tr>
<td>$P_{SRR}$</td>
<td>Power Supply Rejection Ratio</td>
</tr>
<tr>
<td>$V_{imax}$</td>
<td>Maximum Common Mode Input Voltage</td>
</tr>
<tr>
<td>$V_{imin}$</td>
<td>Minimum Common Mode Output Voltage</td>
</tr>
<tr>
<td>$V_{omax}$</td>
<td>Maximum Output Voltage Swing</td>
</tr>
<tr>
<td>$V_{omin}$</td>
<td>Minimum Output Voltage Swing</td>
</tr>
<tr>
<td>$V_{noise}$</td>
<td>Input Referred RMS Noise Voltage</td>
</tr>
<tr>
<td>$S_v$</td>
<td>Input Referred Noise Spectral Density</td>
</tr>
</tbody>
</table>
Performance Parameters

Total: 17
Performance Parameters

Total: 17

System is Generally Highly Over Constrained!
Augmented set of design parameters:

\[ S_{\text{AUGMENTED}} = \{g_{oo}, g_{od}, g_{mo}, g_{md}, C_C, V_{EB1Q}, V_{EB3Q}, V_{EB5Q}, V_{EB6Q}, V_{EB7Q}, I_T, g_{o2}, g_{o4}, g_{o5}, g_{o6}\} \]
Signal Swing of Two-Stage Op Amp

M6: \( V_{OUT} > V_{SS} + V_{EB6} \)

M5: \( V_{OUT} < V_{DD} - |V_{EB5}| \)

M1: \( V_iC < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}| \)

M2: \( V_iC < V_{DD} + V_{T1} - |V_{T5}| - |V_{EB5}| \)

M7: \( V_{ic} > V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \)
Signal Swing of Two-Stage Op Amp

\[ V_{OUT} < V_{DD} - |V_{EB5}| \]

\[ V_{OUT} > V_{SS} + V_{EB6} \]

\[ V_{ic} > V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]

\[ V_{IC} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}| \]

\[ V_{IC} < V_{DD} + V_{T1} - |V_{T5}| - |V_{EB5}| \]
Signal Swing of Two-Stage Op Amp

\[ V_{\text{OUT}} = V_{\text{DD}} + |V_{\text{EB5}}| \]

\[ V_{\text{T1}} + V_{\text{EB1}} + V_{\text{EB7}} \]

\[ V_{\text{SS}} \]

\[ V_{\text{DD}} \]

\[ V_{\text{EB6}} \]

\[ V_{\text{SS}} \]

\[ \max\{|V_{\text{EB3}}| + |V_{\text{T3}}| - V_{\text{T1}}|, \]
\[ (|V_{\text{EB5}}| + |V_{\text{T5}}| - V_{\text{T2}})\]
Common Expressions for the Performance Parameters

\[ A_o \approx \frac{g_{md}g_{mo}}{g_{oo}g_{od}} \]

\[ GB \approx \frac{g_{md}}{C_C} \]

\[ SR \approx \frac{l_T}{C_C} \]
Common Expressions for the Performance Parameters (cont)

\[ V_{OMAX} = V_{DD} - |V_{EB5}| \]
\[ V_{OMIN} = V_{SS} + V_{EB6} \]
\[ V_{inMIN} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]
\[ V_{inMAX} = V_{DD} - \max\{(|V_{EB3}| + |V_{T3}| - V_{T1}), (|V_{EB5}| + |V_{T5}| - V_{T2})\} \]
Parameter Inter-dependence

\[ A_0 \approx \frac{g_{md} g_{mo}}{g_{oo} g_{od}} \]

\[ GB \approx \frac{g_{md}}{C_C} \]

\[ SR \approx \frac{I_T}{C_C} \]

\[ g_{md} \approx \frac{1}{2} \sqrt{\mu C_{OX} \frac{W_1}{L_1}} \sqrt{I_T} \]

\[ I_T \text{ affects} \]
A Set of Independent Design Parameters is Needed

Consider the Natural Reduced Parameter Set

\[
\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}
\]

\[
\theta = \frac{I_{D6Q}}{I_T}
\]

\[
A_O \approx \frac{g_{md} g_{mo}}{g_{oo} g_{od}}
\]

\[
A_O = \frac{2\sqrt{2}C_{Ox} \sqrt{\mu_n \mu_p} \sqrt{\frac{W_1 W_5}{L_1 L_5}}}{(\lambda_n + \lambda_p)^2 I_T \sqrt{\frac{W_6 L_7}{W_7 L_6}}}
\]
\[ GB \simeq \frac{g_{md}}{C_C} \]

\[ GB = \sqrt{\frac{\mu_n C_{OX} W_1}{L_1}} \sqrt{I_T} \]

For a given pole Q and a feedback factor \( \beta \), it can be shown that:

\[ C_C = \frac{C_L \beta}{Q^2} \frac{\sqrt{\mu_n \mu_p}}{\sqrt{\frac{2}{L_1 L_5 L_6 W_7}}} \sqrt{\frac{W_1 W_5 W_6 W_7}{L_1 L_5 L_6 W_7}} \frac{\left( \sqrt{2\mu_p \frac{W_5 W_6 W_7}{L_5 L_6 L_7}} - \beta \sqrt{\frac{\mu_n W_1}{L_1}} \right)^2}{2} \]
\[ V_{in\text{MIN}} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]

\[ V_{imin} = V_{T1} + \sqrt{\frac{I_{TL1}}{\mu_n C_{OX} W_1}} + \sqrt{\frac{2I_{TL7}}{\mu_n C_{OX} W_7}} + V_{SS} \]

Expressions for signal swings are particularly complicated!
Observation

- Even the most elementary performance parameters require very complicated expressions when the natural design parameter space is used.

- Strong simultaneous dependence on multiple natural design parameters.

- Interdependence and notational complexity obscures insight into performance and optimization.
Practical Set of Design Parameters

$S_{\text{PRACTICAL}} = \{ P, \theta, V_{\text{EB1}}, V_{\text{EB3}}, V_{\text{EB5}}, V_{\text{EB6}}, V_{\text{EB7}} \}$

7 degrees of freedom!

- $P$: total power dissipation
- $\theta = \frac{I_{DQ5}}{I_T}$, current split factor
- $V_{\text{EBK}} = V_{\text{GSQK}} - V_{\text{TK}}$, excess bias voltage for the k’th transistor
- Phase margin constraint assumed (so $C_C$ not shown in DoF)
Basic Two-Stage Op Amp

7 Degrees of Freedom

\{ P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7} \}

\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}
Relationship Between the Practical Parameters and the Natural Design Parameters

\[
\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}
\]

\[
\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}
\]

\[
I_T \approx \frac{2I_{DQi}}{\mu_i C_{OX} V_{EBi}^2}
\]

\[
I_{DQi} \in \left\{ I_T, \frac{I_T}{2}, \theta I_T \right\}
\]
Relationship Between the Practical Design Parameters and the Performance Parameters

(Assuming \( Q = \frac{1}{\sqrt{2}} \))

\[
A_O = \frac{4}{(\lambda_n + \lambda_p)^2 V_{EB1} |V_{EB5}|}
\]

\[
GB = \frac{P}{V_{DD}(1+\theta)V_{EB1}C_C} = \frac{P(2\theta V_{EB1} - \beta|V_{EB5}|)^2}{4C_L \theta \beta V_{DD}(1+\theta)V_{EB1}^2|V_{EB5}|}
\]

\[
SR = V_{EB1}GB = \frac{P(2\theta V_{EB1} - \beta|V_{EB5}|)^2}{4C_L \theta \beta V_{DD}(1+\theta)V_{EB1}^2|V_{EB5}|}
\]

\[
C_C = 4C_L \theta \beta \frac{V_{EB1}|V_{EB5}|}{\left(2\theta V_{EB1} - \beta|V_{EB5}| \right)^2}
\]
Relationship Between the Proposed Design Parameters and the Performance Parameters

\[ V_{\text{OMAX}} = V_{\text{DD}} - |V_{\text{EB5}}| \]
\[ V_{\text{OMIN}} = V_{\text{SS}} + V_{\text{EB6}} \]
\[ V_{\text{inMIN}} = V_{T1} + V_{\text{EB1}} + V_{\text{EB7}} + V_{\text{SS}} \]
\[ V_{\text{inMAX}} = V_{\text{DD}} - \max\{(|V_{\text{EB3}}| + |V_{T3}| - V_{T1}), (|V_{\text{EB5}}| + |V_{T5}| - V_{T2})\} \]
Characteristics of the Practical Design Parameter Space

- Minimum set of independent parameters
- Results in major simplification of the key performance parameters
- Provides valuable insight which makes performance optimization more practical
Example for Design Procedure

Given specification:

Ao: 66dB
GB: 5MHz
Vomin=0.25V
Vomax=3.1V
Vimin=1.1V
Vimax=3V

P=0.17mw
β=1

Assume: VTN=0.6, VTP=–0.7, λn=0.04, λp=0.18

7 constraints (in addition to φm) and 7 degrees of freedom
Design Assumptions

• Assume the following system parameters:
  \[ V_{DD} = 3.3 \, \text{V} \]
  \[ C_L = 1 \, \text{pF} \]

• Typical 0.35um CMOS process

• Simulation corner: typ/55°C/3.3V
Example for Design Procedure

1. Choose channel length

2. $V_{EB3}, V_{EB5}, V_{EB6}$
   \[ V_{imax} = V_{DD} + V_{EB3} + V_{T1} + V_{T3} \]
   \[ V_{omax} = V_{DD} + V_{EB5} \]
   \[ V_{omin} = V_{EB6} \]

3. $V_{EB1}$
   \[ A_O = \frac{4}{(\lambda_n + \lambda_p)^2 V_{EB1} |V_{EB5}|} \]

4. $V_{EB7}$
   \[ V_{imin} = V_{EB1} + V_{EB7} + V_{T1} \]

5. Choose $P$ to satisfy power constraint
   \[ I_T = \frac{P}{V_{DD} (1+\theta)} \]
Example for Design Procedure

6. Choose $\theta$ to meet GB constraint

$$GB = \frac{P}{V_{DD}(1+\theta)V_{EB1}C_C}$$

7. Compensation capacitance $C_C$

$$C_C = 4C_L\theta\beta \frac{|V_{EB1}||V_{EB5}|}{(2\theta V_{EB1} - \beta |V_{EB5}|)^2}$$

8. Calculate all transistor sizes

$$I_T = \frac{P}{V_{DD}(1+\theta)}$$

$$\frac{W_k}{L_k} = \frac{2I_{Dk}}{\mu_k C_{OX} V_{EBk}^2}$$

9. Implement structure, simulate, and make modifications if necessary guided by where deviations may occur

Note: It may be necessary or preferable to make some constraints an inequality

Note: Specifications may be over-constrained or have no solution
### Example for Design Procedure

Simulation result:

<table>
<thead>
<tr>
<th>(W/L)_{1,2}</th>
<th>13/2</th>
<th>(W/L)_{3,4}</th>
<th>24.5/2</th>
<th>(W/L)_{5}</th>
<th>54/2</th>
</tr>
</thead>
<tbody>
<tr>
<td>(W/L)_{6,7}</td>
<td>17.4/2</td>
<td>C_{C}</td>
<td>3.7pF</td>
<td>( \phi )phase</td>
<td>45.4deg.</td>
</tr>
<tr>
<td>I_{SS}</td>
<td>25uA</td>
<td>I_{S}</td>
<td>26.68uA</td>
<td>0</td>
<td>1.06</td>
</tr>
<tr>
<td>GB</td>
<td>5.2MHz</td>
<td>P</td>
<td>0.17mw</td>
<td>V_{EB7}</td>
<td>0.2</td>
</tr>
</tbody>
</table>

| Ao | 65dB |

Simulation result:

**Ao** 65dB
## Settling Characteristics of Two-Stage Operational Amplifier

### Process Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>$\mu$Coxn</td>
<td>9E-05</td>
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<tr>
<td>$\mu$Coxp</td>
<td>5E-05</td>
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<tr>
<td>$V_{tn}$</td>
<td>0.768</td>
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<tr>
<td>$V_{tp}$</td>
<td>0.774</td>
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</tbody>
</table>

### Performance Characteristics

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Performance Characteristics</th>
<th>Input Range</th>
<th>Output Range</th>
<th>Device Sizing</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/L5</td>
<td>Ao</td>
<td>GB</td>
<td>ISS(mA)</td>
<td>CC</td>
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<td>0.5</td>
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<td>8.3E+08</td>
<td>1.67</td>
<td>4E-12</td>
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<td>1</td>
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<td>8.9E-13</td>
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<tr>
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</tr>
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### VEB1, VEB2, VEB5, VEB6, VEB7

<table>
<thead>
<tr>
<th>VEB1</th>
<th>VEB2</th>
<th>VEB5</th>
<th>VEB6</th>
<th>VEB7</th>
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<tr>
<td>0.5</td>
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<td>0.5</td>
<td>0.25</td>
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<td>0.25</td>
<td>0.25</td>
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</tbody>
</table>
Summary

1. Determination of Design Space and Degrees of Freedom Often Useful for Understanding the Design Problem

2. Analytical Expressions for Key Performance Parameters give Considerable Insight Into Design Potential

3. Natural Design Parameters Often Not Most Useful for Providing Insight or Facilitating Optimization

4. Concepts Readily Extend to other Widely Used Structures
Basic Two-Stage Op Amp

\[ A_{FB}(s) \approx \frac{g_{md}(g_{m0} - sC_c)}{s^2 C_C C_L + sC_C(g_{mo} - \beta g_{md}) + \beta g_{md}g_{mo}} \]

Right Half-Plane Zero Limits Performance

Why does the RHP zero limit performance? Can anything be done about this problem?
Why does the RHP zero limit performance?

- accumulate phase shift and slow gain drop with RHP zeros
- effects are dramatic

In this example:
- $p_1=1$, $p_2=1000$, $z_x=\{\text{none, 250}\}$
- accumulate phase shift and slow gain drop with RHP zeros
- effects are dramatic
Why does the RHP zero limit performance?

- Accumulate phase shift and slow gain drop with RHP zeros
- Loose phase shift and slow gain drop with RHP zeros
- Effects are dramatic

In this example:
- \( p_1 = 1, p_2 = 1000, z_x = \{\text{none, 250, -250}\} \)
Two-stage amplifier
(with RHP Zero Compensation)

What causes the Miller compensation capacitor to create a RHP zero?

\[ A_V = \left( A_0 p_1 p_2 \right) \frac{1}{(s+p_1)(s+p_2)} \]

with Miller Compensation

\[ A_V = \left( A_0 \frac{p_1 p_2}{z} \right) \frac{-s+z}{(s+p_1)(s+p_2)} \]

\[ V_d = V_{in^+} - V_{in^-} \]

At low frequencies, \( V_{OUT}/V_d \) is negative but at high frequencies it becomes positive.

Alternately, \( C_C \) provides a feed-forward noninverting signal from the output of the first stage to the output of the second stage.
Two-stage amplifier
(with RHP Zero Compensation)

What can be done to remove the RHP zero?

\[ A_V = \left( A_0 p_1 p_2 \right) \frac{1}{(s+p_1)(s+p_2)} \]

with Miller Compensation

\[ A_V = \left( A_0 \frac{p_1 p_2}{z} \right) \frac{-s+z}{(s+p_1)(s+p_2)} \]

Alternately, \( C_C \) provides a feed-forward noninverting signal from the output of the first stage to the output of the second stage.

Break the feed-forward path from the output of the first stage to the output of the second stage at high frequencies.
Two-stage amplifier with LHP Zero Compensation

Right Half-Plane Zero Limits Performance

Zero can be moved to Left Half-Plane

$R_C$ realized with single triode region device
Two-stage amplifier with LHP Zero Compensation

\[ A(s) = \frac{g_{md} \left( g_{m5} + sC_c \left[ \frac{g_{m5}}{g_c} - 1 \right] \right)}{s^2 C_c C_L + sC_c g_{m5} + g_{oo} g_{od}} \]

\[ z_1 = \frac{-g_{m5}}{C_c \left[ \frac{g_{m5}}{g_c} - 1 \right]} \]

- \( z_1 \) location can be programmed by \( R_C \)
- If \( g_c > g_{m5} \), \( z_1 \) in RHP and if \( g_c < g_{m5} \), \( z_1 \) in LHP
- \( R_C \) has almost no effect on \( p_1 \) and \( p_2 \)
Two-stage amplifier with LHP Zero Compensation

\[
A(s) = \frac{g_{md}\left( g_{m5} + sC_c\left[ \frac{g_{m5}}{g_c} - 1 \right]\right)}{s^2C_cC_L + sC_c g_{m5} + g_{oo} g_{od}}
\]

\[
z_1 = \frac{-g_{m5}}{C_c\left[ \frac{g_{m5}}{g_c} - 1 \right]}
\]

\[
p_1 = -\frac{g_{o1} + g_{o5}}{C_c\left( \frac{g_{m5}}{g_{o5} + g_{o6}} \right)}
\]

\[
p_2 = -\frac{g_{m5}}{C_L}
\]

where should \(z_1\) be placed?
Two-stage amplifier with LHP Zero Compensation

where should $z_1$ be placed?

$$z_1 = \frac{-g_{m5}}{C_C \left[ \frac{g_{m5}}{g_C} - 1 \right]}$$

$$p_1 = -\frac{g_{o1} + g_{o5}}{C_C \left( \frac{g_{m5}}{g_{o5} + g_{o6}} \right)}$$

$$p_2 = -\frac{g_{m5}}{C_L}$$

Would make situation worse (because ratio between two dominant poles would be reduced!)
Two-stage amplifier with LHP Zero Compensation

where should $z_1$ be placed?

Would make situation worse (because ratio between two dominant poles would be reduced!)

Other parasitic poles, at higher frequencies are present and not too much larger than $p_2$!
Two-stage amplifier with LHP Zero Compensation

\[ z_1 = \frac{-g_{m5}}{C_C \left[ \frac{g_{m5}}{g_C} - 1 \right]} \]

\( z_1 \) often used to cancel \( p_2 \)

Can reduce size of required compensation capacitor

a) eliminates RHP zero

b) increases spread between \( p_1 \) and \( p_3 \)

Improves phase margin

Design formulations easily extend to this structure
Two-stage amplifier with LHP Zero Compensation

Analytical formulation for compensation requirements not easy to obtain
(must consider at least 3rd –order poles and both T(s) and poles not
mathematically tractable)

$z_1 = \frac{-g_{m5}}{C_C \left[ \frac{g_{m5}}{g_C} - 1 \right]}$

$C_C$ often chosen to meet phase margin (or settling/overshoot) requirements
after all other degrees of freedom used with computer simulation from magnitude
and phase plots
Basic Two-Stage Op Amp with LHP zero

8 Degrees of Freedom

\[ \{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}, R_C, C_C\} \]

1 constraint (phase margin)

with zero cancellation of \( p_2 \)

7 Degrees of Freedom

\[ \{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}, R_C, C_C\} \]

2 constraints (phase margin), \( z_1 = p_2 = -\frac{g_{m5}}{C_C} \left[ \frac{g_{m5}}{g_C} - 1 \right] \)
Basic Two-Stage Op Amp with LHP zero with zero cancellation of $p_2$

7 Degrees of Freedom

$\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}, R_C, C_C\}$

2 constraints (phase margin), $z_1 = p_2 = \frac{-g_{m5}}{C_C\left[\frac{g_{m5}}{g_C} - 1\right]}$

Design Flow:

1. Ignore $R_C$ and design as if RHP zero is present
2. Pick $R_C$ to cancel $p_2$
3. Adjust $p_1$ (i.e. change/reduce $C_C$) to achieve desired phase margin
Basic Two-Stage Op Amp with LHP zero

Realization of $R_C$

$$R_C = \frac{L}{\mu C_{OX} W V_{EB}}$$

Transistors in triode region

Very little current will flow through transistors (and no dc current)

$V_{DD}$ or GND often used for $V_{XX}$ or $V_{YY}$

$V_{BQ}$ well-established since it determines $I_{Q5}$

Using an actual resistor not a good idea (will not track $gm5$ over process and temp)
Two-Stage Amplifiers
Practical Considerations

• Loop Gain
  – Loading of $A$ and $\beta$ networks
  – Breaking the Loop (with appropriate terminations)
  – Biasing of Loop
  – Simulation of Loop Gain

• Open-loop gain simulations
  – Systematic Offset
  – Embedding in closed loop
Loop Gain - $A\beta$

(for voltage-series feedback configuration)

The loop is often broken on the circuit schematic to determine the loop gain.
Loop Gain - $A_\beta$

Breaking the loop to obtain the loop gain

\[ V_{IN} A V V_1 V_1 \]

\[ R_2 \]

\[ R_1 \]

\[ V_{OUT} \]

\[ R_L \]

\[ \beta = \frac{R_1}{R_1+R_2} \]

Note terminations where the loop is broken – open and short

\[ v_{LP} = v_{IN} A_V \frac{R_1}{R_1+R_2} \]

\[ \frac{v_{LP}}{v_{IN}} = A_{LOOP} = A_\beta \]
Loop Gain - $A\beta$

But what if the amplifier is not ideal?

For the feedback amplifier:

$$V_{OUT}(G_O + G_L + G_2) = V_X G_2 + A_V V_1 G_O$$
$$V_X (G_1 + G_2 + G_{IN}) = V_{OUT} G_2 + V_{IN} G_{IN}$$
$$V_{IN} = V_1 + V_X$$

Solving, we obtain

$$A_{FB} = \frac{V_{OUT}}{V_{IN}} = \frac{G_{IN} G_2 + A_V (G_O [G_1 + G_2])}{(G_O + G_L) [G_1 + G_2 + G_{IN}] + G_2 (G_1 + G_{IN}) + A_V G_2 G_O}$$

What is the Loop Gain? Needed to obtain the Phase Margin!
Loop Gain - $A\beta$

But what if the amplifier is not ideal?

$\beta = \frac{R_1}{R_1+R_2}$

$\beta = \frac{G_2}{G_1+G_2}$

$A_{FB} = \frac{v_{OUT}}{v_{IN}} = \frac{G_{IN}G_2 + A_V \left( G_O \left[ G_1+G_2 \right] \right)}{(G_O + G_L)[G_1+G_2+G_1N]+G_2 \left( G_1+G_1N \right) + A_V G_2 G_O}$

Can be rewritten as

$A_{FB} = \frac{G_{IN}G_2}{(G_O + G_L)[G_1+G_2+G_1N]+G_2 \left( G_1+G_1N \right)} + A_V \left( \frac{G_O \left[ G_1+G_2 \right]}{(G_O + G_L)[G_1+G_2+G_1N]+G_2 \left( G_1+G_1N \right)} \right) 1 + A_V \left[ \frac{G_2 G_O}{(G_O + G_L)[G_1+G_2+G_1N]+G_2 \left( G_1+G_1N \right)} \right]$ 

The Loop Gain is

$A_{LP} = A_V \left[ \frac{G_2 G_O}{(G_O + G_L)[G_1+G_2+G_1N]+G_2 \left( G_1+G_1N \right)} \right]$
Loop Gain - $A\beta$

But what if the amplifier is not ideal?

$V_{IN}$

$A$

$V_{1}$

$R_{0}$

$V_{OUT}$

$R_{L}$

$V_{X}$

$R_{1}$

$R_{2}$

$A_{LP} = A_{V} \left[ \frac{G_{2}G_{O}}{(G_{O} + G_{L})(G_{1}+G_{2}+G_{IN})+G_{2}(G_{1}+G_{IN})} \right]$

This can be rewritten as

$A_{LP} = \left( A_{V} \left[ \frac{G_{O}(G_{1}+G_{2})}{(G_{O} + G_{L})(G_{1}+G_{2}+G_{IN})+G_{2}(G_{1}+G_{IN})} \right] \right) \left[ \frac{G_{2}}{G_{1}+G_{2}} \right]$

This is of the form

$A_{LP} = (A_{VL}) \left[ \frac{G_{2}}{G_{1}+G_{2}} \right]$

Where $A_{VL}$ is the open loop gain including loading of the load and $\beta$ network!

$A_{VL} = A_{V} \left[ \frac{G_{O}(G_{1}+G_{2})}{(G_{O} + G_{L})(G_{1}+G_{2}+G_{IN})+G_{2}(G_{1}+G_{IN})} \right]$

$\beta = \frac{R_{1}}{R_{1}+R_{2}}$

$\beta = \frac{G_{2}}{G_{1}+G_{2}}$
Loop Gain - $A\beta$

But what if the amplifier is not ideal?

The Loop Gain is

$$A_{LP} = A_V \left[ \frac{G_2 G_O}{(G_O + G_L)[G_1 + G_2 + G_{IN}] + G_2 (G_1 + G_{IN})} \right]$$

$$A_{VL} = A_V \left[ \frac{G_O (G_1 + G_2)}{(G_O + G_L)[G_1 + G_2 + G_{IN}] + G_2 (G_1 + G_{IN})} \right]$$

Note that $A_{VL}$ is affected by both its own input and output impedance and that of the $\beta$ network.

This is a really “messy” expression.

Any “breaking” of the loop that does not result in this expression will result in some errors though they may be small.

$\beta = \frac{R_1}{R_1 + R_2}$

$\beta = \frac{G_2}{G_1 + G_2}$
End of Lecture 17-18