EE 435

Lecture 18

Systematic Two-Stage Op Amp Design
Nyquist and Gain-Phase Plots convey identical information but gain-phase plots often easier to work with

Note: The two plots do not correspond to the same system in this slide
Gain and Phase Margin Examples

\[ T(s) = \frac{1581}{(s + 1)^2(s + 20)} \]

Review from last lecture

Magnitude in dB

Phase Margin

Angle in degrees
In general, the relationship between the phase margin and the pole Q is dependent upon the order of the transfer function and on the location of the zeros.

In the special case that the open loop amplifier is second-order low-pass, a closed form analytical relationship between pole Q and phase margin exists and this is independent of \( A_0 \) and \( \beta \).

\[
Q = \frac{\sqrt{\cos(\varphi_M)}}{\sin(\varphi_M)}
\]

\[
\varphi_M = \cos^{-1}\left(\sqrt{1 + \frac{1}{4Q^4}} - \frac{1}{2Q^2}\right)
\]

The region of interest is invariable only for \( 0.5 < Q < 0.7 \). Larger Q introduces unacceptable ringing and settling. Smaller Q slows the amplifier down too much.
Phase Margin vs Q

Second-order low-pass Amplifier

Review from last lecture
Phase Margin vs Q

Second-order low-pass Amplifier

Review from last lecture
Review from last lecture

Magnitude Response of 2\textsuperscript{nd}-order Lowpass Function

\[ \xi = \frac{1}{2Q} \]

\[ Q_{\text{MAX}} \text{ for no peaking } = \frac{1}{\sqrt{2}} = 0.707 \]

From Laker-Sansen Text
Review from last lecture

Step Response of 2\textsuperscript{nd}-order Lowpass Function

\[ Q_{\text{MAX}} \text{ for no overshoot } = \frac{1}{2} \]

\[ \zeta = \frac{1}{2Q} \]

From Laker-Sansen Text
Compensation Summary

- Gain and phase margin performance often strongly dependent upon architecture
- Relationship between overshoot and ringing and phase margin were developed only for 2nd-order lowpass gain characteristics and differ dramatically for higher-order structures
- Absolute gain and phase margin criteria are not robust to changes in architecture or order
- It is often difficult to correctly “break the loop” to determine the loop gain $A\beta$ with the correct loading on the loop (will discuss this more later)
Design of Two-Stage Op Amps

- Compensation is critical on two-stage op amps
- General approach to designing two-stage op amps is common even though significant differences in performance for different architectures
- Will consider initially the most basic two-stage op amp with internal compensation
Natural Parameter Space for the Two-Stage Amplifier Design

\[
S_{\text{NATURAL}} = \{W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, I_T, I_{D6}, C_c, V_{B2}, V_{B3}\}
\]
Design Degrees of Freedom

Total independent variables: 15

Degrees of Freedom: 15

If phase margin is considered a constraint, 15 independent variables, 1 constraint and thus 14 degrees of freedom
Observation: W,L appear as W/L ratio in almost all characterizing equations.

Implication: Degrees of Freedom are Reduced

$$S_{\text{NATURAL-REDUCED}} = \{(W/L)_1, (W/L)_3, (W/L)_5, (W/L)_6, (W/L)_7, I_{D6}, I_T, C_C\}$$

With phase margin constraint,

Degrees of freedom: 7
# Common Performance Parameters of Operational Amplifiers

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_0$</td>
<td>Open-loop DC Gain</td>
</tr>
<tr>
<td>$GB$</td>
<td>Gain-Bandwidth Product</td>
</tr>
<tr>
<td>$\Phi m$ (or $Q$)</td>
<td>Phase Margin (or pole $Q$)</td>
</tr>
<tr>
<td>$SR$</td>
<td>Slew Rate</td>
</tr>
<tr>
<td>$T_{SETTLE}$</td>
<td>Settling Time</td>
</tr>
<tr>
<td>$A_T$</td>
<td>Total Area</td>
</tr>
<tr>
<td>$A_A$</td>
<td>Total Active Area</td>
</tr>
<tr>
<td>$P$</td>
<td>Power Dissipation</td>
</tr>
<tr>
<td>$\sigma_{VOS}$</td>
<td>Standard Deviation of Input Referred Offset Voltage (often termed the input offset voltage)</td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common Mode Rejection Ratio</td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power Supply Rejection Ratio</td>
</tr>
<tr>
<td>$V_{imax}$</td>
<td>Maximum Common Mode Input Voltage</td>
</tr>
<tr>
<td>$V_{imin}$</td>
<td>Minimum Common Mode Output Voltage</td>
</tr>
<tr>
<td>$V_{omax}$</td>
<td>Maximum Output Voltage Swing</td>
</tr>
<tr>
<td>$V_{omin}$</td>
<td>Minimum Output Voltage Swing</td>
</tr>
<tr>
<td>$V_{noise}$</td>
<td>Input Referred RMS Noise Voltage</td>
</tr>
<tr>
<td>$S_{v}$</td>
<td>Input Referred Noise Spectral Density</td>
</tr>
</tbody>
</table>
Performance Parameters

Total: 17
Performance Parameters

Total: 17

System is Generally Highly Over Constrained!
Typical Parameter Space for a Two-Stage Amplifier

Augmented set of design parameters:

\[ S_{\text{AUGMENTED}} = \{ g_{oo}, g_{od}, g_{mo}, g_{md}, C_C, V_{EB1Q}, V_{EB3Q}, V_{EB5Q}, V_{EB6Q}, V_{EB7Q}, I_T, g_{o2}, g_{o4}, g_{o5}, g_{o6} \} \]
Signal Swing of Two-Stage Op Amp

\[ V_{\text{OUT}} > V_{SS} + V_{EB6} \]

\[ V_{\text{OUT}} < V_{DD} - |V_{EB5}| \]

\[ V_{ic} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}| \]

\[ V_{ic} < V_{DD} + V_{T1} - |V_{T5}| - |V_{EB5}| \]

\[ V_{ic} > V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]
Signal Swing of Two-Stage Op Amp

\[ \max\{(|V_{EB3}| + |V_{T3} - V_{T1}|, \quad (|V_{EB5}| + |V_{T5} - V_{T2}|)\} \]

\[ V_{OUT} < V_{DD} - |V_{EB5}| \]

\[ V_{OUT} > V_{SS} + V_{EB6} \]

\[ V_{ic} > V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]

\[ V_{ic} < V_{DD} + V_{T1} - |V_{T3} - |V_{EB3}| \]

\[ V_{ic} < V_{DD} + V_{T1} - |V_{T5} - |V_{EB5}| \]
Signal Swing of Two-Stage Op Amp

\[ V_{T1} + V_{EB1} + V_{EB7} \]

\[ \left| V_{EB5} \right| \]

\[ \max\{ (|V_{EB3}| + |V_{T3}| - V_{T1}) , (|V_{EB5}| + |V_{T5}| - V_{T2}) \} \]
Common Expressions for the Performance Parameters

\[ A_o \approx \frac{g_{md} g_{mo}}{g_{oo} g_{od}} \]

\[ GB \approx \frac{g_{md}}{C_C} \]

\[ SR \approx \frac{I_T}{C_C} \]
Common Expressions for the Performance Parameters (cont)

\[ V_{OMAX} = V_{DD} - |V_{EB5}| \]

\[ V_{OMIN} = V_{SS} + V_{EB6} \]

\[ V_{inMIN} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]

\[ V_{inMAX} = V_{DD} - \max\{(|V_{EB3}| + |V_{T3}| - V_{T1}),(|V_{EB5}| + |V_{T5}| - V_{T2})\} \]
Parameter Inter-dependence

\[ A_O \approx \frac{g_{md}g_{mo}}{g_{oo}g_{od}} \]

\[ GB \approx \frac{g_{md}}{C_C} \]

\[ SR \approx \frac{I_T}{C_C} \]

\[ g_{md} \approx \frac{1}{2} \sqrt{\mu C_{OX}} \frac{W_1}{L_1} \sqrt{I_T} \]

\[ I_T \text{ affects} \]
A Set of Independent Design Parameters is Needed

Consider the Natural Reduced Parameter Set

\[
\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}
\]

\[\theta = \frac{I_{D6Q}}{I_T}\]

\[A_O \approx \frac{g_{md} g_{mo}}{g_{oo} g_{od}}\]

\[A_O = \frac{2 \sqrt{2} C_0 \times \sqrt{\mu_n \mu_p} \sqrt{\frac{W_1 W_5}{L_1 L_5}}}{\left(\lambda_n + \lambda_p\right)^2 I_T \sqrt{\frac{W_6 W_7}{W_7 L_6}}}\]
For a given pole $Q$ and a feedback factor $\beta$, it can be shown that:

$$G_B \equiv \frac{g_m d}{C_C} \sqrt{\frac{\mu_n C_{OX} W_1}{L_1}} \sqrt{I_T}$$

$$G_B = \frac{\sqrt{\mu_n \mu_p} \sqrt{\frac{W_1 W_5 W_6 L_7}{L_1 L_5 L_6 W_7}}}{C_C}$$

$$C_C = \frac{C_L \beta}{Q^2} \sqrt{\frac{2 \mu_p}{L_5 L_6 L_7}} - \beta \sqrt{\mu_n \frac{W_1}{L_1}}$$
\[ V_{\text{inMIN}} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]

\[ V_{\text{imin}} = V_{T1} + \sqrt{\frac{I_{\text{T}L1}}{\mu_n C_{\text{OX}} W_1}} + \sqrt{\frac{2I_{\text{T}L7}}{\mu_n C_{\text{OX}} W_7}} + V_{SS} \]

Expressions for signal swings are particularly complicated!
Observation

- Even the most elementary performance parameters require very complicated expressions when the natural design parameter space is used.

- Strong simultaneous dependence on multiple natural design parameters.

- Interdependence and notational complexity obscures insight into performance and optimization.
Practical Set of Design Parameters

\[ S_{\text{PRACTICAL}} = \{ P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7} \} \]

7 degrees of freedom!

- \( P \) : total power dissipation
- \( \theta = \frac{I_{DQ5}}{I_T} \), current split factor
- \( V_{EBK} = V_{GSQK} - V_{TK} \), excess bias voltage for the \( k \)’th transistor
- Phase margin constraint assumed (so \( C_C \) not shown in DoF)
Basic Two-Stage Op Amp

7 Degrees of Freedom

\{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\}

\begin{align*}
\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7} \right\},
I_T, \theta
\end{align*}
Relationship Between the Practical Parameters and the Natural Design Parameters

\[ \{P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7}\} \]

\[ \left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\} \]

\[ I_T \approx \frac{2I_{DQ_i}}{V_{DD} (1 + \theta)} \]

\[ \left( \frac{W}{L} \right)_i \approx \frac{2I_{DQ_i}}{\mu_i C_{OX} V_{EBi}^2} \]

\[ I_{DQ_i} \in \left\{ I_T, \frac{I_T}{2}, \theta I_T \right\} \]
Relationship Between the Practical Design Parameters and the Performance Parameters

\[ A_O = \frac{4}{(\lambda_n + \lambda_p)^2 V_{EB1} | V_{EB5}|} \]

\[ \text{GB} = \frac{P}{V_{DD} (1+\theta) V_{EB1} C_C} = \frac{P(2\theta V_{EB1} - \beta |V_{EB5}|)^2}{4C_L \theta \beta V_{DD} (1+\theta) V_{EB1}^2 |V_{EB5}|} \]

\[ \text{SR} = V_{EB1} \text{GB} = \frac{P(2\theta V_{EB1} - \beta |V_{EB5}|)^2}{4C_L \theta \beta V_{DD} (1+\theta) V_{EB1} |V_{EB5}|} \]

\[ C_C = 4C_L \theta \beta \frac{V_{EB1} |V_{EB5}|}{\left(2\theta V_{EB1} - \beta |V_{EB5}|\right)^2} \]
Relationship Between the Proposed Design Parameters and the Performance Parameters

\[ V_{OMAX} = V_{DD} - |V_{EB5}| \]

\[ V_{OMIN} = V_{SS} + V_{EB6} \]

\[ V_{inMIN} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]

\[ V_{inMAX} = V_{DD} - \max\{(|V_{EB3}| + |V_{T3} - V_{T1}|), (|V_{EB5}| + |V_{T5} - V_{T2}|)\} \]
Characteristics of the Practical Design Parameter Space

- Minimum set of independent parameters
- Results in major simplification of the key performance parameters
- Provides valuable insight which makes performance optimization more practical
Example for Design Procedure

Given specification:

- \( A_o: 66 \text{dB} \)
- \( G_B: 5 \text{MHz} \)
- \( V_{\text{omin}} = 0.25 \text{V} \)
- \( V_{\text{omax}} = 3.1 \text{V} \)
- \( V_{\text{imin}} = 1.1 \text{V} \)
- \( V_{\text{imax}} = 3 \text{V} \)
- \( P = 0.17 \text{mw} \)
- \( \beta = 1 \)

Assume: \( V_{\text{TN}} = 0.6, \ V_{\text{TP}} = -0.7, \ \lambda_n = 0.04, \ \lambda_p = 0.18 \)

7 constraints (in addition to \( \varphi_m \)) and 7 degrees of freedom
Design Assumptions

- Assume the following system parameters:
  \[ V_{DD} = 3.3 \text{ V} \]
  \[ C_L = 1 \text{ pF} \]
- Typical 0.35um CMOS process
- Simulation corner: typ/55°C/3.3V
Example for Design Procedure

1. Choose channel length

2. \( V_{EB3}, V_{EB5}, V_{EB6} \)
   \[
   \begin{align*}
   V_{imax} &= V_{DD} + V_{EB3} + V_{T1} + V_{T3} \\
   V_{omax} &= V_{DD} + V_{EB5} \\
   V_{omin} &= V_{EB6}
   \end{align*}
   \]

3. \( V_{EB1} \)
   \[
   A_O = \frac{4}{(\lambda_n + \lambda_p)^2 V_{EB1} | V_{EB5} |}
   \]

4. \( V_{EB7} \)
   \[
   V_{imin} = V_{EB1} + V_{EB7} + V_{T1}
   \]

5. Choose \( P \) to satisfy power constraint

\[
I \text{ } = \frac{P}{V_{DD} (1+\theta)}
\]
Example for Design Procedure

6. Choose $\theta$ to meet GB constraint

$$GB = \frac{P}{V_{DD}(1+\theta) V_{EB1} C_C}$$

7. Compensation capacitance $C_C$

$$C_C = 4 C_L \beta \frac{V_{EB1} | V_{EB5} |}{\left(2\theta V_{EB1} - \beta | V_{EB5} | \right)^2}$$

8. Calculate all transistor sizes

$$I_T = \frac{P}{V_{DD}(1+\theta)}$$

$$\frac{W_k}{L_k} = \frac{2I_{DK}}{\mu_k C_{OX} V_{EBk}^2}$$

9. Implement structure, simulate, and make modifications if necessary guided by where deviations may occur.

Note: It may be necessary or preferable to make some constraints an inequality.

Note: Specifications may be over-constrained or have no solution.
Example for Design Procedure

Simulation result:

<table>
<thead>
<tr>
<th></th>
<th>(W/L)_{1,2}</th>
<th>(W/L)_{3,4}</th>
<th>(W/L)_{5}</th>
<th>\phi_{phase}</th>
<th>\theta</th>
<th>\text{Ao}</th>
</tr>
</thead>
<tbody>
<tr>
<td>(W/L)_{6,7}</td>
<td>13/2</td>
<td>24.5/2</td>
<td>54/2</td>
<td>45.4deg.</td>
<td></td>
<td>65dB</td>
</tr>
<tr>
<td>I_{ss}</td>
<td>17.4/2</td>
<td>C_C</td>
<td>3.7pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_5</td>
<td>25uA</td>
<td>26.68uA</td>
<td></td>
<td></td>
<td>1.06</td>
<td></td>
</tr>
<tr>
<td>GB</td>
<td>5.2MHz</td>
<td>P</td>
<td>0.17mw</td>
<td>V_{EB7}</td>
<td>0.2</td>
<td></td>
</tr>
<tr>
<td>Ao</td>
<td></td>
<td></td>
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</tbody>
</table>
### Settling Characteristics of Two-Stage Operational Amplifier

#### Process Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>uCoxn</td>
<td>9E-05</td>
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<tr>
<td>uCoxp</td>
<td>5E-05</td>
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<tr>
<td>Vtn</td>
<td>0.768</td>
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<tr>
<td>Vtp</td>
<td>0.774</td>
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#### Performance Characteristics

<table>
<thead>
<tr>
<th>Device Sizing</th>
<th>W/L1</th>
<th>W/L2</th>
<th>W/L5</th>
<th>W/L6</th>
<th>W/L7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>148.1</td>
<td>148.1</td>
<td>289.9</td>
<td>579.7</td>
<td></td>
</tr>
</tbody>
</table>

#### Design Parameters

<table>
<thead>
<tr>
<th>VEB1</th>
<th>VEB2</th>
<th>VEB5</th>
<th>VEB6</th>
<th>VEB7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>0.5</td>
<td>0.25</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>1</td>
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<td>0.25</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0.5</td>
<td>0.25</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>0.5</td>
<td>1</td>
<td>0.25</td>
<td>0.25</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0.25</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0.25</td>
<td>0.25</td>
<td></td>
</tr>
</tbody>
</table>

#### Input Range | Output Range

<table>
<thead>
<tr>
<th>Vmax</th>
<th>Vmin</th>
<th>Vmax</th>
<th>Vmin</th>
<th>W/L1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.52</td>
<td>4.27</td>
<td>0.25</td>
<td>3.5</td>
<td>72.5</td>
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<td>2.02</td>
<td>4.27</td>
<td>0.25</td>
<td>3.5</td>
<td>18.1</td>
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<td>3.02</td>
<td>3.77</td>
<td>0.25</td>
<td>3.5</td>
<td>4.5</td>
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<tr>
<td>1.52</td>
<td>3.77</td>
<td>0.25</td>
<td>3.5</td>
<td>72.5</td>
</tr>
<tr>
<td>2.02</td>
<td>2.77</td>
<td>0.25</td>
<td>3.5</td>
<td>18.1</td>
</tr>
<tr>
<td>3.02</td>
<td>2.77</td>
<td>0.25</td>
<td>3.5</td>
<td>4.5</td>
</tr>
</tbody>
</table>

#### V/I Characteristics

<table>
<thead>
<tr>
<th>Ao</th>
<th>GB</th>
<th>ISS(mA)</th>
<th>CC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>8.3E+08</td>
<td>1.67</td>
<td>4E-12</td>
</tr>
<tr>
<td>556</td>
<td>1.9E+09</td>
<td>1.67</td>
<td>8.9E-13</td>
</tr>
<tr>
<td>278</td>
<td>2.6E+09</td>
<td>1.67</td>
<td>3.3E-13</td>
</tr>
<tr>
<td>1111</td>
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</tbody>
</table>
Summary

1. Determination of Design Space and Degrees of Freedom Often Useful for Understanding the Design Problem

2. Analytical Expressions for Key Performance Parameters give Considerable Insight Into Design Potential

3. Natural Design Parameters Often Not Most Useful for Providing Insight or Facilitating Optimization

4. Concepts Readily Extend to other Widely Used Structures
Basic Two-Stage Op Amp

\[ A_{FB}(s) \approx \frac{g_{md}(g_{m0} - sC_{c})}{s^2C_{c}C_{L} + sC_{C}(g_{mo} - \beta g_{md}) + \beta g_{md}g_{mo}} \]

Right Half-Plane Zero Limits Performance

Why does the RHP zero limit performance?
Can anything be done about this problem?
Why does the RHP zero limit performance?

In this example:

- accumulate phase shift and slow gain drop with RHP zeros
- effects are dramatic

\[ p_1 = 1, \quad p_2 = 1000, \quad z_\infty = \{\text{none,250}\} \]
Why does the RHP zero limit performance?

- Accumulate phase shift and slow gain drop with RHP zeros
- Lose phase shift and slow gain drop with RHP zeros
- Effects are dramatic

In this example:
- \( p_1 = 1, p_2 = 1000, z_x = \{ \text{none, 250, -250} \} \)
End of Lecture 18