Two-Stage Op Amp with LHP Zero
Basic Two-Stage Op Amp

\[
A_{FB}(s) \approx \frac{g_{md}(g_{m0} - sC_C)}{s^2C_CC_L + sC_C(g_{m0} - \beta g_{md}) + \beta g_{md}g_{m0}}
\]

It can be shown that

\[
Q = \sqrt{\frac{C_L}{C_C}} \sqrt{\beta} \frac{\sqrt{g_{m0}g_{md}}}{g_{m0} - \beta g_{md}}
\]

\[
C_C = \frac{C_L\beta}{Q^2} \frac{g_{m0}g_{md}}{(g_{m0} - \beta g_{md})^2}
\]

where \( g_{md} = g_{m1} \)  \( g_{m0} = g_{m5} \)

\( g_{oo} = g_{o5} + g_{o6} \) and \( g_{od} = g_{o2} + g_{o4} \)

But what pole Q is desired?  \(.707 < Q < 0.5\)

Right Half-Plane Zero in OL Gain Limits Performance
Nyquist and Gain-Phase Plots convey identical information but gain-phase plots often easier to work with.

Note: The two plots do not correspond to the same system in this slide.
Review from last lecture

Gain and Phase Margin Examples

\[ T(s) = \frac{1581}{(s + 1)^2(s + 20)} \]
Relationship between pole $Q$ and phase margin

In general, the relationship between the phase margin and the pole $Q$ is dependent upon the order of the transfer function and on the location of the zeros.

In the special case that the open loop amplifier is second-order low-pass, a closed form analytical relationship between pole $Q$ and phase margin exists and this is independent of $A_0$ and $\beta$.

$$Q = \frac{\sqrt{\cos(\varphi_M)}}{\sin(\varphi_M)}$$

$$\varphi_M = \cos^{-1}\left(\sqrt{1 + \frac{1}{4Q^4}} - \frac{1}{2Q^2}\right)$$

The region of interest is invariable only for $0.5 < Q < 0.7$ larger $Q$ introduces unacceptable ringing and settling smaller $Q$ slows the amplifier down too much.
Review from last lecture

Phase Margin vs Q

Second-order low-pass Amplifier
Review from last lecture

Phase Margin vs Q

Second-order low-pass Amplifier

Phase Margin vs Q

0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
40 50 60 70 80

Phase Margin

Pole Q
Review from last lecture

Magnitude Response of 2nd-order Lowpass Function

\[ Q_{\text{MAX}} \text{ for no peaking } = \frac{1}{\sqrt{2}} = .707 \]

\[ \zeta = \frac{1}{2Q} \]

From Laker-Sansen Text
Step Response of 2\textsuperscript{nd}-order Lowpass Function

\[ Q_\text{MAX} \text{ for no overshoot } = \frac{1}{2} \]

\[ \zeta = \frac{1}{2Q} \]

Review from last lecture

From Laker-Sansen Text
Review from last lecture

Compensation Summary

• Gain and phase margin performance often strongly dependent upon architecture
• Relationship between overshoot and ringing and phase margin were developed only for 2\textsuperscript{nd} -order lowpass gain characteristics and differ dramatically for higher-order structures
• Absolute gain and phase margin criteria are not robust to changes in architecture or order
• It is often difficult to correctly “break the loop” to determine the loop gain $A_{\beta}$ with the correct loading on the loop (will discuss this more later)
Design of Two-Stage Op Amps

- Compensation is critical in two-stage op amps

- General approach to designing two-stage op amps is common even though significant differences in performance for different architectures

- Will consider initially the most basic two-stage op amp with internal compensation
Natural Parameter Space for the Two-Stage Amplifier Design

\[ S_{\text{NATURAL}} = \{ W_1, L_1, W_3, L_3, W_5, L_5, W_6, L_6, W_7, L_7, I_T, I_{D6}, C_c \} \]
Design Degrees of Freedom

Total independent variables: 13

Degrees of Freedom: 13

If phase margin is considered a constraint

13 independent variables
1 constraint

12 degrees of freedom
Observation:
W,L appear as W/L ratio in almost all characterizing equations

Implication:
Degrees of Freedom are Reduced

\[ S_{\text{NATURAL-REDUCED}} = \{(W/L)_1, (W/L)_3, (W/L)_5, (W/L)_6, (W/L)_7, I_{D6}, I_T, C_C\} \]

With phase margin constraint,

Degrees of freedom: 7
## Common Performance Parameters of Operational Amplifiers

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ao</td>
<td>Open-loop DC Gain</td>
</tr>
<tr>
<td>GB</td>
<td>Gain-Bandwidth Product</td>
</tr>
<tr>
<td>Φm(or Q)</td>
<td>Phase Margin (or pole Q)</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
</tr>
<tr>
<td>T_{SETTLE}</td>
<td>Settling Time</td>
</tr>
<tr>
<td>A_T</td>
<td>Total Area</td>
</tr>
<tr>
<td>A_A</td>
<td>Total Active Area</td>
</tr>
<tr>
<td>P</td>
<td>Power Dissipation</td>
</tr>
<tr>
<td>σ_{VOS}</td>
<td>Standard Deviation of Input Referred Offset Voltage (often termed the input offset voltage)</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
</tr>
<tr>
<td>Vimax</td>
<td>Maximum Common Mode Input Voltage</td>
</tr>
<tr>
<td>Vimin</td>
<td>Minimum Common Mode Output Voltage</td>
</tr>
<tr>
<td>Vomax</td>
<td>Maximum Output Voltage Swing</td>
</tr>
<tr>
<td>Vomin</td>
<td>Minimum Output Voltage Swing</td>
</tr>
<tr>
<td>Vnoise</td>
<td>Input Referred RMS Noise Voltage</td>
</tr>
<tr>
<td>Sv</td>
<td>Input Referred Noise Spectral Density</td>
</tr>
</tbody>
</table>
Performance Parameters

Total: 17
Performance parameters: 17

Degrees of freedom: 7

System is Generally Highly Over Constrained!
Typical Parameter Space for a Two-Stage Amplifier

Small signal model of the two-stage operational amplifier

Small signal design parameters:

\[ S_{\text{SMALL SIGNAL}} = \{g_{oo}, g_{od}, g_{mo}, g_{md}, C_C, g_{o2}, g_{o4}, g_{o5}, g_{o6}\} \]
Signal Swing of Two-Stage Op Amp

\( M6: \quad V_{OUT} > V_{SS} + V_{EB6} \)

\( M5: \quad V_{OUT} < V_{DD} - |V_{EB5}| \)

\( M1: \quad V_{iC} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}| \)

\( M2: \quad V_{iC} < V_{DD} + V_{T1} - |V_{T5}| - |V_{EB5}| \)

\( M7: \quad V_{iC} > V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \)

\( S_{\text{swing/Bias Related}} = \{ C_C, V_{EB1Q}, V_{EB3Q}, V_{EB5Q}, V_{EB6Q}, V_{EB7Q}, I_T \} \)
Signal Swing of Two-Stage Op Amp

\[ V_{\text{OUT}} < V_{\text{DD}} - |V_{\text{EB}5}| \]

\[ V_{\text{OUT}} > V_{\text{SS}} + V_{\text{EB}6} \]

\[ V_{\text{ic}} > V_{T1} + V_{\text{EB}1} + V_{\text{EB}7} + V_{\text{SS}} \]

\[ V_{\text{ic}} < V_{\text{DD}} + V_{T1} - |V_{T3}| - |V_{\text{EB}3}| \]

\[ V_{\text{ic}} < V_{\text{DD}} + V_{T1} - |V_{T5}| - |V_{\text{EB}5}| \]
Signal Swing of Two-Stage Op Amp

\[ V_{OUT} \]

\[ V_{DD} \]

\[ |V_{EB5}| \]

\[ V_{SS} \]

\[ V_{EB6} \]

\[ V_{SS} \]

\[ V_{T1} + V_{EB1} + V_{EB7} \]

\[ \max\{(|V_{EB5}| + |V_{T3} - V_{T1}|, (|V_{EB5}| + |V_{T5} - V_{T2}|) \} \]
Augmented set of design parameters:

\[ S_{\text{AUGMENTED}} = \{ g_{oo}, g_{od}, g_{mo}, g_{md}, C_C, V_{EB1Q}, V_{EB3Q}, V_{EB5Q}, V_{EB6Q}, V_{EB7Q}, I_T, g_{o2}, g_{o4}, g_{o5}, g_{o6} \} \]

Parameters in this set are highly inter-related
Common Expressions for the Performance Parameters

$$A_O \approx \frac{g_{md}g_{mo}}{g_{oo}g_{od}}$$

$$GB \approx \frac{g_{md}}{C_C}$$

$$SR \approx \frac{l_T}{C_C}$$
Common Expressions for the Performance Parameters (cont)

\[ V_{\text{OMAX}} = V_{\text{DD}} - |V_{\text{EB5}}| \]
\[ V_{\text{OMIN}} = V_{\text{SS}} + V_{\text{EB6}} \]
\[ V_{\text{inMIN}} = V_{T1} + V_{\text{EB1}} + V_{\text{EB7}} + V_{\text{SS}} \]
\[ V_{\text{inMAX}} = V_{\text{DD}} - \max\{(|V_{\text{EB3}}| + |V_{T3}| - V_{T1}), (|V_{\text{EB5}}| + |V_{T5}| - V_{T2})\} \]
Parameter Inter-dependence

\[ A_0 \cong \frac{g_{md}g_{mo}}{g_{oo}g_{od}} \]

\[ GB \cong \frac{g_{md}}{C_C} \]

\[ SR \cong \frac{l_T}{C_C} \]

\[ g_{md} \cong \frac{1}{2} \sqrt{\mu \text{COX} \frac{W_1}{L_1}} \sqrt{l_T} \]

I_T affects
A Set of Independent Design Parameters is Needed

Consider the Natural Reduced Parameter Set

\[
\begin{align*}
\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}
\end{align*}
\]

\[
\theta = \frac{I_{D6Q}}{I_{Tot}} = \frac{P_2}{P}
\]

\[
I_{Tot} = I_T + I_{D6Q}
\]

\[
A_O \approx \frac{g_{md} g_{mo}}{g_{oo} g_{od}}
\]

\[
A_O = \frac{2 \sqrt{2} C_{OX} \sqrt{\mu_n \mu_p}}{\left( \lambda_n + \lambda_p \right)^2 I_T} \sqrt[3]{\frac{W_1 W_5}{L_1 L_5}} \sqrt[3]{\frac{W_6 L_7}{W_7 L_6}}
\]
\[ GB \approx \frac{g_{md}}{C_C} \]
\[ GB = \sqrt{\frac{\mu_n C_{OX} W_1}{L_1}} \sqrt{I_T} \]

For a given pole \( Q \) and a feedback factor \( \beta \), it can be shown that:

\[ C_C = \frac{C_L \beta}{Q^2} \frac{\sqrt{\mu_n \mu_p} \sqrt{2 \frac{W_1 W_5 W_6 L_7}{L_1 L_5 L_6 W_7}}}{\left( \sqrt{2 \mu_p \frac{W_5 W_6 W_7}{L_5 L_6 L_7}} - \beta \sqrt{\mu_n \frac{W_1}{L_1}} \right)^2} \]
\[ V_{\text{inMIN}} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]

\[ V_{\text{imin}} = V_{T1} + \sqrt{\frac{I_{TL1}}{\mu_n C_{OX} W_1}} + \sqrt{\frac{2I_{TL7}}{\mu_n C_{OX} W_7}} + V_{SS} \]

Expressions for signal swings are particularly complicated!
Observation

- Even the most elementary performance parameters require very complicated expressions when the natural design parameter space is used.

- Strong simultaneous dependence on multiple natural design parameters.

- Interdependence and notational complexity obscures insight into performance and optimization.
Practical Set of Design Parameters

\[ S_{\text{PRACTICAL}} = \{P, \theta, V_{\text{EB1}}, V_{\text{EB3}}, V_{\text{EB5}}, V_{\text{EB6}}, V_{\text{EB7}} \} \]

7 degrees of freedom!

- \( P \) : total power dissipation
- \( \theta \) = fraction of total power in second stage
- \( V_{\text{EBk}} \) = excess bias voltage for the \( k^{th} \) transistor
- Phase margin constraint assumed (so \( C_C \) not shown in DoF)
Basic Two-Stage Op Amp

7 Degrees of Freedom

\{ P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7} \}

\begin{align*}
\left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\}
\end{align*}
Relationship Between the Practical Parameters and the Natural Design Parameters

\[ \left\{ P, \theta, V_{EB1}, V_{EB3}, V_{EB5}, V_{EB6}, V_{EB7} \right\} \]

\[ \left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, \frac{W_6}{L_6}, \frac{W_7}{L_7}, I_T, \theta \right\} \]

\[ I_T = \frac{P(1-\theta)}{V_{DD}} \]

\[ I_{DQi} \in \left\{ I_T, \frac{I_T}{2}, \frac{\theta P}{V_{DD}} \right\} \]

\[ \left( \frac{W}{L} \right)_i \approx \frac{2I_{DQi}}{\mu_i C_{OX} V_{EBi}^2} \]
Relationship Between the Practical Design Parameters and the Performance Parameters

(Assuming \( Q = \frac{1}{\sqrt{2}} \))

\[
A_0 = \frac{4}{(\lambda_n + \lambda_p)^2 V_{EB1} | V_{EB5} |}
\]

\[
GB = \frac{P(1-\theta)}{V_{DD} V_{EB1}} = \frac{PQ^2 (2\theta V_{EB1} - \beta (1-\theta) V_{EB5})^2}{C_L \beta 2\theta V_{EB1}^2 V_{EB5} V_{DD}}
\]

\[
SR = \frac{PQ^2 (2\theta V_{EB1} - \beta (1-\theta) V_{EB5})^2}{C_L \beta 2\theta V_{EB1} V_{EB5} V_{DD}}
\]

\[
C_C = \frac{C_L 2\theta (1-\theta) \beta}{Q^2} \frac{V_{EB1} V_{EB5}}{(V_{EB1} 2\theta - \beta V_{EB5} (1-\theta))^2}
\]
Relationship Between the Proposed Design Parameters and the Performance Parameters

\[ V_{O_{MAX}} = V_{DD} - |V_{EB5}| \]
\[ V_{O_{MIN}} = V_{SS} + V_{EB6} \]
\[ V_{in_{MIN}} = V_{T1} + V_{EB1} + V_{EB7} + V_{SS} \]
\[ V_{in_{MAX}} = V_{DD} - \max\{(|V_{EB3}| + |V_{T3}| - V_{T1}), (|V_{EB5}| + |V_{T5}| - V_{T2})\} \]
Characteristics of the Practical Design Parameter Space

- Minimum set of independent parameters
- Results in major simplification of the key performance parameters
- Provides valuable insight which makes performance optimization more practical
Design Assumptions

- Assume the following system parameters:
  \[ V_{DD} = 3.3 \, \text{V} \]
  \[ C_L = 1 \, \text{pF} \]
- Typical 0.35um CMOS process
- Simulation corner: typ/55°C/3.3V
Given specifications:

A_0: 66dB  
GB: 5MHz  
V_{\text{OMIN}}=0.25V  
V_{\text{OMAX}}=3.1V  
V_{\text{INMIN}}=1.1V  
V_{\text{INMAX}}=3V  
P=0.17mw  
\beta=1

Assume: V_{TN} = 0.6, V_{TP}= -0.7, \lambda_n=0.04, \lambda_p=0.18

7 constraints (in addition to \varphi_m) and 7 degrees of freedom
Example for Design Procedure

1. Choose channel length
2. $V_{EB3}, V_{EB5}, V_{EB6}$
   
   $V_{imax} = V_{DD} + V_{EB3} + V_{T1} + V_{T3}$
   $V_{omax} = V_{DD} + V_{EB5}$
   $V_{omin} = V_{EB6}$

3. $V_{EB1}$

   
   $A_O = \frac{4}{\left(\lambda_n + \lambda_p\right)^2 V_{EB1} V_{EB5}}$

4. $V_{EB7}$

   
   $V_{imin} = V_{EB1} + V_{EB7} + V_{T1}$

5. Choose $P$ to satisfy power constraint

   
   $I_T = \frac{P(1-\theta)}{V_{DD}}$

   (note this step could have occurred earlier since $P$ is one of the design variables)
Example for Design Procedure

6. Choose $\theta$ to meet GB constraint
   
   \[
   GB = \frac{P(1-\theta)}{V_{DD}V_{EB1}C_C}
   \]
   
   (the expression for GB really contains only one unknown at this stage, $\theta$, though expression is not explicit since $\theta$ also appears in $C_C$)

7. Compensation capacitance $C_C$
   
   \[
   C_C = \frac{C_L\beta}{Q^2} \cdot 2\theta(1-\theta) \cdot \frac{V_{EB1} V_{EB5}}{(V_{EB1} 2\theta - \beta V_{EB5} (1-\theta))^2}
   \]
   
   (Assuming $Q = \frac{1}{\sqrt{2}}$)

8. Calculate all transistor sizes
   
   \[
   I_T = \frac{P(1-\theta)}{V_{DD}} \quad I_{5Q} = \frac{P\theta}{V_{DD}} \quad \frac{W_k}{L_k} = \frac{2I_{Dk}}{\mu_k C_{OX} V_{EBk}^2}
   \]

9. Implement structure, simulate, and make modifications if necessary guided by where deviations may occur

Note: It may be necessary or preferable to make some constraints an inequality
Note: Specifications may be over-constrained or have no solution
Example for Design Procedure

Summary of Design Procedure for This Set of Specifications:

1. Choose channel length
2. Select: $V_{EB3}$, $V_{EB5}$, $V_{EB6}$
3. Select: $V_{EB1}$
4. Select: $V_{EB7}$
5. Choose $P$ to satisfy power constraint
6. Choose $\theta$ to meet GB constraint
7. Compensation capacitance $C_C$
8. Calculate all transistor sizes
9. Implement structure, simulate, and make modifications if necessary guided by where deviations may occur

Note: Though not shown, this design procedure was based upon looking at the set of equations that must be solved and developing a sequence to solve these equations. It may not always be the case that equations can be solved sequentially.

Note: Different specification requirements (constraints) will generally require a different design procedure.
Example for Design Procedure

Design results (with L=2µm):

<table>
<thead>
<tr>
<th>M_{1,2} W/L</th>
<th>M_{3,4} W/L</th>
<th>M_5 W/L</th>
<th>M_6 W/L</th>
<th>M_7 W/L</th>
<th>P</th>
<th>θ</th>
<th>C_C</th>
</tr>
</thead>
<tbody>
<tr>
<td>13/2</td>
<td>24.5/2</td>
<td>54/2</td>
<td>17.4/2</td>
<td>17.4/2</td>
<td>0.17mW</td>
<td>.51</td>
<td>3.7pF</td>
</tr>
</tbody>
</table>

Simulation results:

<table>
<thead>
<tr>
<th>A0</th>
<th>GB</th>
<th>P</th>
<th>Phase margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>65dB</td>
<td>5.2MHz</td>
<td>.17mW</td>
<td>45.4 degrees</td>
</tr>
</tbody>
</table>
## Spreadsheet for Design Space Exploration

### Settling Characteristics of Two-Stage Operational Amplifier

<table>
<thead>
<tr>
<th>Process Parameters</th>
<th>Settling Characteristics</th>
<th>Input Range</th>
<th>Output Range</th>
<th>Device Sizing</th>
</tr>
</thead>
<tbody>
<tr>
<td>uCoxn 9E-05</td>
<td>ln 0.02</td>
<td>Power 0.01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>uCoxp 5E-05</td>
<td>lp 0.1</td>
<td>CT 1E-12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vtn 0.768</td>
<td>Vdd 4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vtp 0.774</td>
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<td></td>
<td></td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>VEB1</th>
<th>Design Parameters</th>
<th>Performance Characteristics</th>
<th>Input Range</th>
<th>Output Range</th>
<th>Device Sizing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VEB2 VEB5 VEB6 VEB7</td>
<td>n Ao GB ISS(mA) CC</td>
<td>Vmin Vmax</td>
<td>Vmir Vmax</td>
<td>W/L1 W/L2 W/L5 W/L6 W/L7</td>
</tr>
<tr>
<td>0.5</td>
<td>0.5 0.5 0.25 0.25</td>
<td>0.5 1111 8.3E+08 1.67 4E-12</td>
<td>1.52 4.27 0.25 3.5 72.5 148.1</td>
<td>148.1 289.9 579.7</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0.5 0.5 0.25 0.25</td>
<td>0.5 556 1.9E+09 1.67 8.9E-13</td>
<td>2.02 4.27 0.25 3.5 18.1 148.1</td>
<td>148.1 289.9 579.7</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1 0.5 0.25 0.25</td>
<td>0.5 278 2.6E+09 1.67 3.3E-13</td>
<td>3.02 3.77 0.25 3.5 4.5 37.0</td>
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<td>3.02 3.77 0.25 3.5 4.5 37.0</td>
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<td>0.5 2 0.25 0.25</td>
<td>0.5 278 8.3E+08 1.67 4E-12</td>
<td>1.52 4.27 0.25 2 72.5 148.1</td>
<td>9.3 289.9 579.7</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0.5 2 0.25 0.25</td>
<td>0.5 139 ERR 1.67 ERR</td>
<td>2.02 4.27 0.25 2 18.1 148.1</td>
<td>9.3 289.9 579.7</td>
<td></td>
</tr>
</tbody>
</table>
Summary

1. Determination of Design Space and Degrees of Freedom Often Useful for Understanding the Design Problem

2. Analytical Expressions for Key Performance Parameters give Considerable Insight Into Design Potential

3. Natural Design Parameters Often Not Most Useful for Providing Insight or Facilitating Optimization

4. Concepts Readily Extend to other Widely Used Structures
Power distribution between stages

How should the power be split between the two stages?

- Would often like to minimize power for a given speed (GB) requirement
- Optimal split may depend upon architecture
Power distribution between stages

How should the power be split between the two stages?

Consider basic two-stage with first-stage compensation

Assume $p_2 = 3\beta A_0 p_1$

Thus

$$GB = \frac{g_{m1}}{g_{01} + g_{03}} \frac{g_{m5}}{g_{05} + g_{06}} \frac{g_{01} + g_{03}}{C_C} = \frac{g_{m1} g_{m5}}{(g_{05} + g_{06}) C_C}$$
Power distribution between stages

How should the power be split between the two stages?

\[ V_{IN} \quad F_1 \quad P_1 \quad V_{OUT} \quad F_2 \quad P_2 \quad VDD \]

Since \[ p_2 = 3 \beta A_0 p_1 \]

\[
\begin{align*}
A_{10} &= \frac{-g_{m1}}{g_{01} + g_{03}} \\
A_{20} &= \frac{-g_{m5}}{g_{05} + g_{06}} \\
p_1 &= \frac{g_{01} + g_{03}}{C_C} \\
p_2 &= \frac{g_{05} + g_{06}}{C_L}
\end{align*}
\]

Since \[ GB = \frac{g_{m1}g_{m5}}{(g_{05} + g_{06})C_C} \]

\[ GB = \frac{g_{05} + g_{06}}{3 \beta C_L} \]

Finally \[ GB = \frac{(\lambda_p + \lambda_n) \theta P}{V_{DD} 3 \beta C_L} \]

Thus for given GB, for this structure want \( \theta \) as close to 1 as is practical.
Power distribution between stages

Note: Optimum power split for previous example was for dominant pole compensation in first stage. Results may be different for Miller compensation or for output compensation.

For first-stage compensation capacitor with compensation criteria: \( p_2 = 3\beta A_0 p_1 \):

\[
GB = \frac{(\lambda_p + \lambda_n) \theta P}{V_{DD} 3\beta C_L}
\]

For Miller Compensation with RHP zero and arbitrary Q compensation criteria:

\[
GB = \frac{P(1-\theta)}{V_{DD} V_{EB1} C_C} = \frac{PQ^2 (2\theta V_{EB1} - \beta (1-\theta) V_{EB5})^2}{C_L \beta 2\theta V_{EB1}^2 V_{EB5} V_{DD}}
\]
End of Lecture 18