EE 435

Lecture 22

Data Converters
Basic Operation of CMFB Block

$V_{O1}$
$V_{O2}$
$
\begin{array}{c}
\text{CMFB Circuit} \\
\hline
V_{FB}
\end{array}$

$V_{OXX}$

Averager

$\text{CMFB Block}$

$V_{O1}$
$V_{O2}$

$V_{AVG}$

$A$

$V_{FB}$

$V_{FB} = \left( \frac{V_{O1} + V_{O2}}{2} \right) A(s)$

$V_{OXX}$ is the desired quiescent voltage at the stabilization node (irrespective of where $V_{FB}$ goes)

Review from last lecture
Definition: The common-mode offset voltage is the voltage that must be applied to the biasing node at the CMFB point to obtain the desired operating point at the stabilization node.
Common-mode gains

\[ A_{\text{COM0}} = - \frac{g_{01} + g_{03}/2}{g_{05}} = - \frac{\lambda I_T}{\lambda I_T/2} = - \frac{1}{2} \]

\[ A_{\text{COM20}} = - \frac{g_{m5}}{g_{05}} = - \frac{2I_T/V_{EB5}}{\lambda I_T/2} = - \frac{4}{V_{EB5} \lambda} \]

\[ A_{\text{COM30}} = - \frac{g_{m3}/2}{g_{05}} = - \frac{V_{EB3}}{\lambda I_T/2} = \frac{2}{\lambda V_{EB3}} \]

Although the common-mode gain \( A_{\text{COM0}} \) is very small, \( A_{\text{COM20}} \) is very large!

Shift in \( V_{02Q} \) from \( V_{OXX} \) is the product of the common-mode offset voltage and \( A_{\text{COM20}} \).
How much gain is needed in the CMFB amplifier?

This does not require a particularly large gain:

- This is the loop that must be compensated since $A$ and $A_{\text{COMP2}}$ will be frequency dependent.
- Miller compensation capacitor for compensation of differential loop will often appear in shunt with $C_2$.
- Can create this loop without CM inputs on fully differential structure for simulations.
- Results extend readily to two-stage structures with no big surprises.

$$\Delta V_{\text{OUT-ACCEPTABLE}} = V_{\text{COFF}} \frac{A_{\text{COM2}}}{1 - AA_{\text{COM2}}}$$
CMFB Circuits

Several (but not too many) CMFB circuits exist
Can be classified as either continuous-time or discrete-time

Review from last lecture
Data Converters

Types:

A/D (Analog to Digital)

Converts Analog Input to a Digital Output

D/A (Digital to Analog)

Converts a Digital Input to an Analog Output

A/D is the world’s most widely used mixed-signal component

D/A is often included in a FB path of an A/D

A/D and D/A fields will remain hot indefinitely

technology advances make data converter design more challenging

embedded applications
designs often very application dependent
D/A Converters

Basic structure:

\[ \vec{X}_{IN} \rightarrow DAC \rightarrow \vec{X}_{OUT} \]

\[ \vec{X}_{REF} \]

Basic structure with differential outputs:

\[ \vec{X}_{IN} \rightarrow DAC \rightarrow \vec{X}^{+}_{OUT}, \vec{X}^{-}_{OUT} \]

\[ \vec{X}^{+}_{REF}, \vec{X}^{-}_{REF} \]
D/A Converters

Notation:
D/A Converters

\[ \tilde{X}_{\text{IN}} = \langle b_{n-1}, b_{n-1}, \ldots, b_1, b_0 \rangle \]

- \( b_0 \) is the Least Significant Bit (LSB)
- \( b_{n-1} \) is the Most Significant Bit (MSB)

Note: some authors use different index notation

An Ideal DAC is characterized at low frequencies by its static performance
D/A Converters

\[ \bar{X}_{IN} = \langle b_{n-1}, b_{n-1}, \ldots, b_1, b_0 \rangle \]

An Ideal DAC transfer characteristic (3-bits)

Code \( C_k \) is used to represent the decimal equivalent of the binary number \( \langle b_{n-1} \ldots b_0 \rangle \)
D/A Converters

\( \vec{X}_{\text{IN}} = <b_{n-1}, b_{n-1}, \ldots, b_1, b_0> \)

An Ideal DAC transfer characteristic (3-bits)
D/A Converters

$\hat{X}_{IN} = \langle b_{n-1}, b_{n-1}, \ldots b_1, b_0 \rangle$

An ideal DAC transfer characteristic (3-bits)

All points of this ideal DAC lie on a straight line
D/A Converters

- Most D/A ideally have a linear relationship between binary input and analog output
- Output represents a discrete set of continuous variables
- Typically this number is an integral power of 2, i.e. $2^n$
- $X_{IN}$ is always dimensionless

- $X_{OUT}$ could have many different dimensions
- An ideal nonlinear characteristic is also possible (waveform generation and companding)
- Will assume a linear transfer characteristic is desired unless specifically stated to the contrary
For this ideal DAC

$$x_{\text{OUT}} = x_{\text{REF}} \left( \frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \frac{b_{n-3}}{8} + \ldots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n} \right)$$

$$x_{\text{OUT}} = x_{\text{REF}} \sum_{j=1}^{n} \frac{b_{n-j}}{2^j}$$

- Number of outputs gets very large for \( n \) large
- Spacing between outputs is \( X_{\text{REF}}/2^n \) and gets very small for \( n \) large
D/A Converters

- Ideal steps all equal and termed the LSB
- \( X_{LSB} \) gets very small for small \( X_{REF} \) and large \( n \)

**Example**: If \( X_{REF}=1V \) and \( n=16 \), then \( N=2^{16}=65,536 \), \( X_{LSB}=15.25\mu V \)
D/A Converters

An alternate ideal 3-bit DAC

Irrespective of which form is considered, the increment in the output for one Boolean bit change in the input is $\Delta x_{\text{LSB}}$ and the total range is 1LSB less than $x_{\text{REF}}$. 
Applications of DACs

- Waveform Generation
- Voltage Generation
- Analog Trim or Calibration
- Industrial Control Systems
- Feedback Element in ADCs
- ....
Waveform Generation with DACs

Ramp (Saw-tooth) Generator

Example: For $n=3$

Example: For large $n$

Ramp (Saw-tooth) Generator
Waveform Generation with DACs

Sine Wave Generator

Distortion of the desired waveforms occurs due to both time and amplitude quantization

Often a filter precedes or follows the buffer amplifier to smooth the output waveform
A/D Converters

Basic structure:

\[ x_{IN} \rightarrow \text{ADC} \rightarrow x_{OUT} \]

Input range is \( x_{REF} \)

Basic structure with differential inputs/references:

\[ x_{IN} \rightarrow \text{ADC} \rightarrow x_{OUT} \]

Input range is \( x^+_{REF} - x^-_{REF} \)

\[ x^+_{IN} \rightarrow \text{ADC} \rightarrow x^-_{OUT} \]

Input range is \( 2(x^+_{REF} - x^-_{REF}) \)
A/D Converters

Notation:
A/D Converters

\[ \vec{X}_{OUT} = \langle d_{n-1}, d_{n-2}, \ldots, d_0 \rangle \]

- \( d_0 \) is the Least Significant Bit (LSB)
- \( d_{n-1} \) is the Most Significant Bit (MSB)

Note: some authors use different index notation

An Ideal ADC is characterized at low frequencies by its static performance
A/D Converters

An Ideal ADC transfer characteristic (3-bits)

\[ \bar{X}_{\text{OUT}} = \langle d_{n-1}, d_{n-2}, \ldots, d_0 \rangle \]

\[ X_{\text{LSB}} = \frac{X_{\text{REF}}}{2^n} \]

\[ X_{\text{REF}} - X_{\text{LSB}} \]
A/D Converters

An Ideal ADC transfer characteristic (3-bits)

$\tilde{X}_{OUT} = \langle d_{n-1}, d_{n-2}, ..., d_0 \rangle$

$x_{LSB} = \frac{x_{REF}}{2^n}$

The second vertical axis, labeled $\tilde{X}_{OUT}$, is the interpreted value of $\tilde{X}_{OUT}$.
A/D Converters

For this ideal ADC

\[ X_{\text{REF}} \left( \frac{d_{n-1}}{2} + \frac{d_{n-2}}{4} + \frac{d_{n-3}}{8} + \ldots + \frac{d_1}{2^{n-1}} + \frac{d_0}{2^n} \right) = X_{\text{IN}} + \varepsilon \]

where \( \varepsilon \) is small (typically less than 1LSB)

\[ X_{\text{REF}} \sum_{j=1}^{n} \frac{d_{n-j}}{2^j} = X_{\text{IN}} + \varepsilon \]

- Number of bins gets very large for \( n \) large
- Spacing between break points is \( X_{\text{REF}}/2^n \) and gets very small for \( n \) large

\( \varepsilon \) is the quantization error and is inherent in any ADC
A/D Converters

Transition Points

- Actual values of $x_{IN}$ where transitions occur are termed transition points or break points.
- For an ideal n-bit ADC, there are $2^n - 1$ transition points.
- Ideally the transition points are all separated by 1 LSB -- $X_{LSB} = X_{REF}/2^n$.
- Ideally the transition points are uniformly spaced.
- In an actual ADC, the transition points will deviate a little from their ideal location.

Labeling Convention:

We will define the transition point $X_{Tk}$ to be the break point where the transition in the code output to code $C_k$ occurs. This seemingly obvious ordering of break points becomes ambiguous, though, when more than one break points cause a transition to code $C_k$ which can occur in some nonideal ADCs.
A/D Converters

Quantization Errors

$$x_{T1} = x_{LSB}$$

$$\varepsilon_Q = \tilde{x}_{OUT} - x_{IN}$$

Magnitude of $$\varepsilon_Q$$ bounded by $$x_{LSB}$$ for an ideal A/D
A/D Converters

Quantization Errors

Another Ideal ADC

\[ x_{T1} = \frac{x_{LSB}}{2} \]

\[ \varepsilon_Q = \tilde{x}_{OUT} - x_{IN} \]

Magnitude of \( \varepsilon_Q \) bounded by \( \frac{1}{2} x_{LSB} \)

Is the performance of this ideal ADC really better than that of the previous ideal ADC?
Data Converter Architectures

- Large number of different circuits have been proposed for building data converters.
- Often a dramatic difference in performance from one structure to another.
- Performance of almost all structures are identical if ideal components are used.
- Much of data converter design involves identifying the problems associated with a given structure and figuring out ways to reduce the effects of these problems.
- Critical that all problems that are significant be identified and solved.
- Many of the problems are statistical in nature and implications of not solving problems are in a yield loss that may be dramatic.
Data Converter Architectures

Strategy for discussing data converters

- Briefly look at some different data converter architectures
- Detailed discussion of performance parameters for data converters
- More detailed discussion of data converter architectures
Data Converter Architectures

Nyquist Rate

Flash
Charge Redistribution
Pipeline
Two-step and Multi-Step
Interpolating
Algorithmic/Cyclic
Successive Approximation (Register) SAR
Single Slope / Dual Slope
Subranging
Folded
Interleaved

Current Steering
R-string
Charge Redistribution
Algorithmic
R-2R (ladder)
Pipelined
Subranging

Over-Sampled (Delta-Sigma)

Discrete-time
First-order/Higher Order
Continuous-time

Discrete-time
First-order/Higher Order
Continuous-time
Data Converter Architectures

Flash

Thermometer to Binary Decoder
End of Lecture 22