EE 435

Lecture 22

Offset Voltages
Common Mode Feedback
Offset Voltage

Two types of offset voltage:

- Systematic Offset Voltage
- Random Offset Voltage

Definition: The output offset voltage is the difference between the desired output and the actual output when \( V_{id} = 0 \) and \( V_{ic} \) is the quiescent common-mode input voltage.

\[
V_{OUTOFF} = V_{OUT} - V_{OUTDES}
\]

Note: \( V_{OUTOFF} \) is dependent upon \( V_{ICQ} \), although this dependence is usually quite weak and often not specified.
Definition: The input-referred offset voltage is the differential dc input voltage that must be applied to obtain the desired output when \( V_{ic} \) is the quiescent common-mode input voltage.

Note: \( V_{OFF} \) is usually related to the output offset voltage by the expression

\[
V_{OFF} = \frac{V_{OUTOFF}}{A_C}
\]

Note: \( V_{OFF} \) is dependent upon \( V_{ICQ} \) although this dependence is usually quite weak and often not specified.
Offset Voltage

Two types of offset voltage:

- Systematic Offset Voltage
- Random Offset Voltage

After fabrication it is impossible (difficult) to distinguish between the systematic offset and the random offset in any individual op amp.

Measurements of offset voltages for a large number of devices will provide mechanism for identifying systematic offset and statistical characteristics of the random offset voltage.
Gradient Effects: Locally Appear Linear

- Magnitude and Direction of Gradients are random
- Highly Correlated over Short Distances

Local Random Effects:
Vary Locally With No Correlation

- Both Contribute to Offset
- Both are random variables
- If Not Managed, Both Can Cause Large Offsets
- Strategies for minimizing their effects are different
- Will refer to the local random effects as “random” and the random gradient effects as “gradient” effects
Offset Voltage

Can be modeled as a dc voltage source in series with the input
Offset Voltage

Effects of Offset Voltage - an example

Desired I/O relationship

![Diagram of an operational amplifier circuit with input (VIN) and output (VOUT) terminals, resistors R1 and R2, and desired input-output (I/O) relationship graph. The graph shows voltage levels (VDD, VM) over time (t).]
Offset Voltage

Effects of Offset Voltage - an example

Desired I/O relationship

Actual I/O relationship due to offset
Effects can be reduced or eliminated by adding equal amplitude opposite Dc signal (many ways to do this)

Widely used in offset-critical applications

Comes at considerable effort and expense

*Prefer to have designer make $V_{OS}$ small in the first place*
Effects of Offset Voltage

• Deviations in performance will change from one instantiation to another due to the random component of the offset

• Particularly problematic in high-gain circuits

• A major problem in many other applications

• Not of concern in many applications as well
Offset Voltage Distribution

Typical histogram of random offset voltage (binned) after fabrication
Offset Voltage Distribution

Gaussian (Normal) pdf

Typical histogram of offset voltage (binned) after fabrication

Mean is nearly 0 (actually the systematic offset voltage)
Offset Voltage Distribution

Typical histogram of offset voltage (binned) in shipped parts

Extreme offset parts have been sifted at test
Offset Voltage Distribution

Typical histogram of offset voltage (binned) in shipped parts

Low-offset parts sold at a premium

Extreme offset parts have been sifted at test
Offset Voltage Distribution

Pdf of zero-mean Gaussian distribution

Characterized by its standard deviation $\sigma$ or variance $\sigma^2$

Offset voltage often specified as the $1\sigma$ or $3\sigma$ value
Offset Voltage Distribution

Pdf of zero-mean Gaussian distribution

Percent between:

- $\pm \sigma$ 68.3%
- $\pm 2\sigma$ 95.5%
- $\pm 3\sigma$ 99.73%
Source of Random Offset Voltages

Consider as an example:

\[ V_{OUT} = V_{DD} - \left( \frac{I_T}{2} \right) R \]

Ideally \( R_1=R_2=R \), \( M_1 \) and \( M_2 \) are matched

Assume this is the desired output voltage
Source of Random Offset Voltages

Consider as an example:

If everything ideal except $R_2 = R + \Delta R$

$$V_{OUT} = V_{DD} \left( \frac{I_T}{2} \right) [R + \Delta R]$$

$$\Delta V_{OUT} = -\left( \frac{I_T}{2} \right) \Delta R$$
Source of Random Offset Voltages

Consider as an example:

\[ A_V = -\frac{g_m}{2} R \]
Source of Random Offset Voltages

Determine the offset voltage – i.e. value of $V_X$ needed to obtain desired output

$$V_{OUT} = \left[ V_{DD} - \left( \frac{I_T}{2} \right) R \right] - \left( \frac{I_T}{2} \right) \Delta R - A_V V_X$$

$$V_X = \left( \frac{I_T}{2} \right) \Delta R$$

$$A_V = -\frac{g_m}{2} R$$
Source of Random Offset Voltages

Determine the offset voltage – i.e. value of $V_X$ needed to obtain desired output

$$A_V = -\frac{g_m}{2}R$$

$$V_X = \frac{-1}{A_V} \left( \frac{I_T}{2} \right) \Delta R$$

$$V_X = \frac{2}{g_m R} \left( \frac{I_T}{2} \right) \Delta R = \left( \frac{I_T}{g_m} \right) \frac{\Delta R}{R} = \left( \frac{I_T}{I_T/V_{EB}} \right) \frac{\Delta R}{R} = V_{EB} \frac{\Delta R}{R}$$

$$V_X = V_{EB} \frac{\Delta R}{R}$$
The random offset voltage is almost entirely that of the input stage in most op amps.
Random Offset Voltages

Impurities vary randomly with position as do edges of gate, oxide and diffusions.

Model and design parameters vary throughout channel and thus the corresponding equivalent lumped model parameters will vary from device to device.
The random offset is due to mismatches in the four transistors, dominantly mismatches in the parameters \( \{V_T, \mu, C_{OX}, W \text{ and } L\} \)

The relative mismatch effects become more pronounced as devices become smaller.

\[
V_{Ti} = V_{TN} + V_{TRi}
\]

\[
C_{OXi} = C_{OXN} + C_{OXRi}
\]

\[
\mu_i = \mu_N + \mu_{Ri}
\]

\[
W_i = W_N + W_{Ri}
\]

\[
L_i = L_N + L_{Ri}
\]

Each design and model parameter is comprised of a nominal part and a random component.
For each device, the device model is often expressed as

\[
I_{Di} = \frac{1}{2} \left( \mu_N + \mu_{Ri} \right) \left( C_{OXi} = C_{OXN} + C_{OXri} \right) \left( W_i = W_N + W_{Ri} \right) \left( V_{GSi} - (V_{TN} + V_{TRi}) \right)^2 \left( 1 + (\lambda_N + \lambda_{Ri}) [V_{DS}] \right)
\]

Because of the random components of the parameters in every device, matching from the left-half circuit to the right half-circuit is not perfect.

This mismatch introduces an offset voltage which is a random variable.
Random Offset Voltages

From a straightforward but tedious analysis it follows that:

\[
\sigma_{V_{OS}}^2 = 2 \left[ \frac{A_{VTO n}^2 + \mu_p L_n A_{VTO p}^2}{W_n L_n} + \frac{V_{EB n}^2}{4} \right] \left( \frac{1}{W_n L_n} \frac{A^2}{\mu_n} + \frac{1}{W_p L_p} \frac{A^2}{\mu_p} + A_{COX}^2 \left[ \frac{1}{W_n L_n} + \frac{1}{W_p L_p} \right] + 2A_L^2 \left[ \frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2} \right] + A_W^2 \left[ \frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2} \right] \right)
\]

where the terms \( A_{VTO}, A_\mu, A_{COX}, A_L, \) and \( A_W \) are process parameters

\[
A_{VTO} \approx \begin{cases} 21 \text{mV} \cdot \mu & \text{(n-ch)} \\ 25 \text{mV} \cdot \mu & \text{(p-ch)} \end{cases}
\]

\[
\sqrt{A_\mu^2 + A_{COX}^2} \approx \begin{cases} 0.016 \mu & \text{(n-ch)} \\ 0.023 \mu & \text{(p-ch)} \end{cases}
\]

\[
A_L = A_W \approx 0.017 \mu^{1/2}
\]

Usually the \( A_{VTO} \) terms are dominant, thus the variance simplifies to

\[
\sigma_{V_{OS}}^2 \approx 2 \left[ \frac{A_{VTO n}^2 + \mu_p L_n A_{VTO p}^2}{W_n L_n} \right]
\]
Random Offset Voltages

Correspondingly:

$$\sigma_{V_{OS}}^2 = 2 \left[ \frac{A_{VTO_n}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n L_p^2} A_{VTO_p}^2 + \frac{V_{EBn}^2}{4} \left( \frac{1}{W_n L_n} A_{\mu_n}^2 + \frac{1}{W_p L_p} A_{\mu_p}^2 + A_{\text{COX}}^2 \left[ \frac{1}{W_n L_n} + \frac{1}{W_p L_p} \right] \right) + 2A_L \left[ \frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2} \right] + A_w^2 \left[ \frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2} \right] \right]$$

which again simplifies to

$$\sigma_{V_{OS}}^2 \approx 2 \left[ \frac{A_{VTO_n}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n L_p^2} A_{VTO_p}^2 \right]$$

Note these offset voltage expressions are identical!
Random Offset Voltages

Example: Determine the $3\sigma$ value of the input offset voltage for the MOS differential amplifier if

a) $M_1$ and $M_3$ are minimum-sized and
b) the area of $M_1$ and $M_3$ are 100 times minimum size

$$
\sigma_{V_{OS}}^2 \approx 2 \left[ \frac{A_{V_{TO \, n}}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n^2}{W_n L_p} \right]
$$

$$
\sigma_{V_{OS}}^2 \approx \frac{2}{W_n L_n} \left[ \frac{A_{V_{TO \, n}}^2}{\mu_n} + \frac{\mu_p}{\mu_n} A_{V_{TO \, p}}^2 \right]
$$

a) $$
\sigma_{V_{OS}}^2 \approx \frac{2}{(0.5\mu)^2} \left[ 0.021^2 + \frac{1}{3} 0.025^2 \right]
$$

$$
\sigma_{V_{OS}} \approx 72\text{mV}
$$

$$
3 \sigma_{V_{OS}} \approx 216\text{mV}
$$

Note this is a very large offset voltage!
Random Offset Voltages

Example: Determine the $3\sigma$ value of the input offset voltage for the MOS differential amplifier is

a) $M_1$ and $M_3$ are minimum-sized and
b) the area of $M_1$ and $M_3$ are 100 times minimum size

\[
\begin{align*}
\sigma^2_{V_{OS}} & \approx 2 \left[ \frac{A^2_{VTO_n}}{W_n L_n} + \frac{\mu_p L_n}{\mu_n W_n L_p^2} A^2_{VTO_p} \right] \\
\sigma^2_{V_{OS}} & \approx \frac{2}{W_n L_n} \left[ \frac{A^2_{VTO_n}}{\mu_n} + \frac{\mu_p A^2_{VTO_p}}{\mu_n} \right]
\end{align*}
\]

\[\sigma_{V_{OS}} \approx 7.2\text{mV}\]

\[3 \sigma_{V_{OS}} \approx 21.6\text{mV}\]

Note this is much lower but still a large offset voltage!

The area of $M_1$ and $M_3$ needs to be very large to achieve a low offset voltage.
It can be shown that

\[ \sigma_{V_{OS}}^2 \approx 2V_t^2 \left[ \frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}} \right] \]

where very approximately

\[ A_{Jn} = A_{Jp} = 0.1 \mu \]
Random Offset Voltages

Example: Determine the $3\sigma$ value of the offset voltage of a bipolar input stage if $A_{E1}=A_{E3}=10\mu^2$

$$\sigma^2_{V_{OS}} \approx 2V_t^2 \left[ \frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}} \right]$$

$$\sigma_{V_{OS}} \approx \sqrt{2}V_t A_J \frac{\sqrt{2}}{\sqrt{A_E}}$$

$$\sigma_{V_{OS}} \approx 2 \cdot 25mV \cdot 0.1\mu \cdot \frac{1}{\sqrt{10\mu^2}} = 1.6mV$$

$$3\sigma_{V_{OS}} \approx 4.7mV$$

Note this value is much smaller than that for the MOS input structure!
Random Offset Voltages

Typical offset voltages:

MOS - 5mV to 50MV
BJT - 0.5mV to 5mV

These can be scaled with extreme device dimensions

Often more practical to include offset-compensation circuitry
Common Centroid Layouts

Define $p$ to be a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

**Almost Theorem:**

If $p(x,y)$ varies throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A} \int_A p(x,y) \, dx \, dy$$

Parameters such as $V_T$, $\mu$ and $C_{OX}$ vary throughout a two-dimensional region.
\[ p_{EQ} = \frac{1}{A} \int_A p(x, y) \, dx \, dy \]
Almost Theorem:

If \( p(x,y) \) varies linearly throughout a two-dimensional region, then
\[ p_{\text{EQ}} = p(x_0, y_0) \]
where \( x_0, y_0 \) is the geometric centroid to the region.

If a parameter varies linearly throughout a two-dimensional region, it is said
to have a linear gradient.

Many parameters have a dominantly linear gradient over rather small regions.
If \( \rho(x,y) \) varies linearly in any direction, then the theorem states

\[
\rho_{\text{EQ}} = \frac{1}{A} \int_A \rho(x,y) \, dx \, dy
\]

\((x_0,y_0)\) is geometric centroid

\[
\rho_{\text{EQ}} = \frac{1}{A} \int_A \rho(x,y) \, dx \, dy = \rho(x_0,y_0)
\]
Common Centroid Layouts

A layout of two devices is termed a common-centroid layout if both devices have the same geometric centroid.

Almost Theorem:

If \( p(x,y) \) varies linearly throughout a two-dimensional region, then if two devices have the same centroid, the lateral-variable parameters are matched!

Note: This is true independent of the magnitude and direction of the gradient!
Recall parallel combinations of transistors equivalent to a single transistor of appropriate $W, L$.
Centroids of Segmented Geometries

Denotes Geometric Centroid
Common Centroid of Multiple Segmented Geometries
Common Centroid of Multiple Segmented Geometries
Common centroid layouts widely (almost always) used where matching of devices or components is critical because these layouts will cancel all first-order gradient effects.

Applies to resistors, capacitors, transistors and other components.

Always orient all devices in the same way.

Keep common centroid for interconnects, diffusions, and all features.

Often dummy devices placed on periphery to improve matching!
Common Centroid Layout Surrounded by Dummy Devices
End of Lecture 22