EE 435

Lecture 23

Offset Voltages
Offset Voltage

Two types of offset voltage:

• Systematic Offset Voltage
• Random Offset Voltage

Definition: The output offset voltage is the difference between the desired output and the actual output when $V_{id} = 0$ and $V_{ic}$ is the quiescent common-mode input voltage.

$$V_{OUTOFF} = V_{OUT} - V_{OUTDES}$$

Note: $V_{OUTOFF}$ is dependent upon $V_{ICQ}$ although this dependence is usually quite weak and often not specified.
Offset Voltage

Definition: The input-referred offset voltage is the differential dc input voltage that must be applied to obtain the desired output when $V_{ic}$ is the quiescent common-mode input voltage.

$V_{OFF}$

$V_{ICQ}$

$V_{OUT}$

Note: $V_{OFF}$ is usually related to the output offset voltage by the expression

$$V_{OFF} = \frac{V_{OUTOFF}}{A_C}$$

Note: $V_{OFF}$ is dependent upon $V_{ICQ}$ although this dependence is usually quite weak and often not specified
Review from last lecture

## Offset Voltage

### Two types of offset voltage:

- **Systematic Offset Voltage**
- **Random Offset Voltage**

After fabrication it is impossible (difficult) to distinguish between the systematic offset and the random offset in any individual op amp.

Measurements of offset voltages for a large number of devices will provide mechanism for identifying systematic offset and statistical characteristics of the random offset voltage.
Gradient and Local Random Effect

Gradient Effects: Locally Appear Linear
- Magnitude and Direction of Gradients are random
- Highly Correlated over Short Distances

Local Random Effects:
- Vary Locally With No Correlation
- Both Contribute to Offset
- Both are random variables
- If Not Managed, Both Can Cause Large Offsets
- Strategies for minimizing their effects are different
- Will refer to the local random effects as “random” and the random gradient effects as “gradient” effects
Offset Voltage

Can be modeled as a dc voltage source in series with the input
Offset Voltage

Effects of Offset Voltage - an example

Desired I/O relationship

\[ V_{IN} \quad V_{OUT} \]

\[ R_1 \quad R_2 \]

\[ V_{IN} \quad V_{OUT} \quad V_{DD} \quad V_{M} \]
Offset Voltage

Effects of Offset Voltage - an example

Desired I/O relationship

Actual I/O relationship due to offset
Offset Voltage

Effects can be reduced or eliminated by adding equal amplitude opposite Dc signal (many ways to do this)

Widely used in offset-critical applications

Comes at considerable effort and expense

Prefer to have designer make $V_{OS}$ small in the first place
Effects of Offset Voltage

- Deviations in performance will change from one instantiation to another due to the random component of the offset
- Particularly problematic in high-gain circuits
- A major problem in many other applications
- Not of concern in many applications as well
Offset Voltage Distribution

Typical histogram of random offset voltage (binned) after fabrication
Offset Voltage Distribution

Typical histogram of offset voltage (binned) after fabrication

Mean is nearly 0 (actually the systematic offset voltage)
Offset Voltage Distribution

Typical histogram of offset voltage (binned) in shipped parts

Extreme offset parts have been sifted at test
Offset Voltage Distribution

Typical histogram of offset voltage (binned) in shipped parts

Low-offset parts sold at a premium

Extreme offset parts have been sifted at test
Offset Voltage Distribution

Pdf of zero-mean Gaussian distribution

Characterized by its standard deviation $\sigma$ or variance $\sigma^2$

Offset voltage often specified as the 1$\sigma$ or 3$\sigma$ value
Offset Voltage Distribution

Pdf of zero-mean Gaussian distribution

Percent between:

- $\pm \sigma$: 68.3%
- $\pm 2\sigma$: 95.5%
- $\pm 3\sigma$: 99.73%
Source of Random Offset Voltages

Consider as an example:

\[ V_{OUT} = V_{DD} - \left( \frac{I_T}{2} \right) R \]

Assume this is the desired output voltage
Source of Random Offset Voltages

Consider as an example:

If everything ideal except $R_2 = R + \Delta R$

$$V_{OUT} = V_{DD} \left( \frac{I_T}{2} \right) [R + \Delta R]$$

$$\Delta V_{OUT} = - \left( \frac{I_T}{2} \right) \Delta R$$
Source of Random Offset Voltages

Consider as an example:

\[ A_V = -\frac{g_m}{2} R \]
Source of Random Offset Voltages

Determine the offset voltage – i.e. value of $V_X$ needed to obtain desired output

$$A_V = -\frac{g_m R}{2}$$

$$V_{OUT} = V_{DD} - \left(\frac{I_T}{2}\right) R - \left(\frac{I_T}{2}\right) \Delta R - A_V V_X$$

$$V_X = -\frac{1}{A_V} \left(\frac{I_T}{2}\right) \Delta R$$
Source of Random Offset Voltages

Determine the offset voltage – i.e. value of $V_X$ needed to obtain desired output

$$A_V = -\frac{g_m}{2}$$

$$V_X = \frac{-1}{A_V} \left( \frac{I_T}{2} \right) \Delta R$$

$$V_X = \frac{2}{g_m R} \left( \frac{I_T}{2} \right) \Delta R = \left( \frac{I_T}{g_m R} \right) \Delta R = \left( \frac{I_T}{I_T / V_{EB}} \right) \Delta R = V_{EB} \frac{\Delta R}{R}$$

$$V_X = V_{EB} \frac{\Delta R}{R}$$
Source of Random Offset Voltages

The random offset voltage is almost entirely that of the input stage in most op amps.
Impurities vary randomly with position as do edges of gate, oxide and diffusions.

Model and design parameters vary throughout channel and thus the corresponding equivalent lumped model parameters will vary from device to device.
Random Offset Voltages

The random offset is due to mismatches in the four transistors, dominantly mismatches in the parameters \{V_T, \mu, C_{OX}, W and L\}

The relative mismatch effects become more pronounced as devices become smaller

\[ V_{Ti} = V_{TN} + V_{TRi} \]
\[ C_{OXi} = C_{OXN} + C_{OXRi} \]
\[ \mu_i = \mu_N + \mu_{Ri} \]
\[ W_i = W_N + W_{Ri} \]
\[ L_i = L_N + L_{Ri} \]

Each design and model parameter is comprised of a nominal part and a random component
Random Offset Voltages

\[ V_{Ti} = V_{TN} + V_{TRi} \]

\[ C_{OXi} = C_{OXN} + C_{OX Ri} \]

\[ \mu_i = \mu_N + \mu_{Ri} \]

\[ W_i = W_N + W_{Ri} \]

\[ L_i = L_N + L_{Ri} \]

For each device, the device model is often expressed as

\[ I_{Di} = \frac{(\mu_N + \mu_{Ri})(C_{OXN} + C_{OX Ri})(W_N + W_{Ri})}{2(L_N + L_{Ri})}(V_{GSi} - (V_{TN} + V_{TRi}))^2 (1 + (\lambda_N + \lambda_{Ri})[V_{DS}]) \]

Because of the random components of the parameters in every device, matching from the left-half circuit to the right half-circuit is not perfect.

This mismatch introduces an offset voltage which is a random variable.
Random Offset Voltages

From a straightforward but tedious analysis it follows that:

\[ \sigma_{V_{OS}}^2 = 2 \left[ \frac{A_{VTO n}^2}{W n L n} + \frac{\mu_p}{\mu_n} \frac{L_n^2}{W_n L_p^2} A_{VTO p}^2 + \frac{V_{EB n}^2}{4} \right] \]

where the terms \( A_{VTO} \), \( A_{\mu} \), \( A_{COX} \), \( A_L \), and \( A_W \) are process parameters.

\[ A_{VTO} \approx \begin{cases} 21 \text{mV} \cdot \mu \quad \text{(n-ch)} \\ 25 \text{mV} \cdot \mu \quad \text{(p-ch)} \end{cases} \]

\[ \sqrt{A_{\mu}^2 + A_{COX}^2} \approx \begin{cases} .016 \mu \quad \text{(n-ch)} \\ .023 \mu \quad \text{(p-ch)} \end{cases} \]

\[ A_L = A_W \approx 0.017 \mu^2 \]

Usually the \( A_{VTO} \) terms are dominant, thus the variance simplifies to

\[ \sigma_{V_{OS}}^2 \approx 2 \left[ \frac{A_{VTO n}^2}{W n L n} + \frac{\mu_p}{\mu_n} \frac{L_n^2}{W_n L_p^2} A_{VTO p}^2 \right] \]
Random Offset Voltages

Correspondingly:

\[
\sigma_{V_{OS}}^2 = 2 \left[ \frac{A_{VTOn}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n L_p^2} A_{VTOP}^2 + \frac{V_{EBn}^2}{4} \right] + \frac{1}{W_n L_n} A_{\mu_n}^2 + \frac{1}{W_p L_p} A_{\mu_p}^2 + A_{\text{COX}}^2 \left[ \frac{1}{W_n L_n} + \frac{1}{W_p L_p} \right] + 2A_L^2 \left[ \frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2} \right] + A_w^2 \left[ \frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2} \right]
\]

which again simplifies to

\[
\sigma_{V_{OS}}^2 \approx 2 \left[ \frac{A_{VTOn}^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n L_p^2} A_{VTOp}^2 \right]
\]

Note these offset voltage expressions are identical!
Random Offset Voltages

Example: Determine the $3\sigma$ value of the input offset voltage for the MOS differential amplifier if

a) $M_1$ and $M_3$ are minimum-sized and

b) the area of $M_1$ and $M_3$ are 100 times minimum size

\[
\sigma_{V_{OS}}^2 \approx 2 \left[ \frac{A^2_{VTO n}}{W_n L_n} + \frac{\mu_p L_n}{\mu_n W_n L_p^2} A^2_{VTO p} \right]
\]

\[
\sigma_{V_{OS}}^2 \approx \frac{2}{W_n L_n} \left[ A^2_{VTO n} + \frac{\mu_p A^2_{VTO p}}{\mu_n} \right]
\]

\[
\sigma_{V_{OS}}^2 \approx \frac{2}{(0.5\mu)^2} \left[ .021^2 + \frac{1}{3} .025^2 \right]
\]

\[
\sigma_{V_{OS}} \approx 72\text{mV}
\]

\[
3 \sigma_{V_{OS}} \approx 216\text{mV}
\]

Note this is a very large offset voltage!
Random Offset Voltages

Example: Determine the $3\sigma$ value of the input offset voltage for

The MOS differential amplifier is

a) $M_1$ and $M_3$ are minimum-sized and

b) the area of $M_1$ and $M_3$ are 100 times minimum size

\[
\sigma_{V_{OS}}^2 \approx 2 \left[ \frac{A^2}{W_n L_n} + \frac{\mu_p}{\mu_n} \frac{L_n}{W_n} A^2 \frac{V_{TO n}}{V_{TO p}} \right]
\]

\[
\sigma_{V_{OS}}^2 \approx \frac{2}{W_n L_n} \left[ \frac{A^2}{V_{TO n}} + \frac{\mu_p}{\mu_n} A^2 \frac{V_{TO n}}{V_{TO p}} \right]
\]

b) 

\[
\sigma_{V_{OS}}^2 \approx \frac{2}{100(0.5\mu)^2} \left[ 0.021^2 + \frac{1}{3} \cdot 0.025^2 \right]
\]

\[
\sigma_{V_{OS}} \approx 7.2\text{mV}
\]

\[
3 \sigma_{V_{OS}} \approx 21.6\text{mV}
\]

Note this is much lower but still a large offset voltage!

The area of $M_1$ and $M_3$ needs to be very large to achieve a low offset voltage.
Random Offset Voltages

\[ \sigma_{V_{OS}}^2 \approx 2V_t^2 \left( \frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}} \right) \]

where very approximately

\[ A_{Jn} = A_{Jp} = 0.1\mu \]
Random Offset Voltages

Example: Determine the $3\sigma$ value of the offset voltage of a bipolar input stage if $A_{E1}=A_{E3}=10\mu^2$

\[ \sigma_{V_{OS}}^2 \approx 2V_t^2 \left[ \frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}} \right] \]

\[ \sigma_{V_{OS}} \approx \sqrt{2}V_t A_J \frac{\sqrt{2}}{\sqrt{A_E}} \]

\[ \sigma_{V_{OS}} \approx 2 \cdot 25\text{mV} \cdot 0.1\mu \cdot \frac{1}{\sqrt{10\mu^2}} = 1.6\text{mV} \]

\[ 3\sigma_{V_{OS}} \approx 4.7\text{mV} \]

Note this value is much smaller than that for the MOS input structure!
Random Offset Voltages

Typical offset voltages:

MOS - 5mV to 50MV
BJT - 0.5mV to 5mV

These can be scaled with extreme device dimensions

Often more practical to include offset-compensation circuitry
End of Lecture 23