EE 435

Lecture 25

Exam 1 Was Given During this Period
Problem 1 Consider the op amp architecture shown below. Assume the lengths of all devices are 2.4\(\mu\)m, the capacitive load is 1pF, the supply voltage is 5V, the excess bias of all transistors is 250mV, and the power dissipation is 5mW.

a) Analytically determine the dimensions of all devices
b) Analytically determine the dc voltage gain
c) Analytically determine the GB of the amplifier
d) Analytically determine the SR of the amplifier
e) Analytically determine the output voltage swing if the common-mode input voltage is 2V.
Problem 2  
Assume a common-centroid layout is used for transistors M1-M4 in the amplifier given in Problem 1 and the matching parameters are as given below.

a) Determine the $3\sigma$ value for the random offset voltage

b) Repeat Part a) if the same architecture is used but with p-channel inputs instead of n-channel inputs. Assume the same design conditions as given in the statement of Problem 1.

c) Size the transistors in the Amplifier of Problem 1 for an offset yield of 92% if the magnitude of the maximum acceptable offset voltage is 10mV.

\[
A_{VT0} = \begin{cases} 
21\text{mV} \cdot \mu & \text{ (n-ch)} \\
25\text{mV} \cdot \mu & \text{ (p-ch)} 
\end{cases}
\]

\[
\sqrt{A_{\mu}^2 + A_{COX}^2} = \begin{cases} 
.016\mu & \text{ (n-ch)} \\
.023\mu & \text{ (p-ch)} 
\end{cases}
\]

\[A_L = A_W = 0\]
Problem 3  
A large number of different op amp architectures were identified in class. A table summarizing some of the more popular possible structures is shown below.

<table>
<thead>
<tr>
<th></th>
<th>Common Source</th>
<th>Cascode</th>
<th>Regulated Cascode</th>
<th>Folded Cascode</th>
<th>Folded Regulated Cascode</th>
<th>Current Mirror</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stage 1</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Differential Input</td>
<td>Single-Ended Input</td>
<td>Differential Output</td>
<td>Single-Ended Output</td>
<td>Tail Voltage Bias</td>
<td>Tail Current Bias</td>
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<tr>
<td>Stage 2</td>
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<tr>
<td></td>
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<td>Tail Voltage Bias</td>
<td>Tail Current Bias</td>
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<tr>
<td></td>
<td>Internally Compensated</td>
<td>Output Compensated</td>
<td></td>
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<td></td>
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</tr>
<tr>
<td></td>
<td>p-channel Input</td>
<td>n-channel Input</td>
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<td></td>
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</tbody>
</table>

a) Give the schematic of a two-stage op amp with a folded cascode first stage, a common source second stage, with a differential input and single-ended output on the first stage. Use p-channel inputs on the first stage and n-channel inputs on the second stage. Use tail current bias on the first stage and tail voltage bias on the second stage. Use output compensation. Assume the total output capacitance (including any compensation capacitance) is $C_L$.

b) Give an expression for the dc gain of the amplifier in terms of the small-signal model parameters.

c) Give an expression for the GB of the amplifier in terms of the small-signal parameters.

d) If $C_L=1\mu F$, $V_{DD}=5V$, the total power dissipation is 10mW, and 1/3 of the power is dissipated in the differential input pair, 1/3 in the output stage, and 1/3 in the cascode string, determine the GB. Some degrees of freedom for uniquely solving this problem may not have been given. State clearly how you are using any additional degrees of freedom needed when solving this problem.
Problem 4  

The magnitude and phase plot of an operational amplifier are shown.

a) Determine the phase margin if this is used in a feedback amplifier with a feedback factor of $\beta=0.1$

b) Is the feedback amplifier stable? Why?

c) What is the maximum value of $\beta$ that can be used if the amplifier is to have a $60^\circ$ phase margin?

d) If $\beta = 0.02$, what is the ideal dc closed loop gain if configured as a basic noninverting feedback amplifier and what is the percent closed-loop gain error due to the finite dc gain limitations of the op amp?

e) How many poles does this amplifier have?
Problem 5 The amplifier shown is to be used as a quarter circuit for an operational amplifier. Give the schematic of the operational amplifier, the dc gain, and the GB if driving a capacitive load on each side of $C_L$. If your circuit needs a CMFB, please state and show where it would be connected but do not show any details of the CMFB. If $A=-1$, are there any simplifications that you can make on your circuit? Comment about any practical applications or interesting properties of this circuit.
Problem 6  The network shown is to be used at the β network of a feedback amplifier. If the signal through the β network propagates in the direction shown, determine β under the conditions that the overall feedback amplifier is
   a) A current amplifier
   b) A voltage amplifier
   c) A transresistance amplifier
   d) A transconductance amplifier

![Network Diagram](image-url)
Problem 7 (Extra Credit)

Consider the amplifier shown below where the $C_L$ is 1pF. Obtain analytical expressions for and plot the GB versus power dissipation if $V_{EB}$ is fixed at 500mV, $V_{DD}=5V$, and power is varied from 1nW to 10W under two scenarios

a) All parasitic capacitances in the transistor can be neglected
b) The diffusion capacitors on the drain and source of $M_1$ are included

Assume the transistor is rectangular and that minimum dimensions in the process are used in the layout of the drain and source.