EE 435

Lecture 25

Data Converters

- Architectures
- Characterization
Data Converters

Types:

A/D (Analog to Digital)
Converts Analog Input to a Digital Output

D/A (Digital to Analog)
Converts a Digital Input to an Analog Output

A/D is the world’s most widely used mixed-signal component

D/A is often included in a FB path of an A/D

A/D and D/A fields will remain hot indefinitely;
technology advances make data converter design more challenging for embedded applications;
designs often very application dependent.
D/A Converters

For this ideal DAC

\[ x_{\text{OUT}} = x_{\text{REF}} \left( \frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \frac{b_{n-3}}{8} + \ldots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n} \right) \]

\[ x_{\text{OUT}} = x_{\text{REF}} \sum_{j=1}^{n} \frac{b_{n-j}}{2^j} \]

- Number of outputs gets very large for \( n \) large
- Spacing between outputs is \( X_{\text{REF}}/2^n \) and gets very small for \( n \) large
A/D Converters

Quantization Errors

$X_{T1} = X_{LSB}$

$\epsilon_Q = X_{OUT} - X_{IN}$

Magnitude of $\epsilon_Q$ bounded by $X_{LSB}$ for an ideal A/D
Data Converter Architectures

Nyquist Rate
Flash
Charge Redistribution
Pipeline
Two-step and Multi-Step
Interpolating
Algorithmic/Cyclic
Successive Approximation (Register) SAR
Single Slope / Dual Slope
Subranging
Folded
Interleaved

Over-Sampled (Delta-Sigma)
Discrete-time
First-order/Higher Order
Continuous-time
Data Converter Architectures

Flash
Data Converter Architectures

Successive Approximation Register (SAR)
Data Converter Architectures

**Charge Redistribution**

\[
Q_{SAM} = V_{IN} \left( \sum_{i=0}^{n-1} C_i + \left[ C_0' \right] \right) = V_{IN} \left( \sum_{i=0}^{n-1} \frac{C}{2^{n-i}} + \left[ \frac{C}{2^n} \right] \right) = V_{IN} C
\]

\[
Q_{REDIS} = V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}}
\]

\[
Q_{SAM} = Q_{REDIS}
\]

\[
V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{IN} C
\]

\[
V_{IN} = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}
\]

\[
V_{COMP} = \begin{cases} 1 & t < T_{CONV} \\ 0 & t \geq T_{CONV} \end{cases}
\]

\[
V_{COMP} = \begin{cases} 1 & t < T_{CLK} \\ 0 & t \geq T_{CLK} \end{cases}
\]
Data Converter Architectures

Single Slope

Comparator Changes States when

\[ V_{IN} = I_0 \int_{0}^{t_{TR}} V_{REF} dT = I_0 t_{TR} V_{REF} \]

Counter stops when

\[ V_{IN} = t_{TR} V_{REF} I_0 \neq n_{COUNT} T_{CLK} V_{REF} I_0 \]

If calibrate so that

\[ 2^n \neq \left( \frac{f_{CLK}}{I_0} \right) \]
Data Converter Architectures

R-String

$X_{\text{IN}}$ is decoded to close one switch
Data Converter Architectures

Current Steering

\[ V_{RFF} \]

\[ X_{IN} \]

DAC

\[ x_{OUT} \]

\[ R \]

\[ V_{OUT} \]
Data Converter Architectures

**R-2R** (4-bits)

By superposition:

\[
V_{\text{OUT}} = V_{\text{REF}} d_3 \cdot \frac{1}{2} + V_{\text{REF}} d_2 \cdot \frac{1}{4} + V_{\text{REF}} d_1 \cdot \frac{1}{8} + V_{\text{REF}} d_0 \cdot \frac{1}{16} = V_{\text{REF}} \sum_{k=0}^{3} \frac{d_k}{2^{4-k}} = V_{\text{REF}} \sum_{k=1}^{4} \frac{d_{4-k}}{2^k}
\]
Data Converter Architectures

Charge Redistribution

\[ \dot{X}_{IN} \rightarrow \text{DAC} \rightarrow X_{OUT} \]

Successive Approximation Block

\[ Q_{SET} = V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} \]

\[ Q_{RDIS} = V_{OUT} \left( \sum_{i=0}^{n-1} C_i + \left[ C_0 \right] \right) = V_{OUT} \left( \sum_{i=0}^{n-1} \frac{C}{2^{n-i}} + \left[ \frac{C}{2^n} \right] \right) = V_{OUT} C \]

\[ Q_{SET} = Q_{RDIS} \]

\[ V_{REF} \sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{OUT} C \]

\[ V_{OUT} = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}} \]
Performance Characterization of Data Converters

- A very large number of parameters ($2^n$) characterize the static performance of an ADC!

- And even more parameters needed to characterize the dynamic performance of an ADC

- A large (but much smaller) number of parameters are invariably used to characterize a data converter

- Performance parameters of interest depend strongly on the application

- Very small number of parameters of interest in many/most applications

- "Catalog" data converters are generally intended to satisfy a wide range of applications and thus have much more stringent requirements placed on their performance

- Custom application-specific data converter will generally perform much better than a "catalog" part in the same application
Performance Characterization of Data Converters

• Static characteristics
  – Resolution
  – Least Significant Bit (LSB)
  – Offset and Gain Errors
  – Absolute Accuracy
  – Relative Accuracy
  – Integral Nonlinearity (INL)
  – Differential Nonlinearity (DNL)
  – Monotonicity (DAC)
  – Missing Codes (ADC)
  – Low-f Spurious Free Dynamic Range (SFDR)
  – Low-f Total Harmonic Distortion (THD)
  – Effective Number of Bits (ENOB)
  – Power Dissipation
Performance Characterization of Data Converters

• Dynamic characteristics
  – Conversion Time or Conversion Rate (ADC)
  – Settling time or Clock Rate (DAC)
  – Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  – Dynamic Range
  – Spurious Free Dynamic Range (SFDR)
  – Total Harmonic Distortion (THD)
  – Signal to Noise Ratio (SNR)
  – Signal to Noise and Distortion Ratio (SNDR)
  – Sparkle Characteristics
  – Effective Number of Bits (ENOB)
Dynamic characteristics

• Degradation of dynamic performance parameters often due to nonideal effects in time-domain performance

• Dynamic characteristics of high resolution data converters often challenging to measure, to simulate, to understand source of contributions, and to minimize

Example: An n-bit ADC would often require SFDR at the 6n+6 bit level or better. Thus, considering a 14-bit ADC, the SFDR would be expected to be at the -90dB level or better. If the input to the ADC is a 1V p-p sinusoidal waveform, the second harmonic term would need to be at the $10^{(-90dB/20dB)} = 32\mu V$ level. A 32uV level is about 1 part in 30,000. Signals at this level are difficult to accurately simulate in the presence of a 1V level signal. For example, convergence parameters in simulators and sample (strobe) points used in data acquisition adversely affect simulation results and observing the time domain waveforms that contribute to nonlinearity at this level and relationships between these waveforms and the sources of nonlinearity is often difficult to visualize. Simulation errors that are at the 20dB level or worse can occur if the simulation environment is not correctly established.
Performance Characterization of Data Converters

What is meant by “low frequency”? 

Operation at frequencies so low that further decreases in frequency cause no further changes in a parameter of interest 

Low frequency operation is often termed Pseudo-static operation
Low-frequency or Pseudo-Static Performance
End of Lecture 25