EE 435

Lecture 27

Data Converters
D/A Converters

\[
\tilde{X}_{IN} = \langle b_{n-1}, b_{n-1}, \ldots b_1, b_0 \rangle
\]

An Ideal DAC transfer characteristic (3-bits)

All points of this ideal DAC lie on a straight line
Waveform Generation with DACs

Ramp (Saw-tooth) Generator

Example: For $n=3$

Example: For large $n$
A/D Converters

An Ideal ADC transfer characteristic (3-bits)

\[ \tilde{X}_{\text{OUT}} = \langle d_{n-1}, d_{n-2}, \ldots, d_0 \rangle \]

\[ \chi_{\text{LSB}} = \frac{\chi_{\text{REF}}}{2^n} \]

Review from last lecture.
A/D Converters

Quantization Errors

Another Ideal ADC

\[ x_{T1} = \frac{x_{LSB}}{2} \]

\[ \varepsilon_Q = \tilde{x}_{OUT} - x_{IN} \]

Magnitude of \( \varepsilon_Q \) bounded by \( \frac{1}{2} x_{LSB} \)

Is the performance of this ideal ADC really better than that of the previous ideal ADC?
Data Converter Architectures

- Large number of different circuits have been proposed for building data converters
- Often a dramatic difference in performance from one structure to another
- Performance of almost all structures are identical if ideal components are used
- Much of data converter design involves identifying the problems associated with a given structure and figuring out ways to reduce the effects of these problems
- Critical that all problems that are significant be identified and solved
- Many of the problems are statistical in nature and implications of not solving problems are in a yield loss that may be dramatic
Data Converter Architectures

Strategy for discussing data converters

• Briefly look at some different data converter architectures
• Detailed discussion of performance parameters for data converters
• More detailed discussion of data converter architectures
Data Converter Architectures

Nyquist Rate

Flash
Pipeline
Two-step and Multi-Step Interpolating
Algorithmic/Cyclic
Successive Approximation Register
Single Slope / Dual Slope
Subranging
Folded

Current Steering
R-string
Charge Redistribution
Algorithmic
R-2R (ladder)
Pipelined
Subranging

Over-Sampled (Delta-Sigma)

Discrete-time
First-order/Higher Order
Continuous-time

Discrete-time
First-order/Higher Order
Continuous-time
Data Converter Architectures

Flash

Thermometer to Binary Decoder
Data Converter Architectures

Successive Approximation Register (SAR)
Data Converter Architectures

Single Slope
Data Converter Architectures

R-String

\( \bar{X}_{IN} \) \( \rightarrow \) DAC \( \Rightarrow X_{OUT} \)

\( V_{RFF} \) \( \downarrow \) \( X_{IN} \)

\( V_{OUT} \)
Data Converter Architectures

Current Steering

\[ \bar{X}_{IN} \xrightarrow{n} DAC \xrightarrow{} X_{OUT} \]

\[ V_{RFF} \]

\[ X_{IN} \xrightarrow{n} \]

\[ S_1 \quad S_2 \quad \ldots \quad S_k \]

\[ I_1 \quad I_2 \quad \ldots \quad I_k \]

\[ R \]

\[ V_{OUT} \]
Data Converter Architectures

\[ \bar{x}_{\text{IN}} \xrightarrow{n} \text{DAC} \xrightarrow{} x_{\text{OUT}} \]

\textbf{R-2R}

\[ \begin{array}{cccccc}
V_{\text{OUT}} & \text{R} & & & & \text{R} \\
\text{R} & & \text{2R} & & & \\
d_1 & & & & & \\
V_{\text{REF}} & & & & & \\
\text{2R} & & \text{R} & & & \\
d_2 & & & & & \\
\text{2R} & & \text{R} & & & \\
d_3 & & & & & \\
\text{2R} & & \text{R} & & & \\
d_4 & & & & & \\
\text{R} & & \text{R} & & & \\
\end{array} \]
End of Lecture 27