EE 435

Lecture 28

Data Converters
Data Converter Architectures

- Large number of different circuits have been proposed for building data converters
- Often a dramatic difference in performance from one structure to another
- Performance of almost all structures are identical if ideal components are used
- Much of data converter design involves identifying the problems associated with a given structure and figuring out ways to reduce the effects of these problems
- Critical that all problems that are significant be identified and solved
- Many of the problems are statistical in nature and implications of not solving problems are in a yield loss that may be dramatic
Data Converter Architectures

Nyquist Rate

Flash
Pipeline
Two-step and Multi-Step
Interpolating
Algorithmic/Cyclic
Successive Approximation Register
Single Slope / Dual Slope
Subranging
Folded

Current Steering
R-string
Charge Redistribution
Algorithmic
R-2R (ladder)
Pipelined
Subranging

Over-Sampled (Delta-Sigma)

Discrete-time
First-order/Higher Order
Continuous-time

Discrete-time
First-order/Higher Order
Continuous-time
Performance Characterization of Data Converters

- A very large number of parameters \(2^n\) characterize the static performance of an ADC!

- A large (but much smaller) number of parameters are invariably used to characterize a data converter

- Performance parameters of interest depend strongly on the application

- Very small number of parameters of interest in many/most applications

- “Catalog” data converters are generally intended to satisfy a wide range of applications and thus have much more stringent requirements placed on their performance

- Custom application-specific data converter will generally perform much better than a “catalog” part in the same
Performance Characterization of Data Converters

• Static characteristics
  – Resolution
  – Least Significant Bit (LSB)
  – Offset and Gain Errors
  – Absolute Accuracy
  – Relative Accuracy
  – Integral Nonlinearity (INL)
  – Differential Nonlinearity (DNL)
  – Monotonicity (DAC)
  – Missing Codes (ADC)
  – Low-f Spurious Free Dynamic Range (SFDR)
  – Low-f Total Harmonic Distortion (THD)
  – Effective Number of Bits (ENOB)
  – Power Dissipation
Performance Characterization of Data Converters

• Dynamic characteristics
  – Conversion Time or Conversion Rate (ADC)
  – Settling time or Clock Rate (DAC)
  – Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  – Dynamic Range
  – Spurious Free Dynamic Range (SFDR)
  – Total Harmonic Distortion (THD)
  – Signal to Noise Ratio (SNR)
  – Signal to Noise and Distortion Ratio (SNDR)
  – Sparkle Characteristics
  – Effective Number of Bits (ENOB)
Dynamic characteristics

- Degradation of dynamic performance parameters often due to nonideal effects in time-domain performance

- Dynamic characteristics often high resolution data converters often challenging to measure, to simulate, to understand source of contributions, and to minimize

Example: An n-bit ADC would often require SFDR at the $6n+6$ bit level or better. Thus, considering a 14-bit ADC, the SFDR would be expected to be at the -90dB level or better. If the input to the ADC is a 1V p-p sinusoidal waveform, the second harmonic term would need to be at the $10^{-90dB/20dB} = 32\mu V$ level. A 32uV level is about 1 part in 30,000. Signals at this level are difficult to accurately simulate in the presence of a 1V level signal. For example, convergence parameters in simulators and sample (strobe) points used in data acquisition adversely affect simulation results and observing the time domain waveforms that contribute to nonlinearity at this level and relationships between these waveforms and the sources of nonlinearity is often difficult to visualize. Simulation errors that are at the 20dB level or worse can occur if the simulation environment is not correctly established.
Performance Characterization of Data Converters

What is meant by “low frequency”?

Operation at frequencies so low that further decreases in frequency cause no further changes in a parameter of interest

Low frequency operation is often termed Pseudo-static operation
Low-frequency or Pseudo-Static Performance

Parameter

Pseudo-Static Region

f
Performance Characterization of Data Converters

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    - Missing Codes (ADC)
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    - Low-f Total Harmonic Distortion (THD)
    - Effective Number of Bits (ENOB)
    - Power Dissipation
Performance Characterization

Resolution

- Number of distinct analog levels in an ADC
- Number of digital output codes in A/D
- In most cases this is a power of 2
- If a converter can resolve $2^n$ levels, then we term it an $n$-bit converter
  - $2^n$ analog outputs for an $n$-bit DAC
  - $2^{n-1}$ transition points for an $n$-bit ADC
- Resolution is often determined by architecture and thus not measured
- Effective resolution can be defined and measured
  - If $N$ levels can be resolved for a DAC then
    $$n_{\text{EQ}} = \frac{\log N}{\log 2}$$
  - If $N-1$ transition points in an ADC, then
    $$n_{\text{EQ}} = \frac{\log N}{\log 2}$$
Performance Characterization

Least Significant Bit

Assume \( N = 2^n \)

Generally Defined by Manufacturer to be

\[ \chi_{\text{LSB}} = \chi_{\text{REF}} / N \]

Effective Value of LSB can be Measured

For DAC: \( \chi_{\text{LSB}} \) is equal to the maximum increment in the output for a single bit change in the Boolean input

For ADC: \( \chi_{\text{LSB}} \) is equal to the maximum distance between two adjacent transition points
Offset

For DAC the offset is

$X_{\text{OUT}} (<0, \ldots, 0>)$ - absolute

$X_{\text{OUT}} ([0, \ldots, 0])$

$X_{\text{LSB}}$

$X_{\text{OUT}}$

$x_{\text{REF}}$

Offset

$C_0$ $C_1$ $C_2$ $C_3$ $C_4$ $C_5$ $C_6$ $C_7$ $X_{\text{IN}}$
• Offset strongly (totally) dependent upon performance at a single point

• Probably more useful to define relative to a fit of the data
Performance Characterization

**Offset** (for DAC)

Offset relative to fit of data
Offset

For ADC the offset is

\[ X_{T1} - X_{\text{LSB}} \]

- absolute

\[ \frac{X_{T1} - X_{\text{LSB}}}{X_{\text{LSB}}} \]

- in LSB

\[ \dot{X}_{\text{OUT}} \]

\[ X_{\text{LSB}} \]

\[ X_{T1} \]

\[ \dot{X}_{\text{OFFSET}} \]

\[ \dot{X}_{\text{REF}} \]
Performance Characterization

Offset

For ADC the offset is

\[ \hat{x}_{\text{OUT}} \]

\[ C_7 \]
\[ C_6 \]
\[ C_5 \]
\[ C_4 \]
\[ C_3 \]
\[ C_2 \]
\[ C_1 \]
\[ C_0 \]

\[ x_{\text{LSB}} \]
\[ x_{\text{T1}} \]
\[ x_{\text{OFFSET}} \]
\[ x_{\text{REF}} \]

- Offset strongly (totally) dependent upon performance at a single point
- Probably more useful to define relative to a fit of the data
Offset

For ADC the offset is

Offset relative to fit of data
Performance Characterization

Gain and Gain Error

For DAC

\( x_{\text{OUT}} \)

\( x_{\text{REF}} \)

\( x_{\text{IN}} \)

Ideal Output

Actual Output

Gain Error

C0 C1 C2 C3 C4 C5 C6 C7
Performance Characterization

Gain and Gain Error

For ADC

\[ \bar{X}_{\text{OUT}} \]

\[ X_{\text{LSB}} \]

\[ X_{\text{REF}} \]

Actual Output

Ideal Output

Gain Error
Gain and Offset Errors

• Fit line would give better indicator of error in gain but less practical to obtain in test

• Gain and Offset errors of little concern in many applications

• Performance often nearly independent of gain and offset errors

• Can be trimmed in field if gain or offset errors exist.
Integral Nonlinearity (DAC)

Nonideal DAC

\[ x_{\text{OUT}} \quad x_{\text{REF}} \quad C_0 \quad C_1 \quad C_2 \quad C_3 \quad C_4 \quad C_5 \quad C_6 \quad C_7 \quad \hat{x}_{\text{IN}} \]
Integral Nonlinearity (DAC)

Nonideal DAC

\[ \mathcal{X}_{OF}(k) = mk + (\mathcal{X}_{OUT}(N-1) - \mathcal{X}_{OUT}(0)) \]

\[ m = \frac{\mathcal{X}_{OUT}(N-1) - \mathcal{X}_{OUT}(0)}{N-1} \]
Integral Nonlinearity (DAC)

**Nonideal DAC**

\[ \text{INL}_k = x_{\text{OUT}}(k) - x_{\text{OF}}(k) \]

\[ \text{INL} = \max_{0 \leq k \leq N-1} \left\{ |\text{INL}_k| \right\} \]
Integral Nonlinearity (DAC)

Nonideal DAC

\[ x_{\text{REF}} \]

\[ x_{\text{OUT}} \]

\[ x_{\text{IN}} \]
Integral Nonlinearity (DAC)

Nonideal DAC

INL often expressed in LSB

\[ \text{INL}_k = \frac{\mathcal{X}_{\text{OUT}}(k) - \mathcal{X}_{\text{OF}}(k)}{\mathcal{X}_{\text{LSB}}} \]

\[ \text{INL} = \max_{0 \leq k \leq N-1} \left\{ \| \text{INL}_k \| \right\} \]

- INL is often the most important parameter of a DAC
- INL$_0$ and INL$_{N-1}$ are 0 (by definition)
- There are N-2 elements in the set of INL$_k$ that are of concern
- INL is almost always nominally 0 (i.e. designers try to make it 0)
- INL is a random variable at the design stage
- INL$_k$ is a random variable for 0<k<N-1
- INL$_k$ and INL$_{k+j}$ are almost always correlated for all k,j (not incl 0, N-1)
- Fit Line is a random variable
- INL is the N-2 order statistic of a set of N-2 correlated random variables
Integral Nonlinearity (DAC)

Nonideal DAC

- At design stage, INL characterized by standard deviation of the random variable
- Closed-form expressions for INL almost never exist because PDF of order statistics of correlated random variables is extremely complicated
- Simulation of INL very time consuming if \( n \) is very large (large sample size required to establish reasonable level of confidence)
  - Model parameters become random variables
  - Process parameters affect multiple model parameters causing model parameter correlation
  - Simulation times can become very large
- INL can be readily measured in laboratory but often dominates test costs because of number of measurements needed when \( n \) is large
- Expected of \( \text{INL}_k \) at \( k=(N-1)/2 \) is largest for many architectures
- Major effort in DAC design is in obtaining acceptable yield!
Integral Nonlinearity (ADC)

Nonideal ADC

Transition points are not uniformly spaced!

More than one definition for INL exists!

Will give two definitions here
Integral Nonlinearity (ADC)

Consider end-point fit line with interpreted output axis

\[ X_{\text{INF}}(x_{\text{IN}}) = m x_{\text{IN}} + \left( \frac{x_{\text{LSB}}}{2} - m x_{T1} \right) \]

\[ m = \frac{(N-2)x_{\text{LSB}}}{x_{T7} - x_{T1}} \]
Integral Nonlinearity (ADC)

Nonideal ADC

Continuous-input based INL definition

\[ \tilde{X}_{IN} = \tilde{X}_{IN}(X) - X_{INF}(X) \]

\[ \text{INL} = \max_{0 \leq X_{IN} \leq X_{REF}} \left| \text{INL}(X_{IN}) \right| \]
Integral Nonlinearity (ADC)

Nonideal ADC

Continuous-input based INL definition

Often expressed in LSB

\[
\text{INL}(x_{\text{IN}}) = \frac{x_{\text{IN}}(x_{\text{IN}}) - x_{\text{INF}}(x_{\text{IN}})}{x_{\text{LSB}}}
\]

\[
\text{INL} = \max_{0 \leq x_{\text{IN}} \leq x_{\text{REF}}} \left\{ \left| \text{INL}(x_{\text{IN}}) \right| \right\}
\]
Integral Nonlinearity (ADC)

Nonideal ADC

With this definition of INL, the INL of an ideal ADC is $\Delta \text{LSB}/2$ (for $\Delta T_1 = \Delta \text{LSB}$)

This is effective at characterizing the overall nonlinearity of the ADC but does not vanish when the ADC is ideal and the effects of the breakpoints is not explicit.
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

Place N-3 uniformly spaced points between \( X_{T1} \) and \( X_{T(N-1)} \) designated \( X_{FTk} \)

\[
INL_k = X_{Tk} - X_{FTk} \quad 1 \leq k \leq N-2
\]

\[
INL = \max_{2 \leq k \leq N-2} \{ \left| \text{INL}_k \right| \}
\]
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

\[ \text{INL}_k = \frac{x_{T_k} - x_{F_k}}{x_{\text{LSB}}} \]

\[ \text{INL} = \max_{2 \leq k \leq N-2} \{ |\text{INL}_k| \} \]

1 \leq k \leq N-2

Often expressed in LSB

For an ideal ADC, INL is ideally 0.
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

\[ \text{INL}_k = \frac{x_{Tk} - x_{FT_k}}{x_{LSB}} \quad 1 \leq k \leq N-2 \]

\[ \text{INL} = \max_{2 \leq k \leq N-2} \{ |\text{INL}_k| \} \]

- INL is often the most important parameter of an ADC
- INL_1 and INL_{N-1} are 0 (by definition)
- There are N-3 elements in the set of INL_k that are of concern
- INL is a random variable at the design stage
- INL_k is a random variable for 0<k<N-1
- INL_k and INL_{k+j} are correlated for all k,j (not incl 0, N-1) for most architectures
- Fit Line (for cont INL) and uniformly spaced break pts (breakpoint INL) are random variables
- INL is the N-3 order statistic of a set of N-3 correlated random variables (breakpoint INL)
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

\[ \text{INL}_k = \frac{x_{T_k} - x_{F_T}}{x_{LSB}} \quad 1 \leq k \leq N-2 \]

\[ \text{INL} = \max_{2 \leq k \leq N-2} \{ |\text{INL}_k| \} \]

• At design stage, INL characterized by standard deviation of the random variable
• Closed-form expressions for INL almost never exist because PDF of order statistics of correlated random variables is extremely complicated
• Simulation of INL very time consuming if n is very large (large sample size required to establish reasonable level of confidence)
  - Model parameters become random variables
  - Process parameters affect multiple model parameters causing model parameter correlation
  - Simulation times can become very large
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

\[ \text{INL}_k = \frac{x_{Tk} - x_{FTl}}{x_{LSB}} \quad 1 \leq k \leq N-2 \]

\[ \text{INL} = \max \{ |\text{INL}_k| \} \]

\[ 2 \leq k \leq N-2 \]

- INL can be readily measured in laboratory but often dominates test costs because of number of measurements needed when \( n \) is large
- Expected of \( \text{INL}_k \) at \( k = (N-1)/2 \) is largest for many architectures
- Major effort in ADC design is in obtaining an acceptable yield
INL-based ENOB

Consider initially the continuous INL definition for an ADC where the INL of an ideal ADC is \( X_{\text{LSB}}/2 \)

Assume

\[
\text{INL} = \theta X_{\text{REF}} = \nu X_{\text{LSBR}}
\]

where \( X_{\text{LSBR}} \) is the LSB based upon the defined resolution

Define the LSB by

\[
X_{\text{LSB}} = \frac{X_{\text{REF}}}{2^{n_{\text{EQ}}}}
\]

Thus

\[
\text{INL} = \theta 2^{n_{\text{EQ}}} X_{\text{LSB}}
\]

Since an ideal ADC has an INL of \( X_{\text{LSB}}/2 \), express INL in terms of ideal ADC

\[
\text{INL} = \left[ \theta 2^{(n_{\text{EQ}}+1)} \right] \left( \frac{X_{\text{LSB}}}{2} \right)
\]

Setting term in [ ] to 1, can solve for \( n_{\text{EQ}} \) to obtain

\[
\text{ENOB} = n_{\text{EQ}} = \log_2 \left( \frac{1}{2\theta} \right) = n_R - 1 - \log_2 (\nu)
\]

where \( n_R \) is the defined resolution
INL-based ENOB

$$\text{ENOB} = n_R - 1 - \log_2 (v)$$

Consider an ADC with specified resolution of $n_R$ and INL of $v$ LSB

<table>
<thead>
<tr>
<th>$v$</th>
<th>ENOB</th>
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<tbody>
<tr>
<td>$\frac{1}{2}$</td>
<td>$n$</td>
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End of Lecture 28