EE 435

Lecture 33

DAC Design
- The String DAC

Parasitic Capacitances
DAC Architectures (Nyquist Rate)

Types

• Voltage Scaling
  – Resistor String DACs (string DACs)
  – Interpolating

• Current Steering
  – Binarily Weighted Resistors
  – R-2R Ladders
  – Current Source Steering
    • Thermometer Coded
    • Binary Weighted
    • Segmented

• Charge Redistribution
  – Switched Capacitor

• Serial
  – Algorithmic
  – Cyclic or Re-circulating
  – Pipelined

• Integrating
• Resistor Switching
• MDACs (multiplying DACs)
DAC Architectures

Structures

• Hybrid or Segmented
• Mode of Operation
  – Current Mode
  – Voltage Mode
  – Charge Mode
• Self-Calibrating
  – Analog Calibration
    • Foreground
    • Background
  – Digital Calibration
    • Foreground
    • Background
  – Dynamic Element Matching
• Laser of Link Trimmed
• Thermometer Coded or Binary
• Radix 2 or non-radix 2
• Inherently Monotone
DAC Architectures

- Type of Classification may not be unique nor mutually exclusive
- Structure is not mutually exclusive
- All approaches listed are used (and probably some others as well)
- Some are much more popular than others
  - Popular Architectures
    - Resistor String (interpolating)
    - Current Source Steering (with segmentation)
- Many new architectures are possible and some may be much better than the best currently available
- All have perfect performance if parasitic and matching performance are ignored!
- Major challenge is in determining appropriate architecture and managing the parasitics
Nonideal Effects of Concern

- Matching
- Parasitic Capacitances
  (including Charge injection)
- Loading
- Nonlinearities
- Interconnect resistors
- Noise
- Slow and plagued by jitter
- Temperature Effects
- Aging
- Package stress

Review from last lecture

•


Data Converter Design Strategies

- There are many different DAC and ADC architectures that have been proposed and that are in widespread use today
- Almost all work perfectly if all components are ideal
- Most data converter design work involves identifying the contributors to nonideal performance and finding work-arounds to these problems
- Some architectures are more difficult to find work-arounds than others
- All contributors to nonidealities that are problematic at a given resolution of speed level must be identified and mitigated
- The effects of not identifying nonidealities generally fall into one of two categories
  - Matching-critical nonidealities (degrade yield)
  - Component nonlinearities (degrade performance even if desired matching is present)

Review from last lecture.
Identifying Problems/Challenges and Clever/Viable Solutions

- Many problems occur repeatedly so should recognize what they are
- Identify clever solutions to basic problems – they often are useful in many applications
- Don’t make the same mistake twice!

The problem:

The perceived solution:

The practical or clever solution:

The List Keeper!
R-String DAC

Basic R-String DAC
R-String DAC

If all components are ideal, performance of the R-string DAC is that of an ideal DAC!

Key Properties of R-String DAC

- One of the simplest DAC architectures
- R-string DAC is inherently monotone

Possible Limitations or Challenges

- Binary to Thermometer Decoder (BTTD) gets large for n large
- Logic delays in BTTD may degrade performance
- Matching of the resistors may not be perfect
  - Local random variations
  - Gradient effects
- How can switches be made?
R-String DAC

R-String DAC with MOS switches

Possible Limitations:

Switch impedance is not 0

Switch may not even turn on at all if $V_{\text{REF}}$ is large

Switch impedance is input-code dependent

Time constants are input-code dependent

Transition times are previous-code dependent

$C_L$ has $2^n$ diffusion capacitances so can get very large

- Mismatch of resistors
  - local random variation
  - gradient effects

Decoder can get very large for $n$ large

Routing of the $2n$ switch signals can become very long and consume lots of area
R-String DAC

- Review from last lecture.
Parasitic Capacitors in MOSFET

(will initially consider two)
Parasitic Capacitors in MOSFET
Parasitic Capacitors in MOSFET

Recall that pn junctions have a depletion region!
Parasitic Capacitors in MOSFET

pn junction capacitance

\[ C = \frac{C_{JOA} A}{1 - \left( \frac{V_{FB}}{\phi_B} \right)^m} \]

For \( V_{FB} < \phi_B / 2 \)
Parasitic Capacitors in MOSFET

pn junction capacitance

The bottom and the sidewall:
Parasitic Capacitors in MOSFET

pn junction capacitance

For a pn junction capacitor

\[ C_J = C_{BOT} A + C_{SW} P \]

\[ C_{BOT} = \frac{C_{BOT} A}{(1 - \frac{V_{FB}}{\phi_B})^m} \]

\[ C_{SW} = \frac{C_{SW} P}{(1 - \frac{V_{FB}}{\phi_B})^m} \]
Question

• Are the parasitic capacitors relevant?
Observation

- Parasitic Capacitors are Small

Consider a minimum-sized transistor
## Process Parameters from AMI 0.5u Process

### Process Parameters

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>N+ACTV</th>
<th>P+ACTV</th>
<th>POLY</th>
<th>PLY2_</th>
<th>HR</th>
<th>POLY2</th>
<th>MTL1</th>
<th>MTL2</th>
<th>UNITS</th>
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<td>101.9</td>
<td>21.6</td>
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<td>0.09</td>
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<td>Gate Oxide Thickness</td>
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### Process Parameters

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>MTL 3</th>
<th>N|PLY</th>
<th>N WELL</th>
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</thead>
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<tr>
<td>Sheet Resistance</td>
<td>0.06</td>
<td>822</td>
<td>812</td>
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<tr>
<td>Contact Resistance</td>
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</table>

**Comments:** N\|POLY is N-well under polysilicon.

### Capacitance Parameters

<table>
<thead>
<tr>
<th>CAPACITANCE PARAMETERS</th>
<th>N+ACTV</th>
<th>P+ACTV</th>
<th>POLY</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>N_WELL</th>
<th>UNITS</th>
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<td>87</td>
<td>32</td>
<td>16</td>
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<td></td>
<td>aF/(\mu)m^2</td>
</tr>
<tr>
<td>Area (N+active)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/(\mu)m^2</td>
</tr>
<tr>
<td>Area (P+active)</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/(\mu)m^2</td>
</tr>
<tr>
<td>Area (poly)</td>
<td></td>
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<td>aF/(\mu)m^2</td>
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<td>Area (poly2)</td>
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<td>aF/(\mu)m^2</td>
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<tr>
<td>Area (metal1)</td>
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<td>aF/(\mu)m^2</td>
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<tr>
<td>Area (metal2)</td>
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<td>aF/(\mu)m^2</td>
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<td>247</td>
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<td>72</td>
<td>58</td>
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<td>aF/(\mu)m</td>
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<tr>
<td>Fringe (poly)</td>
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<td>57</td>
<td>39</td>
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<td>aF/(\mu)m</td>
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<td>Fringe (metal1)</td>
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<td></td>
<td></td>
<td>48</td>
<td>34</td>
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<td>aF/(\mu)m</td>
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<tr>
<td>Fringe (metal2)</td>
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<td>Overlap (N+active)</td>
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<td>Overlap (P+active)</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/(\mu)m</td>
</tr>
</tbody>
</table>

\[\lambda = .35 \text{ microns}\]
Size of Capacitances

Gate-Channel Capacitance = $6\lambda^2 \times 2.47\text{fF}/\mu^2 = 1.82\text{fF}$

Source Diffusion-Substrate Capacitance =

$12\lambda^2 \times .424\text{fF}/\mu^2 + 14\lambda \times .315\text{fF}/\mu = .624\text{fF} + 1.54\text{fF} = 2.16\text{fF}$

Note Sidewall Capacitance larger than Bottom Capacitance

Are these negligible?
Are these negligible?

These small capacitors play the dominant role in the speed limitations of most digital circuits.

These small capacitors play a major role in the performance of many linear circuits.

It is essential that these capacitors (parasitic capacitors) be considered and managed when designing most integrated circuits today!
Types of Capacitors

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

2. Operating Region Dependent
   a. Fixed Geometry
   b. Junction
Parasitic Capacitors in MOSFET

Fixed Capacitors
Parasitic Capacitors in MOSFET

Fixed Capacitors

Overlap Capacitors: \( C_{\text{GDO}} \), \( C_{\text{GSO}} \)
### Parasitic Capacitance Summary

<table>
<thead>
<tr>
<th></th>
<th>Cutoff</th>
<th>Ohmic</th>
<th>Saturation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{GS}$</td>
<td>$C_{oxWL_D}$</td>
<td>$C_{oxWL_D}$</td>
<td>$C_{oxWL_D}$</td>
</tr>
<tr>
<td>$C_{GD}$</td>
<td>$C_{oxWL_D}$</td>
<td>$C_{oxWL_D}$</td>
<td>$C_{oxWL_D}$</td>
</tr>
</tbody>
</table>

$L_D$ is a model parameter
Parasitic Capacitors in MOSFET

Fixed Capacitors

Junction Capacitors: $C_{BS1}$, $C_{BD1}$
Parasitic Capacitors in MOSFET

Fixed Capacitors

Overlap Capacitors: $C_{GDO}$, $C_{GSO}$

Junction Capacitors: $C_{BS1}$, $C_{BD1}$
Fixed Parasitic Capacitance
Summary

C\textsubscript{BOT} and C\textsubscript{SW} are model parameters

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<tr>
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<td>(\text{CoxWL}_D)</td>
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<tr>
<td>(C\textsubscript{GD})</td>
<td>(\text{CoxWL}_D)</td>
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</tr>
<tr>
<td>(C\textsubscript{BG})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C\textsubscript{BS})</td>
<td>(C\textsubscript{BS1} = C\textsubscript{BOT}A\textsubscript{S} + C\textsubscript{SW}P\textsubscript{S})</td>
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</tr>
<tr>
<td>(C\textsubscript{BD})</td>
<td>(C\textsubscript{BD1} = C\textsubscript{BOT}A\textsubscript{D} + C\textsubscript{SW}P\textsubscript{D})</td>
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</table>
Parasitic Capacitors in MOSFET Operation Region Dependent
Parasitic Capacitors in MOSFET
Operation Region Dependent -- Cutoff

Cutoff Capacitor: $C_{\text{GBCO}}$
Parasitic Capacitors in MOSFET
Operation Region Dependent -- Cutoff

Note: A depletion region will form under the gate if a positive Gate voltage is applied thus decreasing the capacitance density

Cutoff Capacitor: $C_{GBCO}$
Parasitic Capacitors in MOSFET
Operation Region Dependent and Fixed -- Cutoff

Overlap Capacitors: $C_{GDO}, C_{GSO}$
Junction Capacitors: $C_{BS1}, C_{BD1}$
Cutoff Capacitor: $C_{GBCO}$
Parasitic Capacitance Summary

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<td>$CoxWL_D$</td>
<td>$CoxWL_D$</td>
<td>$CoxWL_D$</td>
</tr>
<tr>
<td>$C_{BG}$</td>
<td>$CoxWL$ (or less)</td>
<td>$C_{BS1} = C_{BOTAS} + C_{SWPS}$</td>
<td>$C_{BS1} = C_{BOTAS} + C_{SWPS}$</td>
</tr>
<tr>
<td>$C_{BS}$</td>
<td>$C_{BOTAS} + C_{SWPS}$</td>
<td>$C_{BD1} = C_{BOTAD} + C_{SWPD}$</td>
<td>$C_{BD1} = C_{BOTAD} + C_{SWPD}$</td>
</tr>
<tr>
<td>$C_{BD}$</td>
<td>$C_{BOTAD} + C_{SWPD}$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Parasitic Capacitors in MOSFET Operation Region Dependent -- Ohmic

Note: The Channel is not a node in the lumped device model so cannot directly include this distributed capacitance in existing models.

Note: The distributed channel capacitance is usually lumped and split evenly between the source and drain nodes.

**Ohmic Capacitor**: $C_{GCH}$, $C_{BCH}$
Parasitic Capacitors in MOSFET
Operation Region Dependent and Fixed -- Ohmic

Overlap Capacitors: $C_{GDO}$, $C_{GSO}$
Junction Capacitors: $C_{BS1}$, $C_{BD1}$
Ohmic Capacitor: $C_{GCH}$, $C_{BCH}$
### Parasitic Capacitance Summary

**Diagram**

- **$C_{GS}$**
- **$C_{GD}$**
- **$C_{BG}$**
- **$C_{BS}$**
- **$C_{BD}$**

**Table**

<table>
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<td>$CoxWL_{D}$</td>
<td>$CoxWL_{D}$</td>
<td>$CoxWL_{D}$</td>
</tr>
<tr>
<td>$C_{BG}$</td>
<td>$CoxWL$ (or less)</td>
<td>$C_{BS1} = C_{BOTA_S} + C_{SWP_S}$</td>
<td>$C_{BS1} = C_{BOTA_S} + C_{SWP_S}$</td>
</tr>
<tr>
<td>$C_{BS}$</td>
<td>$C_{BOTA_S} + C_{SWP_S}$</td>
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<td>$C_{BS1} = C_{BOTA_S} + C_{SWP_S}$</td>
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<tr>
<td>$C_{BD}$</td>
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<td>$C_{BD1} = C_{BOTA_D} + C_{SWP_D}$</td>
<td>$C_{BD1} = C_{BOTA_D} + C_{SWP_D}$</td>
</tr>
</tbody>
</table>
Parasitic Capacitors in MOSFET Operation Region Dependent -- Saturation

Saturation Capacitors: $C_{GCH}, C_{BCH}$

Note: Since the channel is an extension of the source when in saturation, the distributed capacitors to the channel are generally lumped to the source node.
Parasitic Capacitors in MOSFET
Operation Region Dependent and Fixed --Saturation

Overlap Capacitors: $C_{GDO}$, $C_{GSO}$
Junction Capacitors: $C_{BS1}$, $C_{BD1}$
Saturation Capacitors: $C_{GCH}$, $C_{BCH}$
## Parasitic Capacitance Summary

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<td>$C_{oxWL_D} + 0.5C_{oxWL}$</td>
<td>$C_{oxWL_D} + (2/3)C_{oxWL}$</td>
</tr>
<tr>
<td>$C_{GD}$</td>
<td>$C_{oxWL_D}$</td>
<td>$C_{oxWL_D} + 0.5C_{oxWL}$</td>
<td>$C_{oxWL_D}$</td>
</tr>
<tr>
<td>$C_{BG}$</td>
<td>$C_{oxWL}$ (or less)</td>
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<td>0</td>
</tr>
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<td>$C_{BS}$</td>
<td>$C_{BOT_A S} + C_{SW P_S}$</td>
<td>$C_{BOT_A S} + C_{SW P_S} + 0.5WLC_{BOTCH}$</td>
<td>$C_{BOT_A S} + C_{SW P_S} + (2/3)WLC_{BOTCH}$</td>
</tr>
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<td>$C_{BD}$</td>
<td>$C_{BOT_A D} + C_{SW P_D}$</td>
<td>$C_{BOT_A D} + C_{SW P_D} + 0.5WLC_{BOTCH}$</td>
<td>$C_{BOT_A D} + C_{SW P_D}$</td>
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## Parasitic Capacitance Summary

![Diagram of parasitic capacitance](image)

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<td>$C_{GD}$</td>
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<tr>
<td>$C_{BG}$</td>
<td>$C_{oxWL} \text{ (or less)}$</td>
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<tr>
<td>$C_{BS}$</td>
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<td>$C_{BOTAS} + C_{SWPS} + 0.5WLC_{BOTCH}$</td>
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<tr>
<td>$C_{BD}$</td>
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<td>$C_{BOTAD} + C_{SWPD} + 0.5WLC_{BOTCH}$</td>
<td>$C_{BOTAD} + C_{SWPD}$</td>
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R-String DAC

Parasitic Capacitances in Tree Decoder
R-String DAC

Example:

\[ V_3 \]

Assume all C’s initially with 0V
Red denotes \( V_3 \), black denotes 0V, Purple some other voltage

Previous-Code Dependent Settling
R-String DAC

Transition from \(<010>\) to \(<101>\)

Assume all C’s initially with 0V
Red denotes \(V_3\), green denotes \(V_6\), black denotes 0V, Purple some other voltage

Previous-Code Dependent Settling

Example:
\(V_3\) to \(V_6\)
R-String DAC

Transition from <010> to <101>  

White boxes show capacitors dependent upon previous code <010>

Assume all C’s initially with 0V
Red denotes $V_3$, green denotes $V_6$, black denotes 0V, Purple some other voltage

Previous-Code Dependent Settling
Do the resistors that form part of PTL dissipate any substantial power?

No because only one will be conducting for any DAC output

Single transistor used at each marked intersection to for PTL AND gates

Tree-Decoder in Digital Domain

Tree Decoder

Decoder

b3  b3  b2  b2  b1  b1

R-String DAC
R-String DAC

$V_{\text{REF}}$  $X_{\text{IN}}$  $V_{\text{OUT}}$

Decoder

$b_1$  $b_1$  $b_2$  $b_2$  $b_3$  $b_3$

Tree Decoder
R-String DAC

![Diagram of R-String DAC](image)

\[ V_{RFF} \]

\[ X_{IN} \]

\[ n = n_1 : n_2 \]

\[ V_{OUT} \]
Sometimes termed sub-divider, sub-range or dual-string DAC
R-String DAC

\[ X_{\text{IN}} \]

\[ n = n_1 : n_2 \]

\[ V_{\text{RFF}} \]

\[ V_{\text{OUT}} \]

Interpolator
R-String DAC

\[ X_{IN} \]

\[ n = n_1 : n_2 \]

\[ V_{RFF} \]

\[ V_{OUT} \]

\[ V_D \]

\[ I_{INT} \]

Interpolator
End of Lecture 33