EE 435

Lecture 34

DAC Design

• The String DAC
• Current Steering DACs
R-String DAC

\[ X_{IN} \]

\[ n = n_1 : n_2 \]

\[ V_RFF \]

\[ V_{OUT} \]
Sometimes termed sub-divider, sub-range or dual-string DAC
R-String DAC

Review from last lecture.

\[ V_{\text{RFF}} \]

\[ n = n_1:n_2 \]

\[ X_{\text{IN}} \]

\[ n_1 \]

\[ n_2 \]

\[ V_{\text{OUT}} \]
R-String DAC

Review from last lecture.
R-String DAC

Review from last lecture.
Matching Properties of Circuit Components

\[ \frac{\sigma^2_R}{R_N} \approx \frac{A_{\rho N}^2}{WL} \]

\[ \frac{\sigma^2_{C_R}}{C_N} \approx \frac{A_C^2}{A_{TOP}} \]

\[ \frac{\sigma^2_{I_D}}{I_{DN}} \approx \frac{1}{WL} \left( \frac{4}{V_{EB}^3} A_{VT0}^2 + A_{COX}^2 + A_\mu^2 \right) \]
Matching Properties of Circuit Components

\[
\frac{\sigma_R^2}{R_N} \approx \frac{A_{\rho N}^2}{WL}
\]

\[
\frac{\sigma_{CR}^2}{C_N} \approx \frac{A_C^2}{A_{TOP}}
\]

\[
\frac{\sigma_{I_D}^2}{I_{DN}} \approx \frac{1}{WL} \left( \frac{4}{V_{EB}^3} A_{VT0}^2 + A_{COX}^2 + A_{\mu}^2 \right)
\]

- If edge roughness effects are neglected, standard deviation of components proportional to \( \frac{\sigma_X}{X_N} \)
- INL and DNL of most data converters (at low f) depends upon matching characteristics of basic circuit components
- Often INL and DNL proportional to standard deviation
- Each additional bit of ENOB generally requires a factor of 2 reduction in \( \sigma \)
R-String DAC

A 10-b 50-MHz CMOS D/A converter with 75-ω buffer
Abstract-A 10-b 50-MHz digital-to-analog (D/A) converter is presented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy,...

Note Dual Ladder is used!
A 10-b 50-MHz CMOS D/A converter with 75-Ω buffer - Get It@ISU
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A 10-b 50-MHz CMOS D/A Converter with 75-Ω Buffer

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Abstract — A 10-b 50-MHz digital-to-analog (D/A) converter is presented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy, and signal-dependent switch signals reduce high-frequency distortion. The output buffer allows driving 1 Vpp to 75 Ω. The chip consumes 65 mW at maximum clock frequency and a full-swing output signal. The device is processed in a standard 1.6-μm CMOS process with a single 5-V supply voltage.

Current-based circuits dump the complementary part of the signal current to ground: the power supply current is thereby twice the average signal current. If a two-sided terminated transmission line has to be fed by the high-impedance output of the current cell D/A converter, the current should be doubled to obtain the required output swing. In this case, the power supply current is four times the average signal current. A triple video D/A converter
Current-based circuits dump the complementary part of the signal current to ground: the power supply current is thereby twice the average signal current. If a two-sided terminated transmission line has to be fed by the high-impedance output of the current cell D/A converter, the current should be doubled to obtain the required output swing. In this case, the power supply current is four times the average signal current. A triple video D/A converter intended for supplying $1 \, V_{pp}$ to $75 \, \Omega$ will consequently require $80$-mA power supply current.

This paper proposes a trimless 10-b 50-MHz D/A converter based on resistor strings. This D/A converter is well suited to be used together with nearly all reported A/D converters for high speed, as these also use resistor strings to obtain the reference for the comparators. The design improves on the standard single-resistor-string approach by using a dual-ladder architecture [3] in a matrix formation [4], [5]. Several measures have been taken in the ladder to reduce the distortion. The decoding aims at minimizing the number of transistors that switch. The on-chip output buffer allows driving $1 \, V_{pp}$ to $75 \, \Omega$. The inherent voltage output allows driving a two-sided terminated transmission line with a better power efficiency than a current cell D/A converter.

Section II presents the design considerations and chip architecture and Section III shows some measurements on the device. The work is summarized in Section IV.
II. **The Chip Design**

A. *The Ladder Structure*

The voltage dependence and the mutual matching of large-area polysilicon resistors allow the design of a converter with high integral and differential linearity. Basically, the variation in the polysilicon resistance value is determined by its geometry variations: the length and width variations result in local mismatches and the thickness variation gives gradients. Equally sized MOS gates suffer in addition to charge variations in the threshold voltage. However, the design of the D/A converter with a single 1024-tap resistor ladder and sufficiently fast output settling requires tap resistors in the order of 6–10 Ω. The size of such resistors in conventional polysilicon technology is such that accurate resistor matching and consequently linearity become a problem.
End of Lecture 34