EE 435

Lecture 36

DAC Design

Current Steering DACs
Other DAC structures
Switch Implementation Issues

- n-channel
- p-channel
- T-gate
Switch Implementation Issues

- n-channel
- p-channel
- T-gate
Current Steering DACs
Current Steering DACs

Inherently Insensitive to Nonlinearities in Switches and Resistors
Current Steering DACs

Inherently Insensitive to Nonlinearities in Switches and Resistors
Smaller ON resistance and less phase-shift from clock edges
Current Steering DACs

Binary to Thermometer Decoder (all ON)

Transistor Implementation of Switches
Current Steering DACs

Transistor Implementation of Switches

\[ \beta = \frac{R_{CELL}}{k} \left( \frac{1}{R_{CELL} + R_F} + \frac{1}{R_{CELL} + kR_F} \right) = \frac{R_{CELL}}{R_{CELL} + kR_F} \]

If \( V_{OUTFS} = V_{REF} \), \( R_{CELL} = NR_F \)

\[ 0.5 < \beta \leq 1 \]
Current Steering DACs

\[ R \]
\[ d_k \]
\[ I_1 \]
\[ C_P \]

 Binary to Thermometer Decoder (p/n)

\[ V_{REF} \]
\[ R \]
\[ S_1 \]
\[ I_1 \]
\[ S_2 \]
\[ I_2 \]
\[ \cdots \]
\[ S_N \]
\[ I_N \]
\[ R_f \]
\[ V_{OUT} \]

\[ \beta \] Compensation

\[ C_P \] Compensation

Differential Output

\[ I_T - I_{SUM} \]

\[ d_k \]
\[ \bar{d}_k \]

DUMP
Current Steering DACs

Binary-Weighted Resistor Arrays
Current Steering DACs

Binary-Weighted Resistor Arrays

Actual layout of resistors is very important
Current Steering DACs

Segmented architectures are widely used
• Offers good tradeoffs between decoder complexity and linearity
• Thermometer Coded Array must be accurate to the n-bit level