EE 435

Lecture 37

DAC Design
  Current Steering DACs
  Charge Redistribution DACs
Current Steering DAC

\[ I_{\text{OUT}} = kI \]
Current Steering DAC

\[ I_{\text{OUT}} = kl \]

Review from last lecture.
Current Steering DAC

- Binary to Thermometer
- Thermometer Coded Array
- Binary Coded Array

• Review from last lecture.
Current Steering DAC

\[ I_{\text{OUT}} = kI \]

- Review from last lecture.

- Current Steering DAC diagram with symbols and equations.
Current Steering DAC

Review from last lecture

\[ I_{OUT} = kI \]
Current Steering DAC

\[ I_{OUT} = kI \]

\[ n \]

\[ V_{OUT} \]

\[ V_{DD} \]

\[ V_{XX} \]

\[ V_{YY} \]

\[ M_1 \]

\[ M_2 \]

\[ M_3 \]

\[ M_4 \]

Cascode Current Source (Mirror)

Differential Amplifier (Analog)
Current Steering DAC

Binary to Thermometer Decoder (all ON)

\[ I_{\text{OUT}} = kI \]

\[ V_{\text{DD}} \]

\[ V_{\text{XX}} \]

\[ V_{\text{YY}} \]

\[ d_k \]

\[ \tilde{d}_k \]

\[ R_F \]

\[ V_{\text{OUT}} \]

\[ C_{P1} \]

\[ C_{P2} \]
Current Steering DAC

\[ V_{DD} \]

\[ V_{XX} \]

\[ V_{YY} \]

\[ d_1 \]

\[ d_2 \]

\[ d_{N-1} \]

Binary to Thermometer Decoder (all ON)

\[ \text{I}_{OUT} = kI \]

\[ R_F \]

\[ V_{OUT} \]

\[ V_{XX} \]

\[ V_{YY} \]

\[ V_{DD} \]

\[ C_{P1} \]

\[ C_{P2} \]

\[ M_1 \]

\[ M_2 \]

\[ M_3 \]

\[ M_4 \]

\[ V_1 \]

\[ V_2 \]

\[ I_T \]

\[ I_{D1} \]

\[ I_{D2} \]
Current Steering DAC with Supply Independent Biasing

If transistors on top row are all matched, \( I_X = \frac{V_{REF}}{R} \)

Thermometer coded structure (requires binary to thermometer decoder)

\[
I_A = \left( \frac{V_{REF}}{R} \right)^{N-1} \sum_{i=0}^{N-1} d_i
\]

Provides Differential Output Currents
Current Steering DAC with Supply Independent Biasing

If transistors on top row are all matched, \( I_X = V_{\text{REF}}/R \)

\[
V_A = \left( -V_{\text{REF}} \frac{R_A}{R} \right)^{N-1} \sum_{i=0}^{N-1} d_i
\]

Provides Differential Output Voltages
Current Current Steering DAC with Supply Independent Biasing

If transistors on top row are binary weighted

\[ I_A = \left( \frac{V_{REF}}{R} \right)^{n-1} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}} \]

Provides Differential Output Currents
Matching is Critical in all DAC Considered

Obtaining adequate matching remains one of the major challenges facing the designer!
Dynamic Current Source Matching

- Correct charge is stored on C to make all currents equal to $I_{\text{REF}}$
- Does not require matching of transistors or capacitors
- Requires refreshing to keep charge on C
- Form of self-calibration
- Calibrates current sources one at a time
- Current source unavailable for use while calibrating
- Can be directly used in DACs (thermometer of binary coded)

Often termed “Current Copier” or “Current Replication” circuit
Dynamic Current Source Matching

Extra current source can be added to facilitate background calibration
A charge redistribution circuit

Clocks are complimentary non-overlapping
A charge redistribution circuit

During phase $\phi_1$

$$Q_{\phi_1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase $\phi_2$

$$\frac{Q_{\phi_1}}{CF} = V_{OUT}$$

$$\frac{CV_{IN}}{CF} = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{C}{CF}$$

Serves as a noninverting amplifier
Gain can be very accurate
Output valid only during $\Phi_2$
Another charge redistribution circuit
A charge redistribution circuit

During phase $\phi_1$

$$Q_{\phi_1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase $\phi_2$

$$-\frac{Q_{\phi_1}}{C_F} = V_{OUT}$$

$$-\frac{CV_{IN}}{C_F} = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{C}{C_F}$$

Serves as a inverting amplifier
Gain can be very accurate
Output valid only during $\Phi_2$
A charge redistribution circuit

An over-sampled ADC (single-bit quantizer)
A charge redistribution DAC

\[ C_F = 2^n C \]

\[ V_{\text{REF}} \]

\[ V_{\text{OUT}} \]

\[ C_X \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_{1A} \]

\[ \phi_{2A} \]

C\textsubscript{X} does some good things
(mitigates V\textsubscript{OS}, 1/f noise and finite gain errors)

Will not consider CX affects at this time
A charge redistribution DAC

During phase $\phi_1$

$$Q_{\phi_1} = V_{\text{REF}} \sum_{i=0}^{n-1} d_i \cdot 2^i C$$

$$Q_{CF} = 0$$

During phase $\phi_2$

$$V_{\text{OUT}}(\phi_2) = \frac{1}{C_F} Q_{\phi_1}$$

$$V_{\text{OUT}}(\phi_2) = \frac{1}{2^n C} V_{\text{REF}} \sum_{i=0}^{n-1} d_i \cdot 2^i C$$

$$V_{\text{OUT}}(\phi_2) = V_{\text{REF}} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$
Analog to Digital Converters

\[ \mathcal{X}_{\text{IN}} \xrightarrow{\text{ADC}} \mathcal{X}_{\text{OUT}} \]

\[ \bar{\mathcal{X}}_{\text{OUT}} \]

\[ C_0 <0 0 0> \]
\[ C_1 <0 0 1> \]
\[ C_2 <0 1 0> \]
\[ C_3 <0 1 1> \]
\[ C_4 <1 0 0> \]
\[ C_5 <1 0 1> \]
\[ C_6 <1 1 0> \]
\[ C_7 <1 1 1> \]

\[ \mathcal{X}_{\text{REF}} - \mathcal{X}_{\text{LSB}} \]
Analog to Digital Converters

The conversion from analog to digital in ALL ADCs is done with comparators.

ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects.
Nyquist Rate

\[ X_{IN}(t) \rightarrow \text{Nyquist-Rate ADC} \rightarrow X_{OUT}(kT) \]

\[ X_{CL} \]

\[ T_{SIG} \]

Sampling Clock
Nyquist Rate

Sampling Clock

$T_{\text{SIG}}$
Over-sampling ratios of 128:1 or 64:1 are common. Dramatic reduction in quantization noise effects. Limited to relatively low frequencies.
ADC Types

Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time
Nyqyist Rate Usage Structures

![Graph showing the Nyquist rate usage structures with Speed on the x-axis and Resolution on the y-axis. The graph contains regions for SAR, Pipeline, and Flash.]
End of Lecture 37