EE 435

Lecture 38

DAC Design

• The String DAC
R-String DAC

\[ X_{IN} \]

\[ n = n_1:n_2 \]

\[ V_{RFF} \]

\[ V_{OUT} \]
Sometimes termed sub-divider, sub-range or dual-string DAC
R-String DAC

\[ n = n_1 : n_2 \]

\[ V_{RFF} \]

\[ V_{\text{OUT}} \]
R-String DAC

\[ V_{RFF} \]

\[ n = n_1 : n_2 \]

\[ V_{OUT} \]

Interpolator
R-String DAC

\[ X_{IN} \]

\[ n = n_1 : n_2 \]

\[ V_{RFF} \]

\[ V_{OUT} \]

Interpolator

\[ I_{INT} \]

\[ V_{DD} \]
Matching Properties of Circuit Components

\[ \sigma_R^2 \approx \frac{A_{\rho N}^2}{WL} \]

\[ \sigma_C^2 \approx \frac{A_C^2}{A_{TOP}} \]

\[ \sigma_{I_b}^2 \approx \frac{1}{WL} \left( \frac{4}{V_{EB}^3} A_{VT0}^2 + A_{Cox}^2 + A_{\mu}^2 \right) \]
Matching Properties of Circuit Components

If edge roughness effects are neglected, standard deviation of components proportional to $\sigma_{X}^{2}/X_{N}^{2}$.

INL and DNL of most data converters (at low f) depends upon matching characteristics of basic circuit components.

Often INL and DNL proportional to standard deviation.

Each additional bit of ENOB generally requires a factor of 2 reduction in $\sigma$. Each additional bit of ENOB generally requires a factor of 4 increase in area in matching critical circuits!!
R-String DAC

V_{REF}

LSB Analog MUX

MSB Row Decoder

V_{OUT}
R-String DAC

A 10-b 50-MHz CMOS D/A converter with 75-Ω buffer


Abstract-A 10-b 50-MHz digital-to-analog (D/A) converter is presented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy, ...

Note Dual Ladder is used!
A 10-b 50-MHz CMOS D/A converter with 75-Ω buffer


Abstract — A 10-b 50-MHz digital-to-analog (D/A) converter is presented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy, and signal-dependent switch signals reduce high-frequency distortion. The output buffer allows driving 1 Vpp to 75 Ω. The chip consumes 65 mW at maximum clock frequency and a full-swing output signal. The device is processed in a standard 1.6-μm CMOS process with a single 5-V supply voltage.

Current-based circuits dump the complementary part of the signal current to ground: the power supply current is thereby twice the average signal current. If a two-sided terminated transmission line has to be fed by the high-impedance output of the current cell D/A converter, the current should be doubled to obtain the required output swing. In this case, the power supply current is four times the average signal current. A triple video D/A converter
End of Lecture 38