EE 435

Lecture 39

ADC Design
Data Converter Type Chart

Review from last lecture.

Oversampled

Nyquist
ADC Types

Nyquist Rate
- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled
- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time
Nyqyist Rate Usage Structures

- SAR
- Pipeline
- Flash

Review from last lecture.
• DAC Controller may be simply U/D counter
• SAR ADC will have no missing codes if DAC is monotone
• Not very fast but can be small
Flash ADC

\[ V_{\text{REF}} \] \quad \text{R} \quad \text{R} \quad \text{R} \quad \text{R} \quad \text{R} \quad V_{\text{IN}} \]

\[ \cdots \]

\[ \text{d}_k \]

\[ \text{Encoder} \]

\[ X_{\text{OUT}} \]

\[ n \]

\[ \text{CL} \]
Clocked Comparator

Regenerative Feedback

Large offset voltage (100mV or more)
Flash ADC with Front-End S/H
Flash ADC Summary

Flash ADC
- Very fast
- Simple structure
- Usually Clocked
- Bubble Removal Important
- Seldom over 6 or 7 bits of resolution
Clocked Comparator

Preamplifier with offset compensation

- Ideally removes all offset effects
- May not have a large enough gain
- Regenerative latch often used
Clocked Comparator

Preamplifier with offset compensation and regenerative latch

Gain of preamplifier may still not be large enough
Flash ADC Summary

Flash ADC

Very fast
Simple structure
Usually Clocked
Bubble Removal Important
Seldom over 6 or 7 bits of resolution

- Flash ADC has some really desirable properties (simple and fast)
- Wouldn’t it be nice if we could derive most of the benefits of the FLASH ADC without the major limitations

To be practical at higher resolution, must address the major limitation of the FLASH ADC

Major Limitation of FLASH ADC at higher resolutions?

Number of comparators increases geometrically --- \(2^n\)
ADC Types

Nyquist Rate
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Over-Sampled
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All have comparable conversion rates
Basic approach in all is very similar
Two-Step Flash ADC

Can operate asynchronously (either after first S/H or even w/o S/H)
Two-Step Flash ADC with Interstage Gain

S/H

Flash ADC$_1$

DAC

A

Flash ADC$_2$

Digital Assembler

X$_{IN}$

C$_{LK1}$

n$_1$

n

n$_2$

C$_{LK2}$

MSB

LSB

X$_{OUT}$
Three-Step Flash ADC with Interstage Gain and S/H

![Three-Step Flash ADC with Interstage Gain and S/H Diagram]
Three-Step Flash ADC with Interstage Gain

[Diagram of the three-step flash ADC with interstage gain, showing the signal flow and components.]
Pipelined ADC

$X_{IN}$ → S/H → Stage 1 → $r_1$ → Stage 2 → $r_2$ → ... → Stage k → $r_k$ → ... → Stage m → $r_m$

$X_{OUT} = <n_1:n_2:...:n_m>$
Pipelined ADC

- **Stage 1**: \( n_1 \) \( r_1 \)
- **Stage 2**: \( n_2 \) \( r_2 \)
- **Stage k**: \( n_k \) \( r_k \)
- **Stage m**: \( n_m \) \( r_m \)

**Shift Register**

- \(<b_m>\), \(<b_{k-1}>\), \(<b_2>\), \(<b_1>\)

**Connections**

- Input: \( X_{IN} \) to \( S/H \)
- Clock: \( C_{LK} \) to inputs
- Output: \( X_{OUT} \)
Pipelined ADC Stage $k$

Pipeline Stage

$X_{IN_k}$ $+$ $A_k$ $S/H_k$ $X_{OUT_k}$

ADC$_k$, DAC$_k$, $n_k$, $d_k$, $V_{REF}$, $C_{LK}$
Pipelined ADC Stage $k$

Pipeline Stage

Usually Realized as Single SC Block
Pipelined ADC Stage $k$

Usually Realized as Flash ADC
(often simple comparator if $n_k=1$)
Pipelined ADC Stage $k$

Pipeline Stage for 1 bit/stage

$X_{INk}$

$ADC_k$

$DAC_k$

$V_{REF}$

$S/H_k$

$X_{OUTk}$

$d_k$

$V_{IN}$

$V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & \text{if } V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & \text{if } V_{IN} > 0 
\end{cases}$
Transfer Characteristics for 1 bit/stage

\[ V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & V_{IN} > 0 
\end{cases} \]
Consider the following circuit

\[ V_{IN} \rightarrow \Phi_1 \rightarrow C_2 \rightarrow \Phi_1 \rightarrow C_1 \rightarrow V^+ \rightarrow V_{OUT} \]

\[ V_X \rightarrow \Phi_2 \]

\[ \Phi_1 \]

\[ \Phi_2 \]

\[ T \]
Consider the following circuit

During $\Phi_1$
Consider the following circuit

During $\Phi_1$

\[ Q_1 = C_1 \left( V_{IN} - V^+ \right) \]
\[ Q_2 = C_2 \left( V_{IN} - V^+ \right) \]
Consider the following circuit

During $\Phi_2$
Consider the following circuit

During $\Phi_2$

Define $Q_{1T}$ to be the charge transferred from $C_1$ during phase $\Phi_2$

$$Q_{1T} = C_1 (V_{IN} - V^+) - C_1 (V_X - V^+) = C_1 (V_{IN} - V_X)$$

Define $Q_{2F}$ to be the total charge on $C_2$ during phase $\Phi_2$

$$Q_{2F} = Q_2 + Q_{1T} = C_2 (V_{IN} - V^+) + C_1 (V_{IN} - V_X) = (C_1 + C_2) V_{IN} - C_2 V^+ - C_1 V_X$$
Consider the following circuit

During $\Phi_2$

$$V_{OUT} = \frac{Q_{2F}}{C_2} = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - V^+ - \frac{C_1}{C_2}V_X$$

$$V_{OUTF} = V_{C2F} + V^+ = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2}V_X$$
Consider the following circuit

\[
V_{\text{OUTF}} = \left(1 + \frac{C_1}{C_2}\right)V_{\text{IN}} - \frac{C_1}{C_2}V_X
\]

If \(C_1 = C_2 = C\) and \(V_X = -\frac{V_{\text{REF}}}{2}\)

\[
V_{\text{OUTF}} = 2V_{\text{IN}} + \frac{V_{\text{REF}}}{2}
\]
Consider the following circuit

\[ V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2}V_X \]

Likewise

If \( C_1 = C_2 = C \) and \( V_X = \frac{V_{REF}}{2} \)

\[ V_{OUTF} = 2V_{IN} - \frac{V_{REF}}{2} \]
Observe

\[ V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & \text{if } V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & \text{if } V_{IN} > 0 
\end{cases} \]
1-bit/Stage Pipeline Implementation

\[ V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & V_{IN} > 0 
\end{cases} \]
1-bit/Stage Pipeline Implementation
Interpolating ADC

- Amplifiers are finite-gain saturating
- Shown for 4-bit
- Clocked comparators usually regenerative
- Reduces Offset Requirements for Comparators
Cyclic (Algorithmic) ADC

- Re-use Pipelined Stage
- Small amount of hardware
- Effective thru-put decreases
References
Types of References

- Voltage References
- Current References
- Time References
- ....
Reference Circuit
Voltage Reference

Voltage Reference Circuit

$V_{BIAS}$

$V_{REF}$

$V_{REF}$
Current Reference

$V_{BIAS} \rightarrow \text{Current Reference Circuit} \rightarrow I_{REF}$

$I_{REF}$
Desired Properties of References

- Accurate
- Temperature Stable
- Time Stable
- Insensitive to $V_{BIAS}$
- Low Output Impedance (voltage reference)
- Floating
- Small Area
- Low Power Dissipation
- Process Tolerant
- Process Transportable
Desired Properties of References

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Similar properties desired in other references
Consider Voltage References

Popular Voltage “Reference”

\[ I_{D1} = \frac{\mu C_{OX} W_1}{2L_1} (V_{GS1} - V_{T1})^2 \]

\[ I_{D2} = \frac{\mu C_{OX} W_2}{2L_2} (V_{GS2} - V_{T2})^2 \]

\[ V_{T1} = V_{T0} + \gamma \left( \sqrt{\phi + V_{REF}} - \sqrt{\phi} \right) \]

\[ V_{DD} - V_{REF} - V_{T1} = \sqrt{\frac{W_2L_1}{W_1L_2}} (V_{REF} - V_{T2}) \]

If matching assumed and \( \gamma \) effects neglected

\[ V_{REF} = \frac{V_{DD} - V_{T0} \left( 1 - \sqrt{\frac{W_2L_1}{W_1L_2}} \right)}{1 + \sqrt{\frac{W_2L_1}{W_1L_2}}} \]
Consider Voltage References

\[ V_{\text{REF}} = \frac{V_{DD} - V_{T0} \left(1 - \frac{W_2}{W_1} \sqrt{L_1} \right)}{1 + \frac{W_2}{W_1} \sqrt{L_1}} \]

If matching assumed and \( \gamma \) effects neglected

Popular Voltage “Reference”

Uses as a reference limited to biasing and even for this may not be good enough!

Dependent upon \( V_{DD}, V_{T0}, \) matching, process variations, \( \gamma \)

Termed a \( V_{DD}, V_{T} \) reference

Does not satisfy key properties of voltage references
Consider Voltage References

V_{DD}, V_T reference

\[ V_{REF} = \frac{V_{DD} - V_{T0} \left( 1 - \sqrt{\frac{W_2L_1}{W_1L_2}} \right)}{1 + \sqrt{\frac{W_2L_1}{W_1L_2}}} \]

Observation – Variables with units Volts needed to build any voltage reference
Voltage References

Observation – Variables with units Volts needed to build any voltage reference

What variables available in a process have units volts?

What variables which have units volts satisfy the desired properties of a voltage reference?

How can a circuit be designed that “expresses” the desired variables?
Voltage References

Observation – Variables with units Volts needed to build any voltage reference

What variables available in a process have units volts?

$V_{DD}$, $V_T$, $V_{BE}$ (diode), $V_Z$, $V_{BE}$, $V_t$  ???

What variables which have units volts satisfy the desired properties of a voltage reference?

How can a circuit be designed that “expresses” the desired variables?
End of Lecture 39