EE 435
Lecture 39
DAC Design
Current Steering DACs

Segmented Resistor Arrays

Review from last lecture.
Current Steering DACs

\[ V_{\text{REF}} \]

\[ \frac{R}{2R} \quad \frac{R}{2R} \quad \frac{R}{2R} \quad \frac{R}{2R} \]

\[ b_1 \quad b_2 \quad b_3 \quad b_4 \]

\[ R_{F} \]

\[ V_{\text{OUT}} \]

R-2R Resistor Arrays

Review from last lecture.
Another R-2R DAC
Current Steering DAC

\[ I_{OUT} = kI \]
Current Steering DAC

\[ I_{OUT} = kI \]
Current Steering DAC

- Binary to Thermometer
- Thermometer Coded Array
- Binary Coded Array

Signals:
- $X_{MSB}$
- $n_1$
- $V_{XX}$
- $X_{LSB}$
- $n_2$
- $I_{OUT}$
- $V_{OUT}$
- $R_F$
Current Steering DAC

\[ I_{OUT} = kI \]

\[ I = d_k \]

\[ V_{XX} \]

\[ V_{DD} \]
Current Steering DAC

\[ I_{\text{OUT}} = kI \]

Binary to Thermometer Decoder (all ON)

\[ V_{XX} \]

\[ V_{DD} \]

\[ d_k \]

\[ R_F \]

\[ n \]

\[ V_{OUT} \]

\[ C_P \]
Current Steering DAC

- Binary to Thermometer Decoder (all ON)
- $I_{OUT} = kI$
- $I_{OUT} = \sum d_i I$
- Cascode Current Source (Mirror)
- Differential Amplifier (Analog)
Current Steering DAC
Current Steering DAC

\[ I_{\text{OUT}} = kI \]

\[ I_D1 \rightarrow I_D2 \]

\[ V_1 \rightarrow M_1 \rightarrow M_2 \rightarrow V_2 \]

\[ I_T \]

\[ \sqrt{2} V_{\text{EB}} \rightarrow \sqrt{2} V_{\text{EB}} \]
Current Steering DAC with Supply Independent Biasing

If transistors on top row are all matched, \( I_X = V_{\text{REF}} / R \)

Thermometer coded structure (requires binary to thermometer decoder)

\[
I_A = \left( \frac{V_{\text{REF}}}{R} \right)^{N-1} \sum_{i=0}^{N-1} d_i
\]

Provides Differential Output Currents
Current Steering DAC with Supply Independent Biasing

If transistors on top row are all matched, $I_X = V_{REF}/R$

$$V_A = \left(-V_{REF} \frac{R_A}{R}\right)^{N-1} \sum_{i=0}^{N-1} d_i$$

Provides Differential Output Voltages
Current Current Steering DAC with Supply Independent Biasing

If transistors on top row are binary weighted

\[ I_A = \left( \frac{V_{\text{REF}}}{R} \right)^{n-1} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}} \]

Provides Differential Output Currents
Matching is Critical in all DAC Considered

Obtaining adequate matching remains one of the major challenges facing the designer!
Dynamic Current Source Matching

- Correct charge is stored on C to make all currents equal to \( I_{REF} \)
- Does not require matching of transistors or capacitors
- Requires refreshing to keep charge on C
- Form of self-calibration
- Calibrates current sources one at a time
- Current source unavailable for use while calibrating
- Can be directly used in DACs (thermometer of binary coded)

Often termed “Current Copier” or “Current Replication” circuit
Dynamic Current Source Matching

Extra current source can be added to facilitate background calibration
End of Lecture 39
A charge redistribution circuit

Clocks are complimentary non-overlapping
A charge redistribution circuit

During phase $\phi_1$

\[ Q_{\phi_1} = CV_{IN} \]

\[ Q_{CF} = 0 \]

During phase $\phi_2$

\[ \frac{Q_{\phi_1}}{C_F} = V_{OUT} \]

\[ \frac{CV_{IN}}{C_F} = V_{OUT} \]

\[ \frac{V_{OUT}}{V_{IN}} = \frac{C}{C_F} \]

Serves as a noninverting amplifier

Gain can be very accurate

Output valid only during $\Phi_2$
Another charge redistribution circuit
A charge redistribution circuit

During phase $\phi_1$

$$Q_{\phi_1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase $\phi_2$

$$\frac{-Q_{\phi_1}}{C_F} = V_{OUT}$$

$$\frac{-CV_{IN}}{C_F} = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{C}{C_F}$$

Serves as an inverting amplifier

Gain can be very accurate

Output valid only during $\Phi_2$
A charge redistribution DAC

\[ C_F = 2^n C \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ V_{\text{OUT}} \]

\[ C_X \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_{1A} \]

\[ \phi_{2A} \]

\[ T_{\text{CLK}} \]

\[ d_{n-1} \]

\[ d_{n-2} \]

\[ d_1 \]

\[ d_0 \]

\[ V_{\text{REF}} \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_{1A} \]

\[ \phi_{2A} \]

\[ C_X \text{ does some good things} \]

(mitigates \( V_{\text{OS}} \), 1/f noise and finite gain errors)

Will not consider \( C_X \) affects at this time
A charge redistribution DAC

During phase $\phi_1$

$$Q_{\phi_1} = V_{REF} \sum_{i=0}^{n-1} d_i \cdot 2^i C$$

$$Q_{CF} = 0$$

During phase $\phi_2$

$$V_{OUT}(\phi_2) = \frac{1}{C_F} Q_{\phi_1}$$

$$V_{OUT}(\phi_2) = \frac{1}{2^n C} V_{REF} \sum_{i=0}^{n-1} d_i \cdot 2^i C$$

$$V_{OUT}(\phi_2) = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$
End of Lecture 39