Current Steering DAC

Review from last lecture

\[ I_{\text{OUT}} = kI \]
Review from last lecture

Current Steering DAC
Current Steering DAC

Review from last lecture
Current Steering DAC with Supply Independent Biasing

If transistors on top row are all matched, $I_X = V_{REF}/R$

Thermometer coded structure (requires binary to thermometer decoder)

$$I_A = \left(\frac{V_{REF}}{R}\right)^{N-1} \sum_{i=0}^{N-1} d_i$$

Provides Differential Output Currents
Matching is Critical in all DAC Considered

Review from last lecture

Obtaining adequate matching remains one of the major challenges facing the designer!
Dynamic Current Source Matching

• Correct charge is stored on C to make all currents equal to $I_{REF}$
• Does not require matching of transistors or capacitors
• Requires refreshing to keep charge on C
• Form of self-calibration
• Calibrates current sources one at a time
• Current source unavailable for use while calibrating
• Can be directly used in DACs (thermometer of binary coded)

Often termed “Current Copier” or “Current Replication” circuit
A charge redistribution circuit

Clocks are complimentary non-overlapping
A charge redistribution circuit

During phase $\phi_1$

\[ Q_{\phi_1} = CV_{IN} \]

\[ Q_{CF} = 0 \]

During phase $\phi_2$

\[ \frac{Q_{\phi_1}}{C_F} = V_{OUT} \]

\[ \frac{CV_{IN}}{C_F} = V_{OUT} \]

\[ \frac{V_{OUT}}{V_{IN}} = \frac{C}{C_F} \]

Serves as a noninverting amplifier
Gain can be very accurate
Output valid only during $\Phi_2$
Another charge redistribution circuit

\[ \text{V}_{\text{IN}} \quad \phi_1 \quad C \quad \phi_2 \quad \phi_1 \quad \phi_2 \quad \phi_1 \quad V_{\text{OUT}} \]

\[ C_F \]

\[ T_{\text{CLK}} \]

\[ \phi_1 \quad \phi_2 \]
A charge redistribution circuit

During phase $\phi_1$

$$Q_{\phi_1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase $\phi_2$

$$\frac{-Q_{\phi_1}}{C_F} = V_{OUT}$$

$$\frac{-CV_{IN}}{C_F} = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{C}{C_F}$$

Serves as a inverting amplifier

Gain can be very accurate

Output valid only during $\Phi_2$
A charge redistribution circuit

An over-sampled ADC (single-bit quantizer)
A charge redistribution DAC

C\textsubscript{X} does some good things
(mitigates V\textsubscript{OS}, 1/f noise and finite gain errors)

Will not consider CX affects at this time
A charge redistribution DAC

During phase $\phi_1$

$$Q_{\phi_1} = V_{\text{REF}} \sum_{i=0}^{n-1} d_i \cdot 2^i C$$

$$Q_{CF} = 0$$

During phase $\phi_2$

$$V_{\text{OUT}}(\phi_2) = \frac{1}{C_F} Q_{\phi_1}$$

$$V_{\text{OUT}}(\phi_2) = \frac{1}{2^n C} V_{\text{REF}} \sum_{i=0}^{n-1} d_i \cdot 2^i C$$

$$V_{\text{OUT}}(\phi_2) = V_{\text{REF}} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$
Analog to Digital Converters

\[ x_{\text{IN}} \rightarrow \text{ADC} \rightarrow x_{\text{OUT}} \]

\[ \bar{x}_{\text{OUT}} \]

- \( C_7 \) \(<1 1 1>\)
- \( C_6 \) \(<1 1 0>\)
- \( C_5 \) \(<1 1 0>\)
- \( C_4 \) \(<1 0 1>\)
- \( C_3 \) \(<1 0 0>\)
- \( C_2 \) \(<0 1 1>\)
- \( C_1 \) \(<0 1 0>\)
- \( C_0 \) \(<0 0 0>\)

\[ x_{\text{LSB}} \]

\[ x_{\text{REF}} - x_{\text{LSB}} \]
Analog to Digital Converters

The conversion from analog to digital in ALL ADCs is done with comparators.

ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects.
Nyquist Rate

Nyquist-Rate ADC

$X_{\text{IN}}(t)$

$X_{\text{CL}}$

$X_{\text{OUT}}(kT)$

$t$

$T_{\text{SIG}}$

Sampling Clock
Nyquist Rate

Sampling Clock
Over-sampling ratios of 128:1 or 64:1 are common. Dramatic reduction in quantization noise effects is achieved, but it is limited to relatively low frequencies.
ADC Types

Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time
Nyquist Rate Usage Structures

![Diagram showing the usage structures for Nyquist rates. The diagram includes categories such as SAR, Pipeline, and Flash, each represented by distinct regions on a graph that plots speed versus resolution.]
SAR ADC

- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small
End of Lecture 39