Clocked Comparator

Regenerative Feedback

Large offset voltage (100mV or more)
Review from Last Time

Flash ADC with Front-End S/H

$X_{IN}$ → S/H → Flash ADC → $X_{OUT}$

$C_{LK}$
Clocked Comparator

Preamplifier with offset compensation and regenerative latch

Gain of preamplifier may still not be large enough
Two-Step Flash ADC with Interstage Gain

Review from Last Time
Review from Last Time

Three-Step Flash ADC with Interstage Gain
Pipelined ADC

\[ X_{\text{OUT}} = \langle n_1 : n_2 : \ldots : n_m \rangle \]
Pipelined ADC
Pipelined ADC Stage $k$
Pipelined ADC Stage $k$

Pipeline Stage

Usually Realized as Single SC Block

$X_{INk}$

$DAC_k$

$ADC_k$

$n_k$

$d_k$

$V_{REF}$

$A_k$

$S/H_k$

$CLK$

$X_{OUTk}$
Pipeline Stage

Pipelined ADC Stage k

Pipeline Stage

\( X_{\text{IN}k} \)

ADC\(_k\)\(,\ \text{DAC}_k\)

\( n_k \)

\( d_k \)

\( V_{\text{REF}} \)

\( C_{\text{LK}} \)

\( x_{\text{OUT}k} \)

Usually Realized as Flash ADC
(often simple comparator if \( n_k = 1 \))
Pipelined ADC Stage $k$

Pipeline Stage for 1 bit/stage

$\begin{align*}
V_O &= \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & \text{if } V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & \text{if } V_{IN} > 0
\end{cases}
\end{align*}$

Diagram:
- $X_{IN_k}$
- $X_{OUT_k}$
- $V_{REF}$
- $V_{IN}$
- $d_k$
- $C_{LK}$

Components:
- $ADC_k$
- $DAC_k$
- $S/H_k$
Transfer Characteristics for 1 bit/stage

\[ V_O = \begin{cases} 
2V_{\text{IN}} + \frac{V_{\text{REF}}}{2} & \text{if } V_{\text{IN}} < 0 \\
2V_{\text{IN}} - \frac{V_{\text{REF}}}{2} & \text{if } V_{\text{IN}} > 0
\end{cases} \]
Consider the following circuit

\[ V_{IN} \]  \[ V_{OUT} \]

\[ C_1 \]

\[ C_2 \]

\[ \Phi_1 \]

\[ \Phi_2 \]

\[ V_X \]

\[ + \]

\[ T \]
Consider the following circuit

During $\Phi_1$

During $\Phi_2$
Consider the following circuit

During $\Phi_1$

$$Q_1 = C_1 \left( V_{IN} - V^+ \right)$$
$$Q_2 = C_2 \left( V_{IN} - V^+ \right)$$
Consider the following circuit

During $\Phi_2$
Consider the following circuit

\[ Q_1 = C_1 (V_{IN} - V^+) \]
\[ Q_2 = C_2 (V_{IN} - V^+) \]

During \( \Phi_2 \)

Define \( Q_{1T} \) to be the charge transferred from \( C_1 \) during phase \( \Phi_2 \)

\[ Q_{1T} = C_1 (V_{IN} - V^+) - C_1 (V_X - V^+) = C_1 (V_{IN} - V_X) \]

Define \( Q_{2F} \) to be the total charge on \( C_2 \) during phase \( \Phi_2 \)

\[ Q_{2F} = Q_2 + Q_{1T} = C_2 (V_{IN} - V^+) + C_1 (V_{IN} - V_X) = (C_1 + C_2)V_{IN} - C_2 V^+ - C_1 V_X \]
Consider the following circuit

During $\Phi_2$

$$Q_{2F} = (C_1 + C_2) \, V_{IN} - C_2 \, V^+ - C_1 \, V_X$$

$$V_{C2F} = \frac{Q_{2F}}{C_2} = \left(1 + \frac{C_1}{C_2}\right) V_{IN} - V^+ - \frac{C_1}{C_2} \, V_X$$

$$V_{OUTF} = V_{C2F} + V^+ = \left(1 + \frac{C_1}{C_2}\right) V_{IN} - \frac{C_1}{C_2} \, V_X$$
Consider the following circuit

\[ V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2}V_X \]

If \( C_1 = C_2 = C \) and \( V_X = -\frac{V_{REF}}{2} \),

\[ V_{OUTF} = 2V_{IN} + \frac{V_{REF}}{2} \]
Consider the following circuit

\[ V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2}V_X \]

Likewise

If \( C_1 = C_2 = C \) and \( V_X = \frac{V_{REF}}{2} \)

\[ V_{OUTF} = 2V_{IN} - \frac{V_{REF}}{2} \]
Observe

\[
V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & \text{if } V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & \text{if } V_{IN} > 0 
\end{cases}
\]
1-bit/Stage Pipeline Implementation

\[
V_O = \begin{cases} 
2V_{IN} + \frac{V_{REF}}{2} & \text{if } V_{IN} < 0 \\
2V_{IN} - \frac{V_{REF}}{2} & \text{if } V_{IN} > 0 
\end{cases}
\]
1-bit/Stage Pipeline Implementation

$V_{INk}$

$V_{REF}$

ADC

$V_{INk}$

$1$

$d_k$
Interpolating ADC

- Amplifiers are finite-gain saturating
- Shown for 4-bit
- Clocked comparators usually regenerative
- Reduces Offset Requirements for Comparators

![Diagram of Interpolating ADC](image-url)
Cyclic (Algorithmic) ADC

- Re-use Pipelined Stage
- Small amount of hardware
- Effective thru-put decreases
End of Lecture 42