EE 435

Lecture 42

Switched-Capacitor Amplifiers and Filters
Some of the most basic and widely used analog circuits

- **Inverting Amplifier**
  \[
  \frac{V_{\text{OUT}}}{V_{\text{IN}}} = -\frac{R_2}{R_1}
  \]

- **Noninverting Amplifier**
  \[
  \frac{V_{\text{OUT}}}{V_{\text{IN}}} = 1 + \frac{R_2}{R_1}
  \]

- **Inverting Integrator**
  \[
  \frac{V_{\text{OUT}}}{V_{\text{IN}}} = -\frac{1}{sRC}
  \]
  \[
  i_0 = \frac{1}{RC}
  \]

- **Low-pass Active Filter**
  \[
  \frac{V_{\text{OUT}}}{V_{\text{IN}}} = -\frac{R/R_1}{1 + RCs}
  \]
  \[
  p = -\frac{1}{RC}
  \]

Not practical to implement on silicon

- Area for R too big
- Area for C too big
- Accuracy of \(i_0\) and \(p\) too poor

But ratio accuracy can be very good (0.1% or better with good layout and appropriate area)
How bad is the problem?

\[ R_{\square} = 21.7 \Omega/\square \text{ and } C_d = 0.864 \text{pF}/\mu^2 \]
How bad is the problem?

Assume $p=2\pi \cdot 1K$ and pole accuracy needed is 0.1%

Process tolerance on $R$ and $C$ is about $\pm 20%$

$R_{\Box}=20\Omega/\Box$ and $C_d=1pF/\mu^2$

If $R=1K$, require $1000/20=50$ squares

$$\frac{1}{RC} = 2000\pi$$
$$C = \frac{1}{R \cdot 2000\pi}$$
$$C = \frac{1}{1000 \cdot 2000\pi} = 0.159 \mu F$$

$$A_C = \frac{C}{C_D} = \frac{0.159 \mu F}{1fF / \mu^2} = 1.59 \times 10^8 \mu^2$$

Pole tolerance $\pm 40%$

Both are orders of magnitude unacceptable!
An amplifier alternative?

Capacitor version is area effective and can have very good accuracy.
The node between $C_1$ and $C_2$ is a floating node if the Op Amp has a MOS differential pair at the input.
But if we get any charge on the intermediate node there is no way to get it off.
An amplifier alternative?:

During $\Phi_1$

$C_1$ is charged to $V_{IN}$ and stores charge $Q_1 = C_1 V_{IN}$

$C_F$ is discharged and $V_{OUT} = 0$

During $\Phi_2$

$C_1$ is discharged but charge is transferred to $C_F$

$Q_2 = -Q_1$ and $V_{OUT} = Q_2/C_2$

Substituting for $Q_1$ we obtain $V_{OUT} = -C_1/C_2 V_{IN}$

Serves as a voltage amplifier during $\Phi_2$

$\Phi_1$ and $\Phi_2$ are nonoverlapping clocks
An amplifier alternative!

\[ V_{\text{OUT}} = -\frac{C_1}{C_2} V_{\text{IN}} \]

- Many applications only need amplifier output at discrete points in time
- Accuracy can be very good
- Area can be very small

But, what about the switches?
Switches for SC Circuits

- Often a single MOS transistor is adequate (either n-ch or p-ch)
- Sometimes need transmission-gate switch (parallel n-ch and p-ch)
- Switches work very well and can be very small but must manage their $R_{\text{ON}}$
Stray Insensitive SC Amplifiers

Noninverting

Inverting
Summing amplifier inputs either inverting or noninverting can be easily obtained.
Consider the Basic Integrator

\[ T(s) = -\frac{1}{RCs} \]

\[ I_0 = \frac{1}{RC} \]

Key performance of integrator (and integrator-based filter) is determined by the integrator time constant \( I_0 \)

Precision of time constants of a filter invariably determined by precision of \( I_0 \)
Integrator-Based Filters:

\[
\frac{V_{OUT}}{V_{IN}} = T(s) = \frac{1}{R_0C_1} \frac{s}{s^2 + s \left( \frac{1}{R_QC_2} \right) + \frac{1}{R_1R_2C_1C_2}}
\]

Second-order Bandpass Filter

Denote as a two-integrator-loop structure
Integrator-Based Filters:

\[ V_{\text{IN}} \rightarrow R_0 \rightarrow C_1 \rightarrow R_2 \rightarrow R_A \rightarrow V_{\text{OUT}} \]

\[ R_0 \rightarrow R_Q \rightarrow C_1 \rightarrow R_2 \rightarrow R_A \rightarrow V_{\text{OUT}} \]

\[ \text{INT}_1 \rightarrow V_{\text{IN}} \rightarrow R_0 \rightarrow C_1 \rightarrow \text{INT}_2 \rightarrow \]

\[ R_0 \rightarrow R_Q \rightarrow C_1 \rightarrow R_2 \rightarrow \text{INT}_2 \rightarrow R_3 \rightarrow \]
Integrator-Based Filters:

\[
\frac{V_{OUT}}{V_{IN}} = T(s) = -\frac{1}{R_0C_1} \cdot \frac{1}{s^2 + s \left(\frac{1}{R_0C_1} + \frac{1}{R_QC_2} + \frac{1}{R_1R_2C_1C_2}\right)}
\]

Second-order Lowpass Filter

Denote as a two-integrator-loop structure

- Any filter transfer function can be implemented with integrators and summers
- Some of the best known filter structures are based upon integrators and summers
- Accuracy of RC products is critical in the design of good filters
Consider the Basic Integrator

\[
T(s) = -\frac{1}{RCs}
\]

\[
I_0 = \frac{1}{RC}
\]

1. Accuracy of R and C difficult to accurately control – particularly in integrated applications (often 2 or 3 orders of magnitude to variable)

2. Size of R and C unacceptably large if \(I_0\) is in audio frequency range (2 or 3 orders of magnitude too large)

3. Amplifier GB limits performance

Incredible Challenge to Building Filters on Silicon!
Integrator Design Issues

\[ T(s) = -\frac{1}{RCs} \]

\[ I_0 = \frac{1}{RC} \]

Consider:

Assume \( T_{CLK} \ll T_{SIG} \)

\( \Phi_1 \) and \( \Phi_2 \) are complementary nonoverlapping clocks

Termed a switched-capacitor circuit
Consider the Switched-Capacitor Circuit

Assume $T_{CLK} \ll T_{SIG}$

$\Phi_1$ and $\Phi_2$ are complimentary nonoverlapping clocks
Consider the Switched-Capacitor Circuit

Assume $T_{CLK} \ll T_{SIG}$

$\Phi_1$ and $\Phi_2$ are complimentary nonoverlapping clocks

Define $T = T_{CLK}$

$V(nT)$

$V((n+1)T)$

$\Phi_1$

$\Phi_2$

$nT_{CLK}$

$T_{CLK}$

$(n+1)T_{CLK}$

$nT$

$T$

$(n+1)T$
Compare the performance of the following two circuits

\[ T(s) = -\frac{1}{RC_s} \quad I_0 = \frac{1}{RC} \]
Consider the charge transferred to the feedback capacitor for both circuits in an interval of length $T_{CLK}$ at arbitrary time $t_1$.

For the RC circuit:

$$Q_{RC} = \int_{t_1}^{t_1 + T_{CLK}} i_{in}(t) \, dt$$

$$Q_{RC} = \int_{t_1}^{t_1 + T_{CLK}} \frac{V_{in}(t)}{R} \, dt$$

Since $V_{in}$ changes slowly

$$Q_{RC} \approx \int_{t_1}^{t_1 + T_{CLK}} \frac{V_{in}(t_1)}{R} \, dt$$

$$Q_{RC} \approx \left[ \frac{V_{in}(t_1)}{R} \right] \int_{t_1}^{t_1 + T_{CLK}} 1 \, dt$$

$$Q_{RC} \approx \left[ \frac{V_{in}(t_1)}{R} \right] T_{CLK}$$
Consider the charge transferred to the feedback capacitor for both circuits in an interval of length $T_{CLK}$ at time $t_1$.

For the RC circuit:

$$Q_{RC} \approx \left[ \frac{V_{in}(t_1)}{R} \right] T_{CLK}$$

Observe that a resistor “transfers” charge proportional to $V_{in}$ in a short interval of $T_{CLK}$.
For the SC circuit

\[ Q_{C1} = C_1 V_{in} \left( t_1 + \frac{T_{CLK}}{2} - \varepsilon \right) \]

Since \( V_{in}(t) \) is slowly varying

\[ Q_{C1} \approx C_1 V_{in}(t_1) \]

But this is the charge that will be transferred to \( C \) during phase \( \Phi_2 \)

\[ Q_{SC} \approx C_1 V_{in}(t_1) \]

Observe that the SC circuit also transfers charge proportional to \( V_{in} \) in short intervals of length \( T_{CLK} \).
Comparing the two circuits

\[ T(s) = -\frac{1}{RCs} \]

\[ I_0 = \frac{1}{RC} \]

Equating charges since both proportional to \( V_{in}(t_1) \)

\[ Q_{RC} \approx \left[ \frac{V_{in}(t_1)}{R} \right] T_{CLK} \]

\[ Q_{SC} \approx C_1 V_{in}(t_1) \]

\[ C_1 \approx \left[ \frac{1}{R} \right] T_{CLK} \]

\[ R_{EQ} \approx \frac{1}{f_{CLK} C_1} \]
\[ T(s) = -\frac{1}{RCs} \]

\[ I_0 = \frac{1}{RC} \]

\[ R_{EQ} \approx \frac{1}{f_{CLK}C_1} \]

Observe that a switched-capacitor behaves as a resistor!

This is an interesting observation that was made by Maxwell over 100 years ago but in and of itself was of almost no consequence

Note that large resistors require small capacitors!

This offers potential for overcoming one of the critical challenges for Implementing integrators on silicon at audio frequencies!
Equivalence Between Rapidly Switched Capacitor and Resistor

\[ R_{EQ} \approx \frac{1}{f_{CLK} C_1} \]
Consider again the SC integrator

\[
T_{SC}(s) \approx \frac{-1}{R_{EQ}C_s}
\]

\[
l_{0eq} = \frac{1}{R_{EQ}C}
\]

\[
l_{0eq} = \frac{1}{R_{EQ}C} = \frac{C_1f_{CLK}}{C}
\]

\[
l_{0eq} = \left[ \frac{C_1}{C} \right] f_{CLK}
\]

This is a frequency referenced filter!
Consider again the SC integrator

\[ T_{SC}(s) = \frac{-1}{R_{EQ} C_s} \]

\[ I_{0eq} = \left[ \frac{C_1}{C} \right] f_{CLK} \]

The expressions \( S_C' \) and \( S_{C_1}' \) have the same magnitude as for the RC integrator

- But the ratio of capacitors can be accurately controlled in IC processes (1% to .01% is achievable with careful layout)
- \( f_{CLK} \) can be VERY accurately controlled with a crystal (1 part in 10^6 or better)
- Variability of \( I_{0eq} \) is very small

The SC integrator can dramatically reduce the second main concern for building integrated integrators
Consider again the SC integrator

\[ T(s) = -\frac{1}{RC_s} \quad \text{and} \quad I_0 = \frac{1}{RC} \]

1. Accuracy of R and C difficult to accurately control (often 2 or 3 orders of magnitude to variable)
2. Area of R and C too large in audio frequency range (2 or 3 orders of magnitude too large)
3. Amplifier GB limits performance

1. Accuracy of cap ratio and \( f_{CLK} \) very good
2. Area of C1 and C not too large
3. Amplifier GB limits performance less
The Genius!!

\[ T(s) = -\frac{1}{RC_s} \quad I_0 = \frac{1}{RC} \]

1. Accuracy of R and C difficult to accurately control (often 2 or 3 orders of magnitude to variable)

2. Area of R and C too large in audio frequency range (2 or 3 orders of magnitude too large)

3. Amplifier GB limits performance

- Accuracy of cap ratio and \( f_{\text{CLK}} \) very good
- Area of C1 and C not too large
- Amplifier GB limits performance less

Observation of Maxwell (and other “Me Too” up until 1977) on equivalence of resistor and switched capacitor had no impact

Two groups independently observed items 1) and 2) in 1976/1977 timeframe and realized that practical implementations on silicon were possible and that is the genius of the concept

Switched Capacitors and the corresponding charge redistribution circuits now used well beyond the SC filter field

Incredible enthusiasm and effort followed for better part of a decade
sC integrator with summing inputs
sC low-pass filter with summing inputs
Consider again the SC integrator

\[
I_{0eq} = \left[ \frac{C_1}{C} \right] f_{CLK}
\]

Observe this circuit has considerable parasitics

\[
C_{1EQ} = C_1 + C_{s1} + C_{d2} + C_{T1}
\]

Parasitic capacitors \( C_{s1} + C_{d2} + C_{T1} \) difficult to accurately match

- Parasitic capacitors of THIS SC integrator limit performance
- Other SC integrators (discussed later) offer same benefits but are not affected by parasitic capacitors
Stray insensitive Inverting and Noninverting SC integrators

Noninverting

Inverting

(a)

(b)
Stray Insensitive SC Low-Pass Filter with Inverting and Noninverting Inputs

Arbitrary number of inverting and ioninverting Inputs can be added
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} << T_{SIG}$
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$

\[ T_{CLK} \quad T_{SIG} \]

\[ \phi_1 \quad \phi_2 \]
Switched-Capacitor Filter Issues

What if $T_{\text{CLK}}$ is not much-much smaller than $T_{\text{SIG}}$?

For $T_{\text{CLK}} << T_{\text{SIG}}$
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$

![Diagram showing waveforms and time intervals with $T_{CLK}$ and $T_{SIG}$]
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much--much smaller than $T_{SIG}$?

For $T_{CLK} \ll T_{SIG}$

\[ V(nT) \quad \rightarrow \quad V((n+1)T) \]

\[ \varphi_1 \quad \rightarrow \quad (n+1)T_{CLK} \quad \rightarrow \quad \varphi_2 \]

Define \( T = T_{CLK} \)

Considerable change in $V(t)$ in clock period
Switched-Capacitor Filter Issues

What if \( T_{CLK} \) is not much smaller than \( T_{SIG} \)?

For \( T_{CLK} < T_{SIG} \)

\[
V(nT) \quad \text{in} \quad V((n+1)T)
\]

\[
V_0(nT+T) = V_0(nT) + \frac{\Delta Q}{C}
\]

but \(-uQ\) is the charge on \( C_1 \) and the time \( \varphi_1 \) opens

\[-uQ \approx C_1 V_{IN}(nT+T/2)\]

\[
\therefore V_{OUT}(nT+T) = V_{OUT}(nT) - \left( \frac{C_1}{C} \right) V_{IN}(nT+T/2)
\]

If an input S/H, \( V_{IN} \) constant over periods of length \( T \) thus, assume \( V_{IN}(nT+T/2) \approx V_{IN}(nT) \)

So obtain

\[
V_{OUT}(nT+T) = V_{OUT}(nT) - \left( \frac{C_1}{C} \right) V_{IN}(nT)
\]
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

$$V_{OUT}(nT+T) = V_{OUT}(nT) - \left(\frac{C_1}{C}\right)V_{IN}(nT)$$

for any $T_{CLK}$, characterized in time domain by difference equation

or in frequency domain characterized by transfer function obtained by taking $z$-transform of the difference equation

$$H(z) = -\frac{C_1}{C} \frac{1}{z-1}$$
What is really required for building a filter that has high-performance features?

Frequency domain:

Transfer function

\[ T(s) = \frac{1}{RCs} \]

Time domain:

Differential Equation

\[ V_{OUT}(t) = V_{OUT}(t_0) + \frac{1}{RC} \int_{t_0}^{t} V_{IN}(\tau) d\tau \]

Accurate control of polynomial coefficients in transfer function or accurate control of coefficients in the differential equation
What is really required for building a filter that has high-performance features?

**Frequency domain:**

Transfer function

\[ T(s) = \frac{1}{RCs} \]

**Time domain:**

- Differential Equation
  \[ V_{OUT}(t) = V_{OUT}(t_0) + \frac{1}{RC} \int_{t_0}^{t} V_{IN}(\tau) d\tau \]

- Difference Equation
  \[ V_{OUT}(nT+T) = V_{OUT}(nT) - (C_1/C)V_{IN}(nT) \]

Accurate control of polynomial coefficients in transfer function or accurate control of coefficients in the differential/difference equation
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

\[ V_{OUT}(nT+T) = V_{OUT}(nT) - \frac{C_1}{C} V_{IN}(nT) \]

\[ H(z) = -\frac{C_1}{C\cdot(z-1)} \]

Switched-capacitor circuits have potential for good accuracy and attractive area irrespective of how $T_{CLK}$ relates to $T_{SIG}$.

But good layout techniques and appropriate area need to be allocated to realize this potential!
Consider the following circuit

Termed a flip-around amplifier

Clock signals are complimentary non-overlapping
The flip-around amplifier

During $\Phi_1$

During $\Phi_2$
The flip-around amplifier
During $\Phi_1$

$$Q_1 = C_1 \left( V_{IN} - V^+ \right)$$
$$Q_2 = C_2 \left( V_{IN} - V^+ \right)$$
The flip-around amplifier

During $\Phi_2$

$$
\begin{align*}
V_{X} & \quad \Phi_2 \\
\Phi_2 & \quad C_1 \\
\Phi_1 & \quad C_2 \\
V_{IN} & \quad V_{OUT} \\
V_{X} & \quad V_{OUT}
\end{align*}
$$
The flip-around amplifier

During $\Phi_2$

$Q_1 = C_1(V_{IN} - V^+)$

$Q_2 = C_2(V_{IN} - V^+)$

$Q_{1T} = C_1(V_{IN} - V^+) - C_1(V_X - V^+) = C_1(V_{IN} - V_X)$

$Q_{2F} = Q_2 + Q_{1T} = C_2(V_{IN} - V^+) + C_1(V_{IN} - V_X) = (C_1 + C_2)V_{IN} - C_2 V^+ - C_1 V_X$
The flip-around amplifier

During $\Phi_2$

$$Q_{2F} = Q_2 + Q_{1T} = C_2 (V_{\text{IN}} - V^+) + C_1 (V_{\text{IN}} - V_X) = (C_1 + C_2)V_{\text{IN}} - C_2 V^+ - C_1 V_X$$

$$V_{C2F} = \frac{Q_{2F}}{C_2} = \left(1 + \frac{C_1}{C_2}\right)V_{\text{IN}} - V^+ - \frac{C_1}{C_2} V_X$$

$$V_{\text{OUTF}} = V_{C2F} + V^+ = \left(1 + \frac{C_1}{C_2}\right)V_{\text{IN}} - \frac{C_1}{C_2} V_X$$
Comparison of Flip Around Amplifier with previous SC amplifier

\[ V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right) V_{IN} - \frac{C_1}{C_2} V_X \]

If \( V_X = 0 \), both have a positive gain but somewhat more gain for a given capacitor ratio for the flip-around structure.

In both cases, gain accuracy dependent upon how closely the capacitor ratios can be controlled.

One particularly useful application is where want dc gain equal to 2 (1-bit/stage pipeline ADC).

Flip-around requires matching two capacitors, other requires ratio matching of two capacitors.
Another Flip Around Amplifier

Clock signals are complimentary non-overlapping
Another Flip Around Amplifier

During phase $\phi_1$

Assume $C_B$ discharged at start of phase – must verify later

\[
Q_{CA1} = C_A V_{IN} \\
Q_{CB1} = C_A V_{IN} \\
V_{OUT} = -\frac{Q_{CB1}}{C_B} = -\frac{C_A}{C_B} V_{IN}
\]
Another Flip Around Amplifier

During phase $\phi_2$

From phase $\phi_1$

\[ Q_{CA1} = C_A \cdot V_{IN} \]
\[ Q_{CB1} = C_A \cdot V_{IN} \]

\[ Q_{CA2} = Q_{CA1} + Q_{CB1} \]
\[ Q_{CB2} = 0 \]

\[ V_{OUT} = -\frac{Q_{CA2}}{C_A} \]

\[ V_{CB} = 0 \]

Verified that $C_B$ was discharged at the start of phase $\phi_1$

\[ V_{OUT} = -\frac{C_A \cdot V_{IN} + C_A \cdot V_{IN}}{C_A} = -2V_{IN} \]

This structure has a gain of 2 independent of any capacitor matching!

Can modify to get noninverting gain and gains of 3, 4, .., without matching requirements.
Non-overlapping Clocks

- Essential that the clocks be non-overlapping
- Simple inverter to derive the complimentary clock will not work
- Must guarantee non-overlap in the presence of PVT variations
- In non-demanding speed applications, $\varphi_1$ and $\varphi_2$ will have 25% duty cycles
Stay Safe and Stay Healthy!
End of Lecture 42