Switched-Capacitor Filters and Amplifiers
Observation:

- The integrator is the key building block in most filters.
- Accuracy of $I_0$ and $\alpha$ is important!
- Most integrated filters are built with integrators, lossy integrators and summers.
If \( I_0 = 1 \text{ KRad/Sec} \) and \( C = 1 \text{ pF} \), how large must \( R \) be?

\[
R = \frac{1}{I_0 C} = 10^9
\]

If sheet resistance is 30ohms/square, one resistor requires 33 million squares!
Challenges in Integrated Filter Design

• Accuracy of components is not good enough (orders of magnitude)
• Area too large for audio frequencies (orders of magnitude)
Challenges in Integrated Filter / Integrated Integrator Design

- Accuracy of R and C difficult to accurately control – particularly in integrated applications
- Size of R and C unacceptably large if $I_0$ is in audio frequency range
- Amplifier GB limits performance

$$T(s) = -\frac{1}{RCs}$$

$$I_0 = \frac{1}{RC}$$
Consider the following circuit

\[ Q_{RC} = - \int_{t=t_1}^{t_1+T} i(t) \, dt = - \frac{1}{R} \int_{t=t_1}^{t_1+T} V_{IN}(t) \, dt \]

\[ V_{OUT}(t_1+T) = V_{OUT}(t_1) - \frac{Q_{RC}}{C} \]

If \( T \ll T_{SIG} \)

\[ V_{IN}(t); \quad V_{IN}(t_1) \quad \text{for} \quad t_1 < t < t_1 + T \]
Consider the following circuit

If $T \ll T_{SIG}$

\[
Q_{RC} = - \int_{t=t_1}^{t_1+T} i(t) dt = - \frac{1}{R} \int_{t=t_1}^{t_1+T} V_{IN}(t) dt - \frac{V_{IN}(t_1)}{R} \int_{t=t_1}^{t_1+T} 1 dt = - \frac{V_{IN}(t_1)}{R} T
\]

\[
V_{OUT}(t_1+T) = V_{OUT}(t_1) - \frac{Q_{RC}}{C} ; V_{OUT}(t_1) - \frac{V_{IN}(t_1)}{RC} T
\]
Consider the following circuit

If $T \ll T_{\text{SIG}}$

$$Q_{SC} = -C_1 \cdot V_{IN}(t_1)$$

$$V_{OUT(t_1+T)} = V_{OUT(t_1)} - \frac{Q_{SC}}{C} ; \ V_{OUT(t_1)} - V_{IN(t_1)} \frac{C_1}{C}$$
Consider the following two circuits

Both transfer charge proportional to $V_{IN}(t_1)$
Consider the following two circuits

\[ V_{IN} \]
\[ R \]
\[ V_{OUT} \]
\[ C \]

\[ \phi \]
\[ \phi \]
\[ V_{IN} \]
\[ C \]
\[ V_{OUT} \]

Thus equating charges

\[ Q_{RC} = -\frac{V_{IN}(t_1)}{R} T \]
\[ Q_{SC} = -C_1 \cdot V_{IN}(t_1) \]

Obtain the equivalent resistance of the switched-capacitor circuit

\[ R_{EQ} = \frac{T}{C_1} \]
Thus, if clocked with a clock period of $T$, for $T \ll T_{\text{SIG}}$, we have the following equivalence

$$R_{\text{EQ}} \approx \frac{T}{C_1}$$

Equivalence of a switched capacitor and a resistor has been known for over 100 years. Up until 1977, this knowledge was of little practical significance.
The switched-capacitor integrator

\[
R_{EQ} = \frac{T}{C_1}
\]

But what about the challenges of integrating the active RC integrator?

- Accuracy of R and C difficult to accurately control – particularly in integrated applications
- Size of R and C unacceptably large if \( I_0 \) is in audio frequency range
- Amplifier GB limits performance

Large resistors require small capacitors (since \( C_1 \) appears in denominator)!
The switched-capacitor integrator

![Diagram of switched-capacitor integrator]

\[ I_0 = \frac{1}{R_{EQ}C} \quad \rightarrow \quad I_0 = T \cdot \left( \frac{C_1}{C} \right) \quad \rightarrow \quad I_0 = \frac{1}{f_{CLK}} \left( \frac{C_1}{C} \right) \]

- Capacitor ratios can be maintained to the 0.1% accuracy level or better
- Very accurate clocks can be inexpensively generated
- GB requirements for Op Amp actually relaxed with SC integrator compared to active RC integrator
The switched-capacitor integrator

\[ \text{Switched-Capacitor Integrators offers orders of magnitude improvement in first two major challenges!} \]

- Accuracy of R and C difficult to accurately control – particularly in integrated applications
- Size of R and C unacceptably large if \( I_0 \) is in audio frequency range
- Amplifier GB limits performance

But what about the challenges of integrating the active RC integrator?
The switched-capacitor integrator

\[ I_0 = \frac{1}{R_{\text{EQ}} C} \quad \rightarrow \quad I_0 = T \cdot \left( \frac{C_1}{C} \right) \quad \rightarrow \quad I_0 = \frac{1}{f_{\text{CLK}}} \left( \frac{C_1}{C} \right) \]
The switched-capacitor (SC) integrator

Non-overlap of clocks is critical in SC circuits

\[ I_0 = \frac{1}{f_{\text{CLK}}} \left( \frac{C_1}{C} \right) \]
Switched-Capacitor Filter

\[ \varphi_1 \quad \varphi_2 \quad \varphi_3 \quad C \quad V_{\text{in}} \quad V_{\text{out}} \]

\[ T_{\text{CLK}} \ll T_{\text{SIG}} \]

\[ T_{\text{SIG}} \]

\[ T_{\text{CLK}} \]

\[ \varphi_1 \quad \varphi_2 \]

\[ t_1 \quad t_1 + T_{\text{CLK}} \]
Basic Building Blocks in Both Cascaded Biquads and Multiple Feedback Structures

- Developed from observations from feedback implementations
  1. Integrators
  2. Summers
  3. First-order filter blocks
  4. Biquads
  5. Switches

- Same building blocks used in open-loop applications as well
Switched-Capacitor Filters

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

For $T_{CLK} \ll T_{SIG}$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} \ll T_{SIG}$
Switched-Capacitor Filters

What if $T_{\text{CLK}}$ is not much much smaller than $T_{\text{SIG}}$?

For $T_{\text{CLK}} \ll T_{\text{SIG}}$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} \ll T_{SIG}$

\[ V(nT) \rightarrow V((n+1)T) \]

Define \( T = T_{CLK} \)

Considerable change in $V(t)$ in clock period
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$

$T_{CLK}$

$T_{SIG}$

$\varphi_1$

$\varphi_2$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$

$V(nT)$

$V((n+1)T)$

Define $T = T_{CLK}$

$V_0(nT + T) = V_0(nT) + \frac{\Delta Q}{C}$

but $-uQ$ is the charge on $C_1$ at the time $\phi_1$ opens

$-uQ; C_1 V_{IN}(nT + T/2)$

$V_{OUT}(nT + T) = V_{OUT}(nT) - (C_1/C)V_{IN}(nT + T/2)$

If an input S/H, $V_{IN}$ constant over periods of length $T$

thus, assume $V_{IN}(nT + T/2); V_{IN}(nT)$

So obtain

$V_{OUT}(nT + T) = V_{OUT}(nT) - (C_1/C)V_{IN}(nT)$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

$V_{OUT}(nT+T) = V_{OUT}(nT) - \frac{C_1}{C} V_{IN}(nT)$

This is a difference equation relating $V_{OUT}(nT)$ to $V_{IN}(nT)$

Coefficients in difference equation are all accurately controlled!

Difference equation is highly insensitive to process variations and temperature variations!
Switched-Capacitor Filters

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

Taking the z-transform we obtain

$$zV_O = V_O - \left( \frac{C_1}{C} \right)V_{IN}$$

$$I(z) = \frac{V_O}{V_{IN}} = -\left( \frac{C_1}{C} \right) \frac{1}{z-1}$$

$$V_{OUT}(nT+T) = V_{OUT}(nT) - (C_1/C)V_{IN}(nT)$$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

$$V_{OUT}(nT+T) = V_{OUT}(nT) - \left(\frac{C_1}{C}\right)V_{IN}(nT)$$

$$I(z) = -\frac{C_1}{C} \frac{1}{z-1}$$

- Switched-capacitor circuits are analyzed in the z-domain rather than in the s-domain.
- Coefficients are precisely controlled with small area even if $T_{CLK}$ is not much smaller than $T_{SIG}$.
- Assumption of input S/H is really not necessary.
- Often no underlying Active RC circuit (direct synthesis in the discrete domain).
- SC circuits are discrete-time continuous-amplitude circuits.
Switched-Capacitor Filters

Parasitic Capacitances

Parasitic capacitances are large, do not match, and most are nonlinear!
Switched-Capacitor Filters

Parasitic Capacitances

Parasitics affecting charge transfer are indicated

\[ V_{\text{OUT}}(nT+T) = V_{\text{OUT}}(nT) - \left( \frac{[C_1+C_P]}{C} \right)V_{\text{IN}}(nT) \]

- Can affect the ratio \( C_1/C_P \) by 30% or more
- Most of the accuracy improvements offered by SC technique lost in parasitics!
Switched-Capacitor Filters

Consider:

\[ V_{OUT}(nT+T) = V_{OUT}(nT) + \left( \frac{C_1}{C} \right) V_{IN}(nT) \]

with input S/H

\[ V_{OUT}(nT+T) = V_{OUT}(nT) + \left( \frac{C_1}{C} \right) V_{IN}(nT) \]

\[ I(z) = \left( \frac{C_1}{C} \right) \frac{1}{z-1}. \]

- Performs as a noninverting integrator
- Note simple noninverting integrator function without need for extra op amp
- Requires extra switches
- Has many more parasitics
Switched-Capacitor Filters

Parasitic Capacitances
Switched-Capacitor Filters

Parasitics affecting charge transfer are indicated

- Effects of all parasitic capacitances have been essentially eliminated!
- Termed a stray-insensitive or parasitic-insensitive structure
- Widely used as a noninverting SC integrator
Switched-Capacitor Filters

Consider the following SC circuit

\[ V_{\text{OUT}}(nT+T) = V_{\text{OUT}}(nT) - \left( \frac{C_1}{C} \right) V_{\text{IN}}(nT+T) \]

Serves as inverting stray-insensitive SC integrator
Switched-Capacitor Filters

Summing inputs (any number of summing inputs can be used)

(Shown stray-sensitive to reduce schematic complexity only)
Switched-Capacitor Filters

Lossy inverting integrator

\[ V_{\text{OUT}}(nT + T) = V_{\text{OUT}}(nT) - \left( \frac{C_2}{C} \right) V_{\text{IN}}(nT) - \left( \frac{C_1}{C} \right) V_{\text{IN}}(nT) \]

\[ \frac{V_{\text{OUT}}(z)}{V_{\text{IN}}(z)} = I(z) = -\frac{z \left( \frac{C_1}{C} \right)}{z \left( 1 - \frac{C_2}{C} \right)} \]

(Shown stray-sensitive to reduce schematic complexity only)
Switched-Capacitor Filters

Summing Lossy inverting integrator

(Shown stray-sensitive to reduce schematic complexity only)
Switched-Capacitor Filters

Stray Insensitive Lossy Integrator with inverting and noninverting summing inputs

\[ V_{OUT}(nT+T) = V_{OUT}(nT) - \left( \frac{C_3}{C} \right) V_{OUT}(nT+T) + \left( \frac{C_1}{C} \right) V_{IN1}(nT+T) - \left( \frac{C_2}{C} \right) V_{IN2}(nT+T) \]

\[ V_{OUT}(z) = \frac{z \left( \frac{C_1}{C} \right) V_{IN1} - z \left( \frac{C_2}{C} \right) V_{IN2}}{\left( 1 + \frac{C_3}{C_1} \right) z - 1} \]
Observation:

- The integrator is the key building block in most filters

- Accuracy of $I_0$ and $\alpha$ is important!

- Most integrated filters are built with integrators, lossy integrators and summers

Have practical method of building integrated audio frequency filters!

Practical summers might still be useful
Typical Filter Implementation

\[ V_{IN} \rightarrow T_0(s) \rightarrow T_1(s) \rightarrow T_2(s) \rightarrow \cdots \rightarrow T_k(s) \rightarrow \cdots \rightarrow T_m(s) \rightarrow V_{OUT} \]

Biquads often LP or BP
Typical Biquad Implementation (Two-Integrator Loop)

\[ T(s) = \frac{-I_0^2}{s^2 + \alpha I_0 s + I_0^2} \]

Accurate control of \( I_0 \) and \( \alpha \) is essential for building most filters!
Switched-Capacitor Amplifiers

Noninverting Amplifier

\[ A_V = \frac{C_1}{C} \]

- Accurate control of gain is possible (0.1% or better) but extreme care to detail in layout and statistical analysis for adequate area allocation is necessary
- Stray-insensitive structures

Inverting Amplifier

\[ A_V = -\frac{C_1}{C} \]
Switched-Capacitor Amplifiers

Noninverting Amplifier

\[ A_V = \frac{C_1}{C} \]

Inverting Amplifier

\[ A_V = -\frac{C_1}{C} \]

Bottom-plate sampling with advanced clock reduces signal-dependent gain errors when \( V_{\text{IN}} \) is time varying: Sample and Hold
Switched-Capacitor Amplifiers

Summing Inverting and Noninverting Amplifier

\[ V_{OUT} = \frac{C_1}{C} V_{IN1} - \frac{C_2}{C} V_{IN2} \]

(modification for bottom-plate sampling needed if \( V_{IN} \) is time varying: track and hold)
Switched-Capacitor Amplifiers

Flip-Around Amplifier

\[ A_V = 1 + \frac{C_1}{C_2} \]

(modification for bottom-plate sampling needed if \( V_{IN} \) is time varying: track and hold)
Switched-Capacitor Amplifiers

\[ V_{\text{OUT}} = V_{\text{IN}1} \left( 1 + \frac{C_1}{C_2} \right) - V_{\text{IN}2} \left( \frac{C_1}{C_2} \right) \]

Flip-Around Subtracting Amplifier

(modification for bottom-plate sampling needed if \( V_{\text{IN}} \) is time varying: track and hold)
Switched-Capacitor Amplifiers

Consider the following circuit

\[ V_{IN} \rightarrow \Phi_1+\Phi_3 \rightarrow C_1 \rightarrow \Phi_2+\Phi_4 \rightarrow C_2 \rightarrow \Phi_1+\Phi_2 \rightarrow V_{OUT} \]
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_1$

$$Q_{C1} = C_1 V_{IN}$$
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_2$

From $\Phi_1$ $Q_{C1} = C_1 V_{IN}$

during $\Phi_2$ $Q_{C1} = 0$ $Q_{C2} = C_1 V_{IN}$
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_3$

from $\Phi_2$ \hspace{1cm} $Q_{C1}=0$ \hspace{1cm} $Q_{C2}=C_1V_{IN}$

during $\Phi_2$ \hspace{1cm} $Q_{C1}=C_1V_{IN}$ \hspace{1cm} $Q_{C2}=C_1V_{IN}$
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_4$

From $\Phi_3$ $Q_{C1}=C_1V_{IN}$ $Q_{C2}=C_1V_{IN}$

During $\Phi_2$ $Q_{C2}=0$ $Q_{C1}=2C_1V_{IN}$

Thus $V_{OUT}=Q_{C1}/C_1=2V_{IN}$
Switched-Capacitor Amplifiers

Consider the following circuit

\[ A_V = 2 \]

Gain of 2 obtained without requiring any matching of components
Top-Plate vs Bottom-Plate Sampling

Top-Plate Sampling

Bottom-Plate Sampling
Top-Plate vs Bottom-Plate Sampling

**Top-Plate Sampling**

\[ V_{IN} \rightarrow \Phi_1 \rightarrow C \rightarrow V_{OUT} \]

**Bottom-Plate Sampling**

\[ V_{IN} \rightarrow C \rightarrow \Phi_1 \rightarrow V_{OUT} \]
Top-Plate Sampling

- Actual sample taken at $t_A$
- Sampled-value is signal-level dependent
- Equivalent to a signal-dependent jitter on sampling clock
- Causes serious nonlinear distortion if signal frequency is high
Bottom-Plate Sampling

- Actual sample taken at $t_A$
- $t_A - t_D$ is independent of $V_{IN}(t)$
- Dramatic reduction in nonlinear distortion and signal-dependent sampling error
- Effectively causes a constant phase shift in sampling time
Bottom-Plate Sampling

[Diagram of a bottom-plate sampling circuit with labels $\Phi_1$, $\Phi_2$, $\Phi_{1A}$, $V_{in}$, and $V_{out}$]
Bottom-Plate Sampling

Expanded time axis:

\[ V_{IN} \]

\[ \varphi_1 \]

\[ \varphi_{1A} \]
Bottom-Plate Sampling

Further expanded time axis ($V_{IN}$ change exaggerated to show effects):
Bottom-Plate Sampling

- Actual sample taken at \( t_A \)
- \( t_A - t_D \) is independent of \( V_{IN}(t) \)
- Some very small change in \( V_{OUT} \) will occur until \( \Phi_1 \) opens
- Time \( \Phi_1 \) opens is input signal-level dependent

\( C_T \) and \( C_B \) are parasitic capacitances that appear at nodes connected to top plate and bottom plate of \( C \).
Bottom-Plate Sampling

\[
V_{\text{OUT}}(t_A) = V_{\text{IN}}(t_A)
\]

but:

\[
V_{\text{OUT}}(t_T) = V_{\text{IN}}(t_A) + \left( \frac{C_B}{C+C_B} \right) (V_{\text{IN}}(t_T) - V_{\text{IN}}(t_A))
\]

can be rewritten as:

\[
V_{\text{OUT}}(t_T) = V_{\text{IN}}(t_A) \left( \frac{C}{C+C_B} \right) + \left( \frac{C_B}{C+C_B} \right) V_{\text{IN}}(t_T)
\]

- Small gain error on sampling \( V_{\text{IN}} \) at \( t_A \)
- Dependent upon \( V_{\text{IN}}(t_T) \) which causes small distortion in sample
- \( C_B \) can be a reasonable percentage of \( C \) so advanced clock does not completely solve the sampling time problem
Bottom-Plate Sampling

Consider the entire SC amplifier

\[ V_{C_1}(t_T) = V_{IN}(t_A) \left[ \frac{C_1}{C_1 + C_B} \right] + \left( \frac{C_B}{C_1 + C_B} \right) V_{IN}(t_T) \]

Likewise:

\[ V_{C_B}(t_T) = \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_T) - \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_A) \]

Thus charges stored on \( C_1 \) and \( C_B \) at \( t_T \) are

\[ Q_{C_1}(t_T) = C_1 V_{IN}(t_A) \left[ \frac{C_1}{C_1 + C_B} \right] + C_1 \left( \frac{C_B}{C_1 + C_B} \right) V_{IN}(t_T) \]

\[ Q_{C_B}(t_T) = C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_T) - C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_A) \]
Bottom-Plate Sampling

Consider the entire SC amplifier

\[ Q_{C_1}(t_T) = C_1 V_{IN}(t_A) \left( \frac{C_1}{C_1 + C_B} \right) + C_1 \left( \frac{C_B}{C_1 + C_B} \right) V_{IN}(t_T) \]

\[ Q_{C_B}(t_T) = C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_T) - C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_A) \]

During \( \Phi_2 \), these capacitors are both discharged and the charge on feedback capacitor \( C \) becomes

\[ Q_C = Q_{C_1} - Q_{C_B} \]

it thus follows that

\[ Q_C(t_T) = C_1 V_{IN}(t_A) \]

- Extra charge accumulated on \( C_1 \) until the top switch opened equal to charge accumulated on \( C_B \)
- For switching scheme used here, effects precisely cancel when charge is transferred to \( C \)
Bottom-Plate Sampling

Consider the entire SC amplifier

\[ Q_C(t_T) = C_1 V_{IN}(t_A) \]

Thus:

\[ V_{OUT}(t_T) = \frac{Q_C(t_T)}{C} = \frac{C_1}{C} V_{IN}(t_A) \]

As predicted the output voltage is not a function of \( t_T \) and thus the parasitic capacitance on the bottom Plate does not affect performance when bottom plate sampling is used
Switch impedance issues

\[ T(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{1}{1 + R_{SW}C \omega} \]

\[ |T(j\omega)| = \frac{1}{\sqrt{1 + (R_{SW}C \omega)^2}} \]

\[ \angle T(j\omega) = -\tan^{-1}\left(\frac{\omega R_{SW}C}{1}\right) \]

- When in track mode, non-zero \( R_{SW} \) causes small amplitude decrease and phase shift but no nonlinear distortion provided \( R_{SW} \) is not signal-level dependent.
- Top-plate switch (\( R_{SW} \) or \( R_{SWT} \)) is signal level dependent if implemented with simple transistor.
- Bottom-plate switch (\( R_{SWB} \)) is not signal-level dependent.
- Make \( R_{SW} \) and \( R_{SWT} \) sufficiently small to avoid distortion.
When transitioning from track mode to hold mode, switch impedance increases rapidly from non-zero $R_{SW}$. 
Switch impedance issues

Amplitude and phase shift for bottom-plate sampler (difficult to distinguish between phase and amplitude effects in this zoom)
Switch impedance issues

\[ V_{IN}(t_A) \]

\[ V_{OUT}(t_A) \]

Track

Hold

Ideal Switch Transition
Switch impedance issues

\[
\begin{align*}
V_{IN} & \quad V_{OUT} \\
R_{SW} & \quad R_{SW\,ON} \\
\phi_1 & \quad \phi_0
\end{align*}
\]

Track/Hold Transition

Actual Switch Transition

Track

Hold

\[
V_{IN}(t_A) \quad V_{OUT}(t_A) \quad V_{OUTI}(t_A)
\]
Switch impedance issues

- Track/Hold Transition usually not of concern if fast fall time on switch
- Switch impedance effects can be managed by making $R_{SW}$ small
- Bottom-plate sampling does not introduce distortion