Switched-Capacitor Amplifiers
Other Integrated Filters
Switched-Capacitor Amplifiers

Noninverting Amplifier

\[ A_V = \frac{C_1}{C} \]

- Accurate control of gain is possible (0.1% or better) but extreme care to detail in layout and statistical analysis for adequate area allocation is necessary
- Stray-insensitive structures

Inverting Amplifier

\[ A_V = -\frac{C_1}{C} \]
Switched-Capacitor Amplifiers

Noninverting Amplifier

\[ A_V = \frac{C_1}{C} \]

Inverting Amplifier

\[ A_V = -\frac{C_1}{C} \]

Bottom-plate sampling with advanced clock reduces signal-dependent gain errors when \( V_{\text{IN}} \) is time varying: Sample and Hold
Switched-Capacitor Amplifiers

Summing Inverting and Noninverting Amplifier

\[ V_{OUT} = \frac{C_1}{C} V_{IN1} - \frac{C_2}{C} V_{IN2} \]

(modification for bottom-plate sampling needed if \( V_{IN} \) is time varying: track and hold)
Switched-Capacitor Amplifiers

\[ A_V = 1 + \frac{C_1}{C_2} \]

Flip-Around Amplifier

(modification for bottom-plate sampling needed if \( V_{IN} \) is time varying: track and hold)
Switched-Capacitor Amplifiers

\[ V_{OUT} = V_{IN1} \left(1 + \frac{C_1}{C_2}\right) - V_{IN2} \left(\frac{C_1}{C_2}\right) \]

Flip-Around Subtracting Amplifier

(modification for bottom-plate sampling needed if \(V_{IN}\) is time varying: track and hold)
Switched-Capacitor Amplifiers

Consider the following circuit
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_1$

$$Q_{C1} = C_1 V_{IN}$$
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_2$

from $\Phi_1$ \quad $Q_{C1} = C_1 V_{IN}$

during $\Phi_2$ \quad $Q_{C1} = 0$ \quad $Q_{C2} = C_1 V_{IN}$
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_3$

From $\Phi_2$ $Q_{C1}=0$, $Q_{C2}=C_1V_{IN}$

During $\Phi_2$ $Q_{C1}=C_1V_{IN}$, $Q_{C2}=C_1V_{IN}$
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_4$

From $\Phi_3$

$Q_{C1} = C_1 V_{IN}$
$Q_{C2} = C_1 V_{IN}$

during $\Phi_2$

$Q_{C2} = 0$
$Q_{C1} = 2C_1 V_{IN}$

Thus $V_{OUT} = Q_{C1}/C_1 = 2V_{IN}$
Switched-Capacitor Amplifiers

Consider the following circuit

\[ A_V = 2 \]

Gain of 2 obtained without requiring any matching of components
Top-Plate vs Bottom-Plate Sampling

Top-Plate Sampling

Bottom-Plate Sampling

\[ V_{IN} \rightarrow \Phi_1 \rightarrow V_{OUT} \]

\[ V_{IN} \rightarrow + \rightarrow C \rightarrow \Phi_1 \rightarrow - \]

Top-Plate Sampling

Bottom-Plate Sampling
Top-Plate vs Bottom-Plate Sampling

Top-Plate Sampling

\[ V_{IN} \rightarrow \Phi_1 \rightarrow V_{OUT} \]
\[ \downarrow \]
\[ C \]
\[ \downarrow \]
\[ V_{IN} \rightarrow \Phi_A \rightarrow V_{OUT} \]
\[ \downarrow \]
\[ C \rightarrow \Phi_1 \]

Bottom-Plate Sampling

\[ V_{IN} \rightarrow \Phi_1 \rightarrow V_{OUT} \]
\[ \downarrow \]
\[ C \]
\[ \downarrow \]
\[ V_{IN} \rightarrow \Phi_A \rightarrow V_{OUT} \]
Top-Plate Sampling

- Actual sample taken at $t_A$
- Sampled-value is signal-level dependent
- Equivalent to a signal-dependent jitter on sampling clock
- Causes serious nonlinear distortion if signal frequency is high
Bottom-Plate Sampling

- Actual sample taken at $t_A$
- $t_A - t_D$ is independent of $V_{IN}(t)$
- Dramatic reduction in nonlinear distortion and signal-dependent sampling error
- Effectively causes a constant phase shift in sampling time
Bottom-Plate Sampling

![Diagram of Bottom-Plate Sampling with notation: $V_{IN}$, $C_1$, $C$, $V_{OUT}$, and switches represented as $\Phi_1$, $\Phi_2$, $\Phi_{1A}$]
Bottom-Plate Sampling

Expanded time axis:

\[
\varphi_1, \quad \varphi_{1A}
\]
Bottom-Plate Sampling

Further expanded time axis ($V_{IN}$ change exaggerated to show effects):

$V_{IN}(t_D)$

$V_{IN}(t_A)$

$V_T$
Bottom-Plate Sampling

- Actual sample taken at $t_A$
- $t_A - t_D$ is independent of $V_{IN}(t)$
- Some change in $V_{OUT}$ will occur until $\Phi_1$ opens
- Time $\Phi_1$ opens is input signal-level dependent

$C_T$ and $C_B$ are parasitic capacitances that appear at nodes connected to top plate and bottom plate of $C$.

Diagram showing the timing and voltage relationships with $V_{IN}$, $V_{OUT}$, and the timing of $\Phi_1$ opening.
Bottom-Plate Sampling

\[ V_{OUT}(t_A) = V_{IN}(t_A) \]

but:

\[ V_{OUT}(t_T) = V_{IN}(t_A) + \left( \frac{C_B}{C+C_B} \right) (V_{IN}(t_T) - V_{IN}(t_A)) \]

can be rewritten as:

\[ V_{OUT}(t_T) = V_{IN}(t_A) \left[ \frac{C}{C+C_B} \right] + \left( \frac{C_B}{C+C_B} \right)V_{IN}(t_T) \]

- Gain error on sampling \( V_{IN} \) at \( t_A \)
- Dependent upon \( V_{IN}(t_T) \) which causes distortion in sample
- \( C_B \) can be a reasonable percentage of \( C \)
Bottom-Plate Sampling

Consider the entire SC amplifier

\[
V_{C_1}(t_T) = V_{IN}(t_A)\left[\frac{C_1}{C_1+C_B}\right] + \left(\frac{C_B}{C_1+C_B}\right)V_{IN}(t_T)
\]

Likewise:

\[
V_{C_B}(t_T) = \left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_T) - \left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_A)
\]

Thus charges stored on \(C_1\) and \(C_B\) at \(t_T\) are

\[
Q_{C_1}(t_T) = C_1V_{IN}(t_A)\left[\frac{C_1}{C_1+C_B}\right] + C_1\left(\frac{C_B}{C_1+C_B}\right)V_{IN}(t_T)
\]

\[
Q_{C_B}(t_T) = C_B\left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_T) - C_B\left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_A)
\]
Bottom-Plate Sampling

Consider the entire SC amplifier

\[ Q_{C_1}(t_T) = C_1 V_{IN}(t_A) \left( \frac{C_1}{C_1 + C_B} \right) + C_1 \left( \frac{C_B}{C_1 + C_B} \right) V_{IN}(t_T) \]

\[ Q_{C_B}(t_T) = C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_T) - C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_A) \]

During \( \Phi_2 \), these capacitors are both discharged and the charge on feedback capacitor \( C \) becomes

\[ Q_C = Q_{C_1} - Q_{C_B} \]

it thus follows that

\[ Q_C(t_T) = C_1 V_{IN}(t_A) \]

- Extra charge accumulated on \( C_1 \) until the top switch opened equal to charge accumulated on \( C_B \)
- For switching scheme used here, effects precisely cancel when charge is transferred to \( C \)
Bottom-Plate Sampling

Consider the entire SC amplifier

\[ Q_C(t_T) = C_1 V_{IN}(t_A) \]

Thus:

\[ V_{OUT}(t_T) = \frac{Q_C(t_T)}{C} = \frac{C_1}{C} V_{IN}(t_A) \]

As predicted the output voltage is not a function of \( t_T \) and thus the parasitic capacitance on the bottom Plate does not affect performance when bottom plate sampling is used.
Switch impedance issues

\[ T(s) = \frac{V_{\text{OUT}}(s)}{V_{\text{IN}}(s)} = \frac{1}{1 + R_{\text{SW}}Cs} \]

\[ |T(j\omega)| = \frac{1}{\sqrt{1 + (R_{\text{SW}}C\omega)^2}} \]

\[ \angle T(j\omega) = -\tan^{-1}\left(\frac{\omega R_{\text{SW}}C}{1}\right) \]

• When in track mode, non-zero \( R_{\text{SW}} \) causes small amplitude decrease and phase shift but no nonlinear distortion provided \( R_{\text{SW}} \) is not signal-level dependent
• Top-plate switch (\( R_{\text{SW}} \) or \( R_{\text{SWT}} \)) is signal level dependent if implemented with simple transistor
• Bottom-plate switch (\( R_{\text{SWB}} \)) is not signal-level dependent
• Make \( R_{\text{SW}} \) and \( R_{\text{SWT}} \) sufficiently small to avoid distortion
Switch impedance issues

When transitioning from track mode to hold mode, switch impedance increases rapidly from non-zero $R_{SW}$. 
Switch impedance issues

Amplitude and phase shift for bottom-plate sampler (difficult to distinguish between phase and amplitude effects in this zoom)
Switch impedance issues

- **Switch Impedance Issues**: When a switch is turned on or off, there can be issues with impedance, leading to unexpected voltage or current levels.

- **Ideal Switch Transition**:的理想开关过渡

- **Track**: Transition phase where the input voltage is being transferred to the output.

- **Hold**: Hold phase where the output voltage remains constant.

- **V_IN(t_A)**: Input voltage at time t_A.

- **V_OUT(t_A)**: Output voltage at time t_A.

- **Vin(t_A)**, **VOUT(t_A)**: Voltage graphs at different points.

- **t_D**, **t_A**: Time points for different phases.

- **Ideal Switch Transition**: A smooth transition without impedance issues.
Switch impedance issues

- Switch Impedance
- Transition
- Track/Hold Transition
- Actual Switch Transition

Diagram showing
- $V_{IN}$
- $V_{OUT}$
- $R_{SW}$
- $R_{SWON}$
- $t_D$, $t_A$
Switch impedance issues

- Track/Hold Transition usually not of concern if fast fall time on switch
- Switch impedance effects can be managed by making $R_{SW}$ small
- Bottom-plate sampling does not introduce distortion