Integrated Filters and Amplifiers

- Integrators
- OTA-C Filters
- Switched-Capacitor Filters
- Voltage Amplifiers
Typical Filter Implementation

Biquads often LP or BP
Typical Biquad Implementation (Two-Integrator Loop)

\[ T(s) = \frac{-l_0^2}{s^2 + \alpha l_0 s + l_0^2} \]

Accurate control of \( l_0 \) and \( \alpha \) is essential for building most filters!
Observation:

- The integrator is the key building block in most filters
- Accuracy of $I_0$ and $\alpha$ is important!
RC Biquadratic Filter

\[
V_{IN} \rightarrow \frac{-I_0}{s + αI_0} \rightarrow \frac{-I_0}{s} \rightarrow -1 \rightarrow X_{OUT}
\]

\[
\text{Review from last lecture.}
\]
What happens if accuracy is not attained?

With process variations of +/- 20% in sheet resistance and another +/-15% variation in resistance with temperature, variability of R is several orders of magnitude too large.

Process variations in C are in the +/- 20% range as well.

Unacceptable performance (variability in I₀ orders of magnitude too large!) No market opportunity!
Economic Implications

If $I_0 = 1\text{KRad}/\text{Sec}$ and $C = 1\text{pF}$, how large must $R$ be?

$$R = \frac{1}{I_0 C} = 10^9$$

If sheet resistance is 30 ohms/square, one resistor requires 33 million squares!
Challenges in Integrated Filter Design

- Accuracy of components is not good enough (orders of magnitude)
- Area too large for audio frequencies (orders of magnitude)
Challenges in Integrated Filter / Integrated Integrator Design

- Accuracy of R and C difficult to accurately control – particularly in integrated applications
- Size of R and C unacceptably large if $I_0$ is in audio frequency range
- Amplifier GB limits performance

\[ T(s) = -\frac{1}{RCs} \]
\[ I_0 = \frac{1}{RC} \]
Consider the following two circuits

\[ Q_{RC} = -\frac{v_{IN}(t_1)}{R} T \quad Q_{SC} = -C_1 \cdot v_{IN}(t_1) \]

Thus equating charges

\[ Q_{RC} \approx Q_{SC} \]

Obtain the equivalent resistance of the switched-capacitor circuit

\[ R_{EQ} = \frac{T}{C_1} \]
Thus, if *clocked* with a clock period of $T$, for $T \ll T_{SIG}$, we have the following equivalence:

$$R_{EQ} \approx \frac{T}{C_1}$$

Equivalence of a switched capacitor and a resistor has been known for over 100 years. Up until 1977, this knowledge was of little practical significance.
The switched-capacitor integrator

\[ R_{EQ} = \frac{T}{C_1} \]

But what about the challenges of integrating the active RC integrator?

- Accuracy of \( R \) and \( C \) difficult to accurately control – particularly in integrated applications
- Size of \( R \) and \( C \) unacceptably large if \( I_0 \) is in audio frequency range
- Amplifier GB limits performance

Large resistors require small capacitors (since \( C_1 \) appears in denominator)!
The switched-capacitor integrator

\[ R_{\text{EQ}} = \frac{T}{C_1} \]

\[ I_0 = \frac{1}{R_{\text{EQ}} C} \quad \Rightarrow \quad I_0 = T^{-1} \cdot \left( \frac{C_1}{C} \right) \quad \Rightarrow \quad I_0 = f_{\text{CLK}} \left( \frac{C_1}{C} \right) \]

- Capacitor ratios can be maintained to the 0.1% accuracy level or better
- Very accurate clocks can be inexpensively generated
- GB requirements for Op Amp actually relaxed with SC integrator compared to active RC integrator
The switched-capacitor integrator

\[ V_{\text{OUT}} \]
\[ V_{\text{IN}} \]
\[ C_1 \]
\[ \varphi_1 \]
\[ \varphi_2 \]
\[ T \]
\[ t_1 \]
\[ t_1 + T \]

\[ R_{\text{EQ}} = \frac{T}{C_1} \]

But what about the challenges of integrating the active RC integrator?

- Accuracy of R and C difficult to accurately control – particularly in integrated applications
- Size of R and C unacceptably large if I_0 is in audio frequency range
- Amplifier GB limits performance

Switched-Capacitor Integrators offers orders of magnitude improvement in first two major challenges!
The switched-capacitor integrator

\[
R_{EQ} = \frac{T}{C_1}
\]

\[
l_0 = \frac{1}{R_{EQ}C}
\]

\[
l_0 = f_{CLK} \left( \frac{C_1}{C} \right)
\]
The switched-capacitor (SC) integrator

\[ V_{OUT} = f_{CLK} \left( \frac{C_1}{C} \right) \]

Non-overlap of clocks is critical in SC circuits
Switched-Capacitor Filter

$T_{CLK} \ll T_{SIG}$

$V_{IN}$  $\Phi_1$  $\Phi_2$  $C_1$  $C$  $V_{OUT}$  $V_{OUT}$

$t_1$  $t_1 + T_{CLK}$

$\Phi_1$  $\Phi_2$

$T_{SIG}$

$T_{CLK}$

$V_{IN}$  $V_{OUT}$
Basic Building Blocks in Both Cascaded Biquads and Multiple Feedback Structures

- Developed from observations from feedback implementations
  1. Integrators
  2. Summers
  3. First-order filter blocks
  4. Biquads
  5. Switches

- Same building blocks used in open-loop applications as well
Switched-Capacitor Filters

What if $T_{\text{CLK}}$ is not much much smaller than $T_{\text{SIG}}$?

For $T_{\text{CLK}} \ll T_{\text{SIG}}$
Switched-Capacitor Filters

What if $T_{\text{CLK}}$ is not much-much smaller than $T_{\text{SIG}}$?

For $T_{\text{CLK}}<<T_{\text{SIG}}$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

For $T_{CLK} \ll T_{SIG}$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} \ll T_{SIG}$

Define $T = T_{CLK}$

Considerable change in $V(t)$ in clock period
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$

\[ T_{CLK} \quad T_{SIG} \]

\[ \phi_1 \quad \phi_2 \]
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$

$V(nT)$

$V((n+1)T)$

$V_0(nT+T) = V_0(nT) + \frac{\Delta Q}{C}$

but - ◆ $Q$ is the charge on $C_1$ at the time $\varphi_1$ opens

◆ $Q \simeq C_1 V_{IN}(nT+T/2)$

\[ \therefore V_{OUT}(nT+T) = V_{OUT}(nT) - \left( \frac{C_1}{C} \right) V_{IN}(nT+T/2) \]

If an input S/H, $V_{IN}$ constant over periods of length $T$ thus, assume $V_{IN}(nT+T/2) \simeq V_{IN}(nT)$

So obtain

$V_{OUT}(nT+T) = V_{OUT}(nT) - \left( \frac{C_1}{C} \right) V_{IN}(nT)$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

This is a difference equation relating $V_{OUT}(nT)$ to $V_{IN}(nT)$

Coefficients in difference equation are all accurately controlled!

Difference equation is highly insensitive to process variations and temperature variations!
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

Taking the z-transform we obtain

$$v_{OUT}(nT+T) = v_{OUT}(nT) - \left(\frac{C_1}{C}\right)v_{IN}(nT)$$

$$zv_{O} = v_{O} - \left(\frac{C_1}{C}\right)v_{IN}$$

$$I(z) = \frac{v_{O}}{v_{IN}} = -\left(\frac{C_1}{C}\right)\frac{1}{z-1}$$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

$$V_{OUT}(nT+T) = V_{OUT}(nT) - \left(\frac{C_1}{C}\right)V_{IN}(nT)$$

$$I(z) = \left(\frac{C_1}{C}\right)\frac{1}{z-1}$$

- Switched-capacitor circuits are analyzed in the $z$-domain rather than in the $s$-domain.
- Coefficients are precisely controlled with small area even if $T_{CLK}$ is not much smaller than $T_{SIG}$.
- Assumption of input S/H is really not necessary.
- Often no underlying Active RC circuit (direct synthesis in the discrete domain).
- SC circuits are discrete-time continuous-amplitude circuits.
Switched-Capacitor Filters

Parasitic Capacitances

Parasitic capacitances are large, do not match, and most are nonlinear!
Switched-Capacitor Filters

Parasitic Capacitances

Parasitics affecting charge transfer are indicated

\[ V_{OUT}(nT+T) = V_{OUT}(nT) - \left( \frac{C_1+CP}{C} \right) V_{IN}(nT) \]

- Can affect the ratio \( C_1/CP \) by 30% or more
- Most of the accuracy improvements offered by SC technique lost in parasitics!
Switched-Capacitor Filters

Consider:

\[ V_{OUT}(nT+T) = V_{OUT}(nT) + \left( \frac{C_1}{C} \right) V_{IN}(nT) \]

with input S/H

\[ I(z) = \frac{\left( \frac{C_1}{C} \right)}{z-1} \]

- Performs as a noninverting integrator
- Note simple noninverting integrator function without need for extra op amp
- Requires extra switches
- Has many more parasitics
Switched-Capacitor Filters

Parasitic Capacitances
Switched-Capacitor Filters

Parasitics affecting charge transfer are indicated

- Effects of all parasitic capacitances have been essentially eliminated!
- Termed a stray-insensitive or parasitic-insensitive structure
- Widely used as a noninverting SC integrator
Switched-Capacitor Filters

Consider the following SC circuit

\[ V_{OUT}(nT+T) = V_{OUT}(nT) - \left[ \frac{C_1}{C} \right] V_{IN}(nT+T) \]

with input S/H

\[ I(z) = - \frac{z \left( \frac{C_1}{C} \right)}{z-1} \]

Serves as inverting stray-insensitive SC integrator
Switched-Capacitor Filters

Summing inputs  (any number of summing inputs can be used)

(Shown stray-sensitive to reduce schematic complexity only)
Switched-Capacitor Filters

Lossy inverting integrator

\[ V_{OUT}(nT+T) = V_{OUT}(nT) - \left( \frac{C_2}{C} \right) V_{IN}(nT) - \left( \frac{C_1}{C} \right) V_{IN}(nT) \]

\[ \frac{V_{OUT}(z)}{V_{IN}(z)} = I(z) = \frac{z \left( \frac{C_1}{C} \right)}{z - \left( 1 - \frac{C_2}{C} \right)} \]

(Shown stray-sensitive to reduce schematic complexity only)
Switched-Capacitor Filters

Summing Lossy inverting integrator

(Shown stray-sensitive to reduce schematic complexity only)
Switched-Capacitor Filters

Stray Insensitive Lossy Integrator with inverting and noninverting summing inputs

\[ V_{\text{OUT}}(nT+T) = V_{\text{OUT}}(nT) - \left( \frac{C_3}{C} \right) V_{\text{OUT}}(nT+T) + \left( \frac{C_1}{C} \right) V_{\text{IN1}}(nT+T) - \left( \frac{C_2}{C} \right) V_{\text{IN2}}(nT+T) \]

\[ V_{\text{OUT}}(z) = \frac{z \left( \frac{C_1}{C} \right) V_{\text{IN1}} - z \left( \frac{C_2}{C} \right) V_{\text{IN2}}}{\left( 1 + \frac{C_3}{C_1} \right) z - 1} \]
Observation:

• The integrator is the key building block in most filters

• Accuracy of $I_0$ and $\alpha$ is important!

• Most integrated filters are built with integrators, lossy integrators and summers

Have practical method of building integrated audio frequency filters!

Practical summers might still be useful
Typical Filter Implementation

Biquads often LP or BP
Typical Biquad Implementation
(Two-Integrator Loop)

\[ T(s) = \frac{-I_0^2}{s^2 + \alpha I_0 s + I_0^2} \]

Accurate control of \( I_0 \) and \( \alpha \) is essential for building most filters!
Switched-Capacitor Amplifiers

Noninverting Amplifier

$$A_V = \frac{C_1}{C}$$

- Accurate control of gain is possible (0.1% or better) but extreme care to detail in layout and statistical analysis for adequate area allocation is necessary
- Stray-insensitive structures

Inverting Amplifier

$$A_V = -\frac{C_1}{C}$$
Switched-Capacitor Amplifiers

Noninverting Amplifier

$$A_V = \frac{C_1}{C}$$

Inverting Amplifier

$$A_V = -\frac{C_1}{C}$$

Bottom-plate sampling with advanced clock reduces signal-dependent gain errors when $V_{IN}$ is time varying: Sample and Hold
Switched-Capacitor Amplifiers

Summing Inverting and Noninverting Amplifier

\[ V_{OUT} = \frac{C_1}{C} V_{IN1} - \frac{C_2}{C} V_{IN2} \]

(modification for bottom-plate sampling needed if \( V_{IN} \) is time varying: track and hold)
Switched-Capacitor Amplifiers

Flip-Around Amplifier

\[ A_V = 1 + \frac{C_1}{C_2} \]

(modification for bottom-plate sampling needed if \( V_{IN} \) is time varying: track and hold)
Switched-Capacitor Amplifiers

$$V_{OUT} = V_{IN1} \left(1 + \frac{C_1}{C_2}\right) - V_{IN2} \left(\frac{C_1}{C_2}\right)$$

Flip-Around Subtracting Amplifier

(modification for bottom-plate sampling needed if $V_{IN}$ is time varying: track and hold)
Switched-Capacitor Amplifiers

Consider the following circuit

\[
\begin{align*}
V_{IN} & \quad \Phi_1 + \Phi_3 \\
\Phi_2 & \quad C_1 \\
\Phi_4 & \quad \Phi_1 + \Phi_2 + \Phi_4 \\
C_2 & \quad \Phi_1 + \Phi_2 \\
V_{OUT} & \quad \Phi_4
\end{align*}
\]
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_1$

$$Q_{C1} = C_1 V_{IN}$$
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_2$

from $\Phi_1$ $Q_{C1} = C_1 V_{IN}$

during $\Phi_2$ $Q_{C1} = 0$ $Q_{C2} = C_1 V_{IN}$
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_3$

- From $\Phi_2$: $Q_{C1}=0$, $Q_{C2}=C_1V_{IN}$
- During $\Phi_2$: $Q_{C1}=C_1V_{IN}$, $Q_{C2}=C_1V_{IN}$
Switched-Capacitor Amplifiers

Consider the following circuit

During phase $\Phi_4$.

From $\Phi_3$, $Q_{C1} = C_1 V_{IN}$

During $\Phi_2$, $Q_{C2} = 0$, $Q_{C1} = 2C_1 V_{IN}$

Thus $V_{OUT} = Q_{C1}/C_1 = 2V_{IN}$
Switched-Capacitor Amplifiers

Consider the following circuit

\[ A_V = 2 \]

Gain of 2 obtained without requiring any matching of components
Top-Plate vs Bottom-Plate Sampling

Top-Plate Sampling

Bottom-Plate Sampling
Top-Plate vs Bottom-Plate Sampling

Top-Plate Sampling

- $V_{IN}$
- $\Phi_1$
- $C$
- $V_{OUT}$

Bottom-Plate Sampling

- $V_{IN}$
- $C$
- $\Phi_1$
- $V_{OUT}$

Waveforms:

- $\Phi_{1A}$
- $\Phi_1$
- $\Phi_2$

Timing:

- $nT$ to $(n+1)T$
Top-Plate Sampling

- Actual sample taken at $t_A$
- Sampled-value is signal-level dependent
- Equivalent to a signal-dependent jitter on sampling clock
- Causes serious nonlinear distortion if signal frequency is high
• Actual sample taken at $t_A$
• $t_A - t_D$ is independent of $V_{IN}(t)$
• Dramatic reduction in nonlinear distortion and signal-dependent sampling error
• Effectively causes a constant phase shift in sampling time
Bottom-Plate Sampling

\[ \phi_1 \quad C_1 \quad \phi_2 \]

\[ \phi_2 \quad \phi_{1A} \]

\[ V_{IN} \quad V_{OUT} \]
Bottom-Plate Sampling

 Expanded time axis:
Bottom-Plate Sampling

Further expanded time axis ($V_{IN}$ change exaggerated to show effects):

- $V_{IN}(t_D)$
- $V_{IN}(t_A)$
- $V_{T}$
- $t_D$ and $t_A$
Bottom-Plate Sampling

- Actual sample taken at $t_A$
- $t_A - t_D$ is independent of $V_{IN}(t)$
- Some very small change in $V_{OUT}$ will occur until $\Phi_1$ opens
- Time $\Phi_1$ opens is input signal-level dependent

$C_T$ and $C_B$ are parasitic capacitances that appear at nodes connected to top plate and bottom plate of $C$
Bottom-Plate Sampling

\[ V_{OUT}(t_D) \]
\[ V_{OUT}(t_A) \]
\[ V_{IN}(t_T) \]

\[ V_{OUT}(t_T) = V_{IN}(t_A) + \left( \frac{C_B}{C+C_B} \right) \left( V_{IN}(t_T) - V_{IN}(t_A) \right) \]

but:

\[ V_{OUT}(t_A) = V_{IN}(t_A) \]

can be rewritten as:

\[ V_{OUT}(t_T) = V_{IN}(t_A) \left[ \frac{C}{C+C_B} \right] + \left( \frac{C_B}{C+C_B} \right) V_{IN}(t_T) \]

- Small gain error on sampling \( V_{IN} \) at \( t_A \)
- Dependent upon \( V_{IN}(t_T) \) which causes small distortion in sample
- \( C_B \) can be a reasonable percentage of \( C \) so advanced clock does not completely solve the sampling time problem
Consider the entire SC amplifier

\[ V_{C_1}(t_T) = V_{IN}(t_A) \left( \frac{C_1}{C_1 + C_B} \right) + \left( \frac{C_B}{C_1 + C_B} \right) V_{IN}(t_T) \]

Likewise:

\[ V_{C_B}(t_T) = \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_T) - \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_A) \]

Thus charges stored on \( C_1 \) and \( C_B \) at \( t_T \) are

\[ Q_{C_1}(t_T) = C_1 V_{IN}(t_A) \left( \frac{C_1}{C_1 + C_B} \right) + C_1 \left( \frac{C_B}{C_1 + C_B} \right) V_{IN}(t_T) \]

\[ Q_{C_B}(t_T) = C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_T) - C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_A) \]
Consider the entire SC amplifier

\[ Q_{C_1}(t_T) = C_1 V_{IN}(t_A) \left[ \frac{C_1}{C_1 + C_B} \right] + C_1 \left( \frac{C_B}{C_1 + C_B} \right) V_{IN}(t_T) \]

\[ Q_{C_B}(t_T) = C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_T) - C_B \left( \frac{C_1}{C_1 + C_B} \right) V_{IN}(t_A) \]

During \( \Phi_2 \), these capacitors are both discharged and the charge on feedback capacitor \( C \) becomes

\[ Q_C = Q_{C_1} - Q_{C_B} \]

It thus follows that

\[ Q_C(t_T) = C_1 V_{IN}(t_A) \]

- Extra charge accumulated on \( C_1 \) until the top switch opened equal to charge accumulated on \( C_B \)
- For switching scheme used here, effects precisely cancel when charge is transferred to \( C \)
Consider the entire SC amplifier

\[ Q_c(t_T) = C_1 V_{IN}(t_A) \]

Thus:

\[ V_{OUT}(t_T) = \frac{Q_C(t_T)}{C} = \frac{C_1}{C} V_{IN}(t_A) \]

As predicted the output voltage is not a function of \( t_T \) and thus the parasitic capacitance on the bottom Plate does not affect performance when bottom plate sampling is used.
Switch impedance issues

When in track mode, non-zero $R_{SW}$ causes small amplitude decrease and phase shift but no nonlinear distortion provided $R_{SW}$ is not signal-level dependent.

Top-plate switch ($R_{SW}$ or $R_{SWT}$) is signal level dependent if implemented with simple transistor.

Bottom-plate switch ($R_{SWB}$) is not signal-level dependent.

Make $R_{SW}$ and $R_{SWT}$ sufficiently small to avoid distortion.

\[ T(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{1}{1 + R_{SW} C s} \]

\[ |T(j\omega)| = \frac{1}{\sqrt{1 + (R_{SW} C \omega)^2}} \]

\[ \angle T(j\omega) = -\tan^{-1}\left(\frac{\omega R_{SW} C}{1}\right) \]
Switch impedance issues

When transitioning from track mode to hold mode, switch impedance increases rapidly from non-zero $R_{SW}$.
Switch impedance issues

Amplitude and phase shift for bottom-plate sampler (difficult to distinguish between phase and amplitude effects in this zoom)
Switch impedance issues

\[ V_{\text{IN}}(t_A) \]

\[ V_{\text{OUT}}(t_A) \]

\[ V_{\text{IN}} \]

\[ V_{\text{OUT}} \]

\[ t_D \]

\[ t_A \]

\[ R_{\text{SW}} \]

\[ R_{\text{SWON}} \]

\[ \Phi_1 \]

Ideal Switch Transition

Track

Hold
Switch impedance issues
Switch impedance issues

- Track/Hold Transition usually not of concern if fast fall time on switch
- Switch impedance effects can be managed by making $R_{SW}$ small
- Bottom-plate sampling does not introduce distortion
End of Lecture 44