EE 435
Lecture 44

• Phased Locked Loops and VCOs
• Over Sampled Data Converters
• Switched Capacitor Filters

Course Evaluation Reminder    - All Electronic

Thanks to Yia Yu Hong for the following summary of clever solutions to data converter challenges

Q1: Mismatch of Resistor

1. Local random variation
   ans: Increase area but keep ratio \(\frac{W_1}{W_2}\)

2. Gradient effects
   ans: Common central layout/combination of a dual ladder with matrix organization

Q2: Switch have different impedance

\[
R_{eq} = \frac{1}{\frac{1}{R_{int}} + \frac{1}{R_{on}} (V_{n5} - V_t)}
\]

different Vss will affect Vth.

ans: Use supply ladder to change Vth and fix Vth.

note: we can group Vth, which means several switches share one Vth \(\Rightarrow\) less area.
Q: 1. When latch is on different position will have different Req. Different Req. when M1 is on, Req = R1/(Rm1 + R1).
   M100 is on, Req = 100 R/1(Rm100 + R100)

Answer: Use perigon structure. Add Req in series with switch.

Q: 2. M1 is on, Req = R1/(Rm1 + R1).
   M100 is on, Req = 100 R/1(Rm100 + R100)

when Req is fixed, transient time will be the same.

Decoder can get very large, 2^n.
Ans: To use tree decoder (not for large bits, because of parasitic capacitors).

Q: 2. Folder structure.
\[ \beta = \frac{R_{E1}}{R_{E1} + H_{RF}} \]

when \( \beta \) is changing, its response time is code dependent.

Answer: Bottom plate switched.

QNS: Segmental Structure

INL is good because resistor is unit cell, but DNL has problem.

eg. 0 1

0 0

QNS: Binary Coded Array - have acceptable DNL under tests.
A. Current Source

Need some time to charge up capacitor

And steering current

when $Q$ is high, current through $M_2$
when $Q$ is high, current through $M_1$.

don't have to charge up or discharge any capacitor, so it is very useful.

A: system could not shut down to refresh each time
not sure for gate capacitance one by one.

Ans. Dynamic Current Source Matched

Force $I = I_{ref} \Rightarrow$ constant current

$P_1$ is y-wich ($P-$junction)
Current leak
A switched capacitor acts as a resistor.

During q₁:
\[ Q_{C_1} = C_{IN} V_{IN} \]
\[ Q_{C} = 0 \]

During q₂:
\[ Q_{C} = V_{OUT} \Rightarrow \frac{C_{IN} V_{IN}}{C} = V_{OUT} \]

Note: It's like multiplying by \( \frac{C}{C_{IN}} \) but it's not.
Often the LF is low order

Example: Assume $N=1$ and 

$$T_{LF}(s) = \frac{1}{1+RCs}$$

Review from Last Lecture
Voltage Controlled Oscillators

Many different VCOs can be used

Integrator-Based VCO

\[
\begin{align*}
-\frac{l_0}{s} & \rightarrow -\frac{l_0}{s} & \rightarrow -\frac{l_0}{s} & \rightarrow X_{out}
\end{align*}
\]

Lossy Integrator-Based VCO

\[
\begin{align*}
-\frac{l_0}{s+\alpha} & \rightarrow -\frac{l_0}{s+\alpha} & \rightarrow -\frac{l_0}{s+\alpha} & \rightarrow X_{out}
\end{align*}
\]
Voltage Controlled Oscillators

$I_{0d}(s) = \frac{g_{m1}}{sC_X}$

Integrator-based VCO

$I_{0d}(s) = \frac{g_{m1}}{sC_X + g_{m3}}$

Lossy Integrator-based VCO
Voltage Controlled Oscillators

Relaxation Oscillator Derived VCO

Voltage Controlled Oscillator (VCO)

Can have either triangle wave or square wave outputs
Phase Detectors

Many different Phase Detectors can be used

Some Popular Phase Detector Circuits
- Analog Multiplier
- Exclusive OR Gate
- Sample and Hold
- Charge Pump

Charge-pump based Phase Detector

Average $I_{OUT}$ is the average phase
Phase Detectors

Many different Phase Detectors can be used

\[ \Phi_D \]

Region of Operation

Average \( I_{OUT} \) is the average phase

Region of Operation

Region of Operation
Phase Detectors

Phase Detector (Φ_D)

Average \( I_{OUT} \) is the average phase

\[ \Delta \phi = \begin{cases} 0 & \Delta \phi > 0 \\ \phi_s & \Delta \phi < 0 \end{cases} \]
Phase Detectors

Phase Detector ($\Phi_D$)

Average $I_{OUT}$ is the average phase

Vulnerable to dead zone problem
Loop Filters

Many different Phase Detectors can be used
Often the loop filter is first or second order
Usually the loop filter circuit is very simple

Basic first-order LF with average current difference as input
What is the phase of a signal?

\[ V_1 = V_{M1}\sin(\omega_1 t + \phi_1) \]

\[ V_2 = V_{M2}\sin(\omega_2 t + \phi_2) \]

Phase Detector \((\Phi_D)\)

Assume \( \omega_1 = \omega_2 = \omega \)

If \( V_1 \) can be expressed as \( V_1 = V_{M1}\sin(\omega t + \phi_1) \) the phase is \( \phi_1 \)

But what is the phase if \( \omega \) is time varying? Or what is the “phase” if this functional form does not really characterize \( V(t) \)? Or what if \( \omega_1 \neq \omega_2 \)?

What does a phase detector do if the two inputs are not at the same frequency?
What is the phase of a signal?

\[ V_1 = V_{M1} \sin(\omega_1 t + \phi_1) \]

\[ V_2 = V_{M2} \sin(\omega_2 t + \phi_2) \]

Most Phase Detectors are actually Phase/Frequency Detectors

- Large output when frequency difference exists
- Also provides output when phase difference exists after frequencies are matched
Basic Architecture of Over Sampled ADC

![Diagram of Sigma-Delta Modulator and Over Sampling ADC](image-url)
Basic Architecture of Over Sampled ADC

Sigma-Delta Modulator
VIN
Modulator Filter
ADC
DAC
Filter and Decimator
XOUT
n
Vin
Modulator Filter
ADC
DAC
Filter and Decimator
XOUT
n
Single-Bit Sigma-Delta Modulator with First-Order Noise Filter

Figure 4: Block diagram of a sigma-delta modulator.
Spectrum showing quantization noise
Over-Sampled Spectrum showing quantization noise

Goal: Filter Out Quantization Noise without affecting Signal
Over-Sampled Spectrum showing quantization noise with digital lowpass filter

Lowpass Filter

Removed Quantization Noise

Residual Quantization Noise if Filter Band-edge at 0.5f_S
Over-Sampled Spectrum showing quantization noise with digital low-pass filter

- Oversampling ratio is how much higher sampling rate is than Nyquist rate
- If Nyquist rate is $f_S$, OSR is $k$ in this figure
Over-Sampled Spectrum showing quantization noise with digital low-pass filter

Assume $A_i$ is the magnitude of the DFT coefficient of the noise at index $i$ and $N$ is the number of samples in the DFT, the RMS noise voltage is given by

$$V_{RMS} = \sqrt{\frac{1}{2k} \sum_{i=1}^{N} A_i^2}$$

If we assume that all DFT noise coefficients are equal to $A_{NN}$

$$V_{RMS} = \sqrt{\frac{1}{2k} \sum_{i=1}^{N} A_i^2} = A_{NN} \sqrt{\frac{N}{2k}}$$

If we pass the digital output to a digital filter with a band-edge of $\theta k_f S/2$ the residual quantization noise is

$$V_{RMS-\text{RESIDUAL}} = \sqrt{\frac{1}{2k} \sum_{i=1}^{\theta N} A_i^2} = A_{NN} \sqrt{\frac{\theta N}{2k}} = \sqrt{\theta} \cdot V_{RMS}$$
Over-Sampled Spectrum showing quantization noise with digital low-pass filter

\[ V_{RMS-RESIDUAL} = \sqrt{\theta \cdot V_{RMS}} \]

If \( 0.5\theta k_f S = f_S/2 \) then the OSR is given by \( k=1/\theta \)

if the OSR is \( k=4 \), the quantization noise will be reduced by a factor of 2
If the OSR is \( k=16 \), the quantization will be reduced by a factor of 4

More generally, every factor of 4 increase in the OSR reduces the quantization noise by a factor of 2 or, equivalently, every factor of 4 increase in the OSR reduces the quantization noise by 6dB
Noise Shaping

If the noise is “shaped” first, before it is passed through the low-pass digital filter, even more reduction in the quantization noise can be achieved.

See Martin and Johns for a discussion of how the noise can be shaped without affecting the signal in a delta-sigma modulator.
Noise Shaped Spectrum

- **Power**
- **Signal amplitude**

The integrator serves as a highpass filter to the noise.

The result is noise shaping.
Filtering the Shaped Noise

Power

Signal amplitude

Digital filter response

HF noise removed by the digital filter

$k F_s / 2$

$k F_s$
Typical Biquad Filter Implementation
(Two-Integrator Loop)

\[ \begin{align*}
T(s) &= \frac{-I_0^2}{s^2 + \alpha I_0 s + I_0^2} \\
X_{IN} &\rightarrow + \left( \frac{-I_0}{s} \right) \rightarrow \frac{I_0}{s} \rightarrow X_{OUT}
\end{align*} \]

Accurate control of \( I_0 \) and \( \alpha \) is essential for building most filters!
Typical Filter Implementation

Biquads often LP or BP
Integrated Filters

- The integrator is the key building block in most filters
- Accuracy of $I_0$ is important!
- Most integrated filters are built with integrators, lossy integrators and summers

\[
A_{\text{INT}}(s) = \frac{V_{\text{OUT}}(s)}{V_{\text{IN}}(s)} = -\frac{I_0}{s}
\]

\[
l_0 = \frac{1}{RC}
\]

If $I_0 = 1 \text{KRad/Sec}$ and $C = 1 \text{pF}$, how large must $R$ be?

\[
R = \frac{1}{I_0C} = 10^9
\]

If sheet resistance is 30 ohms/square, one resistor requires 33 million squares!
Challenges in Integrated Filter Design

• Accuracy of components is not good enough (orders of magnitude)
• Area too large for audio frequencies (orders of magnitude)
Challenges in Integrated Filter / Integrated Integrator Design

- Accuracy of R and C difficult to accurately control – particularly in integrated applications
- Size of R and C unacceptably large if $I_0$ is in audio frequency range
- Amplifier GB limits performance

$T(s) = -\frac{1}{RCs}$

$I_0 = \frac{1}{RC}$
Consider the following integrator circuit:

\[ Q_{RC} = \int_{t=t_1}^{t_1+T} i(t) dt = -\frac{1}{R} \int_{t=t_1}^{t_1+T} V_{IN}(t) dt \]

\[ V_{OUT}(t_1+T) = V_{OUT}(t_1) - \frac{Q_{RC}}{C} \]

If \( T \ll T_{SIG} \)

\[ V_{IN}(t) \approx V_{IN}(t_1) \quad \text{for} \quad t_1 < t < t_1 + T \]
Consider the following circuit

\[
\begin{align*}
Q_{RC} &= -\int_{t=t_1}^{t_1+T} i(t) \, dt = -\frac{1}{R} \int_{t=t_1}^{t_1+T} v_{IN}(t) \, dt \\
&\approx -\frac{v_{IN}(t_1)}{R} \int_{t=t_1}^{t_1+T} 1 \, dt \\
&= -\frac{v_{IN}(t_1)}{R} T
\end{align*}
\]

\[
\begin{align*}
v_{OUT}(t_1+T) &= v_{OUT}(t_1) - \frac{Q_{RC}}{C} \\
&\approx v_{OUT}(t_1) - \frac{v_{IN}(t_1)}{RC} T
\end{align*}
\]

If $T \ll T_{SIG}$
Consider the following circuit

\[ Q = C \left( t - \frac{V}{V_{\text{OUT}}} \right) \]

If \( T \ll T_{\text{SIG}} \)

\[ Q_{\text{SC}} = -C_1 \cdot V_{\text{IN}}(t_1) \]

\[ V_{\text{OUT}}(t_1 + T) = V_{\text{OUT}}(t_1) - \frac{Q_{\text{SC}}}{C} \approx V_{\text{OUT}}(t_1) - V_{\text{IN}}(t_1) \frac{C_1}{C} \]
Consider the following two circuits

\[ Q_{SC} = -C_1 \cdot V_{IN}(t_1) \]

Both transfer charge proportional to \( V_{IN}(t_1) \)

\[ Q_{RC} \approx -\frac{V_{IN}(t_1)}{R}T \]
Consider the following two circuits

\[ Q_{RC} \approx -\frac{v_{IN}(t_1)}{R} T \]
\[ Q_{SC} = -C_1 \cdot v_{IN}(t_1) \]

Thus equating charges

\[ Q_{RC} \approx Q_{SC} \]

Obtain the equivalent resistance of the switched-capacitor circuit

\[ R_{EQ} \approx \frac{T}{C_1} \]
Thus, if clocked with a clock period of \( T \), for \( T \ll T_{\text{SIG}} \), we have the following equivalence:

\[
R_{\text{EQ}} \approx \frac{T}{C_1}
\]

Equivalence of a switched capacitor and a resistor has been known for over 100 years. Up until 1977, this knowledge was of little practical significance.
The switched-capacitor integrator

\[ V_{OUT} = \frac{1}{C_1} \int V_{IN} \, dt \]

But what about the challenges of integrating the active RC integrator?

- Accuracy of R and C difficult to accurately control – particularly in integrated applications
- Size of R and C unacceptably large if \( I_0 \) is in audio frequency range
- Amplifier GB limits performance

Large resistors require small capacitors (since \( C_1 \) appears in denominator)!
The switched-capacitor integrator

\[ V_{OUT} \]
\[ V_{IN} \]
\[ C \]
\[ \phi_1 \]
\[ \phi_2 \]
\[ R \]
\[ t_1 \]
\[ t_1 + T \]

**Equation:**

\[ I_0 = \frac{1}{R_{EQ} C} \]

\[ I_0 = T^{-1} \cdot \left( \frac{C_1}{C} \right) \]

\[ I_0 = f_{CLK} \left( \frac{C_1}{C} \right) \]

- Capacitor ratios can be maintained to the 0.1% accuracy level or better
- Very accurate clocks can be inexpensively generated

- GB requirements for Op Amp actually relaxed with SC integrator compared to active RC integrator
The switched-capacitor integrator

\[ V_{OUT} \approx \frac{T}{C_1} \]

But what about the challenges of integrating the active RC integrator?

- Accuracy of R and C difficult to accurately control – particularly in integrated applications
- Size of R and C unacceptably large if \( I_0 \) is in audio frequency range
- Amplifier GB limits performance

Switched-Capacitor Integrators offers orders of magnitude improvement in first two major challenges! 
The switched-capacitor integrator

\[ V_{OUT} = V_{IN} C_1 \phi_1 \phi_2 \]

\[ R_{EQ} \approx \frac{T}{C_1} \]

\[ I_0 = \frac{1}{R_{EQ} C} \]

\[ I_0 = f_{CLK} \left( \frac{C_1}{C} \right) \]
The switched-capacitor (SC) integrator

Non-overlap of clocks is critical in SC circuits
Switched-Capacitor Filter

\[ V_{IN} \xrightarrow{\phi_1} C_1 \xrightarrow{C} V_{OUT} \]

\[ T_{CLK} \ll T_{SIG} \]

\[ T_{SIG} \]

\[ T_{CLK} \]

\[ \phi_1 \]

\[ \phi_2 \]
Basic Building Blocks in Both Cascaded Biquads and Multiple Feedback Structures

• Developed from observations from feedback implementations
  1. Integrators
  2. Summers
  3. First-order filter blocks
  4. Biquads
  5. Switches

• Same building blocks used in open-loop applications as well
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} << T_{SIG}$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much smaller than $T_{SIG}$?

For $T_{CLK} \ll T_{SIG}$
Switched-Capacitor Filters

What if $T_{\text{CLK}}$ is not much smaller than $T_{\text{SIG}}$?

For $T_{\text{CLK}} \ll T_{\text{SIG}}$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much smaller than $T_{SIG}$?

For $T_{CLK} << T_{SIG}$

$V(nT) \rightarrow V((n+1)T)$

$T = T_{CLK}$

Considerable change in $V(t)$ in clock period
Switched-Capacitor Filters

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$
Switched-Capacitor Filters

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$

$T_{CLK}$

$T_{SIG}$

$\phi_1$

$\phi_2$
Switched-Capacitor Filters

What if $T_{\text{CLK}}$ is not much much smaller than $T_{\text{SIG}}$?

For $T_{\text{CLK}} < T_{\text{SIG}}$

\[
V(nT) \quad \text{and} \quad V((n+1)T)
\]

\[\begin{align*}
\phi_1 & \quad nT_{\text{CLK}} \quad (n+1)T_{\text{CLK}} \\
\phi_2 & \quad T_{\text{CLK}} \\
\text{Define} & \quad T = T_{\text{CLK}}
\end{align*}\]

\[
V_0(nT+T) = V_0(nT) + \frac{\Delta Q}{C}
\]

but $-uQ$ is the charge on $C_1$ at the time $\phi_1$ opens

\[ -uQ \sim C_1 V_{\text{IN}}(nT+T/2) \]

\[ \therefore \quad V_{\text{OUT}}(nT+T) = V_{\text{OUT}}(nT) - \left(\frac{C_1}{C}\right) V_{\text{IN}}(nT+T/2) \]

If an input S/H, $V_{\text{IN}}$ constant over periods of length $T$

thus, assume $V_{\text{IN}}(nT+T/2) \sim V_{\text{IN}}(nT)$

So obtain

\[ V_{\text{OUT}}(nT+T) = V_{\text{OUT}}(nT) - \left(\frac{C_1}{C}\right) V_{\text{IN}}(nT) \]
Switched-Capacitor Filters

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

This is a difference equation relating $V_{OUT}(nT)$ to $V_{IN}(nT)$

$$V_{OUT}(nT+T) = V_{OUT}(nT) - \left(\frac{C_1}{C}\right) V_{IN}(nT)$$

Coefficients in difference equation are all accurately controlled!

Difference equation is highly insensitive to process variations and temperature variations!
Switched-Capacitor Filters

What if $T_{CLK}$ is not much smaller than $T_{SIG}$?

\[ V_{OUT}(nT+T) = V_{OUT}(nT) - \left( \frac{C_1}{C} \right) V_{IN}(nT) \]

Taking the z-transform we obtain

\[ zV_O = V_O - \left( \frac{C_1}{C} \right) V_{IN} \]

\[ I(z) = \frac{V_O}{V_{IN}} = \frac{-\left( \frac{C_1}{C} \right)}{z-1} \]
Switched-Capacitor Filters

What if $T_{CLK}$ is not much smaller than $T_{SIG}$?

$$V_{OUT}(nT+T) = V_{OUT}(nT) - \left(\frac{C_1}{C}\right)V_{IN}(nT)$$

$$I(z) = \frac{-\left(\frac{C_1}{C}\right)}{z-1}$$

- Switched-capacitor circuits are analyzed in the $z$-domain rather than in the $s$-domain.
- Coefficients are precisely controlled with small area even if $T_{CLK}$ is not much smaller than $T_{SIG}$.
- Assumption of input S/H is really not necessary.
- Often no underlying Active RC circuit (direct synthesis in the discrete domain).
- SC circuits are discrete-time continuous-amplitude circuits.
Switched-Capacitor Filters

Parasitic Capacitances

Parasitic capacitances are large, do not match, and most are nonlinear!
Switched-Capacitor Filters

Parasitic Capacitances

Parasitics affecting charge transfer are indicated

\[ V_{OUT}(nT + T) = V_{OUT}(nT) - \left( \frac{[C_1 + C_P]}{C} \right) V_{IN}(nT) \]

- Can affect the ratio \( C_1/C_P \) by 30% or more
- Most of the accuracy improvements offered by SC technique lost in parasitics!
Switched-Capacitor Filters

Consider:

\[ V_{OUT}(nT+T) = V_{OUT}(nT) + \left( \frac{C_1}{C} \right) V_{IN}(nT) \]

with input S/H

\[ I(z) = \frac{\left( \frac{C_1}{C} \right)}{z-1} \]

- Performs as a noninverting integrator
- Note simple noninverting integrator function without need for extra op amp
- Requires extra switches
- Has many more parasitics
Switched-Capacitor Filters

Parasitic Capacitances
Switched-Capacitor Filters

Parasitics affecting charge transfer are indicated

- Effects of all parasitic capacitances have been essentially eliminated!
- Termed a stray-insensitive or parasitic-insensitive structure
- Widely used as a noninverting SC integrator
Switched-Capacitor Filters

Consider the following SC circuit

\[ V_{OUT}(nT+T) = V_{OUT}(nT) - \left(\frac{C_1}{C}\right)V_{IN}(nT+T) \]

Serves as inverting stray-insensitive SC integrator

\[ I(z) = -\frac{z\left(\frac{C_1}{C}\right)}{z-1} \]
Switched-Capacitor Filters

**Summing inputs**  (any number of summing inputs can be used)

(Shown stray-sensitive to reduce schematic complexity only)
Switched-Capacitor Filters

Lossy inverting integrator

\[ V_{\text{OUT}}(nT+T) = V_{\text{OUT}}(nT) - \left( \frac{C_2}{C} \right)V_{\text{IN}}(nT) - \left( \frac{C_1}{C} \right)V_{\text{IN}}(nT) \]

\[
\frac{V_{\text{OUT}}(z)}{V_{\text{IN}}(z)} = I(z) = -\frac{z\left( \frac{C_1}{C} \right)}{z - \left( 1 - \frac{C_2}{C} \right)}
\]

(Shown stray-sensitive to reduce schematic complexity only)
Switched-Capacitor Filters

Summing Lossy inverting integrator

(Shown stray-sensitive to reduce schematic complexity only)
Switched-Capacitor Filters

Stray Insensitive Lossy Integrator with inverting and noninverting summing inputs

\[ V_{OUT}(nT+T) = V_{OUT}(nT) - (C_3/C)V_{OUT}(nT+T) + (C_1/C)V_{IN1}(nT+T) - (C_2/C)V_{IN2}(nT+T) \]

\[ V_{OUT}(z) = \frac{z \left( \frac{C_1}{C} \right) V_{IN1} - z \left( \frac{C_2}{C} \right) V_{IN2}}{\left( 1 + \frac{C_3}{C_1} \right) z - 1} \]
Observation:

• The integrator is the key building block in most filters

• Accuracy of $I_0$ and $\alpha$ is important!

• Most integrated filters are built with integrators, lossy integrators and summers

Have practical method of building integrated audio frequency filters!

Practical summers might still be useful
Typical Filter Implementation

Biquads often LP or BP
Typical Biquad Implementation
(Two-Integrator Loop)

\[ T(s) = \frac{-l_0^2}{s^2 + \alpha l_0 s + l_0^2} \]

Accurate control of \( l_0 \) and \( \alpha \) is essential for building most filters!
End of Lecture 44