EE 435

Lecture 5:

Fully Differential Single-Stage Amplifier Design
Review from last lecture:
Symmetric Networks

Theorem: If a linear network is symmetric, then for all differential symmetric excitations, the small signal voltage is zero at all points on the axis of symmetry.
Review from last lecture:

**Counterpart Networks**

Definition: The counterpart network of a network is obtained by replacing all n-channel devices with p-channel devices, replacing all p-channel devices with n-channel devices, replacing $V_{\text{SS}}$ biases with $V_{\text{DD}}$ biases, and replacing all $V_{\text{DD}}$ biases with $V_{\text{SS}}$ biases.
Review from last lecture:

Counterpart Networks

$V_{DD}$

$M_2$

the counterpart network is unique

$V_{SS}$

$M_1$

the counterpart of the counterpart is the original network
Review from last lecture:

Counterpart Networks

Theorem: The parametric expressions for all small-signal characteristics, such as voltage gain, output impedance, and transconductance of a network and its counterpart network are the same.
Review from last lecture:

Synthesis of fully-differential op amps from symmetric networks and counterpart networks

Theorem: If F is any network with a single input and P is its counterpart network, then the following circuits are fully differential circuits --- “op amps”.

\[ V_d = V_1 - V_2 \]
Synthesis of fully-differential op amps from symmetric networks and counterpart networks

A fully differential op amp is derived from any quarter circuit by combining it with its counterpart to obtain a half-circuit, combining two half-circuits to form a differential symmetric circuit and then biasing the symmetric differential circuit on the axis of symmetry.

Further, most of the properties of the operational amplifier can be obtained by inspection, from those of the quarter circuit.

Implications: Much Op Amp design can be reduced to designing much simpler quarter-circuits where it is much easier to get insight into circuit performance.
Review from last lecture:
Determination of op amp characteristics from quarter circuit characteristics

Small signal Quarter Circuit

\[ I_{XX} \quad V_{IN} \quad F \quad V_{OUT} \quad V_{SS} \]

Small signal differential amplifier

\[ \begin{align*}
A_{\text{voqc}} &= -\frac{G_M}{G} \\
\text{BW} &= \frac{G}{C_L} \\
\text{GB} &= \frac{G_M}{C_L}
\end{align*} \]

\[ \begin{align*}
A_v &= \frac{-G_{M1}}{2(G_1 + G_2)} \\
\text{BW} &= \frac{G_1 + G_2}{C_L} \\
\text{GB} &= \frac{G_{M1}}{2C_L}
\end{align*} \]

Note: Factor of 4 reduction of gain
Comparison of Tail Voltage and Tail Current Source Structures

Review from last lecture:

Small signal half-circuits are identical so voltage gains, BW, and GB are all the same
Review from last lecture:

Biasing Issues for Differential Amplifier

- Tail voltage bias not suitable for large common-mode (CM) input range but does offer good output swing

- Tail current bias provides good CM input range but at the expense of a modest reduction in output signal swing
Differential Output Amplifiers

Review from last lecture:

Single-Ended Outputs

- Differential Voltage Gain Double that of Single-Ended Structure
- BW is the same
- GB Doubles for the Differential Output Structure
Review from last lecture:
Single-stage single-input low-gain op amp

Basic Structure

Quarter Circuit

Counterpart Circuit

Practical Implementation
Review from last lecture:

Small signal model of half-circuit

\[ G = G_1 + G_2 \]
\[ G_M = G_{M1} \]
Review from last lecture:

Single-stage low-gain differential op amp

Quarter Circuit

Single-Ended Output : Differential Input Gain

\[
A(s) = \frac{-g_{m1}}{2} \frac{2}{sC_L + g_{o1} + g_{o3}}
\]

\[
A_o = \frac{2}{g_{o1} + g_{o3}} \frac{g_{m1}}{g_{o1} + g_{o3}}
\]

\[
GB = \frac{g_{m1}}{2C_L}
\]

Need a CMFB circuit to establish $V_{b1}$
Consider an output voltage for any linear circuit with two inputs.

By superposition

\[ V_{\text{OUT}} = A_1 V_1 + A_2 V_2 \]

where \( A_1 \) and \( A_2 \) are the gains (transfer functions) from inputs 1 and 2 to the output respectively.

Define the common-mode and difference-mode inputs by

\[ V_c = \frac{V_1 + V_2}{2} \quad V_d = V_1 - V_2 \]

These two equations can be solved for \( V_1 \) and \( V_2 \) to obtain

\[ V_1 = V_c + \frac{V_d}{2} \quad V_2 = V_c - \frac{V_d}{2} \]
Common-Mode and Differential-Mode Analysis

Consider an output voltage for any linear circuit with two inputs

\[ V_{OUT} = A_1 V_1 + A_2 V_2 \]

Substituting into the expression for \( V_{OUT} \), we obtain

\[ V_{OUT} = A_1 \left( V_c + \frac{V_d}{2} \right) + A_2 \left( V_c - \frac{V_d}{2} \right) \]

Rearranging terms we obtain

\[ V_{OUT} = V_c (A_1 + A_2) + V_d \left( \frac{A_1 - A_2}{2} \right) \]

If we define \( A_c \) and \( A_d \) by

\[ A_c = A_1 + A_2 \quad \quad A_d = \frac{A_1 - A_2}{2} \]

Can express \( V_{OUT} \) as

\[ V_{OUT} = V_c A_c + V_d A_d \]
Consider any output voltage for any linear circuit with two inputs

\[ V_{OUT} = A_1 V_1 + A_2 V_2 \]

\[ V_{OUT} = V_c A_c + V_d A_d \]

Implication: Can solve a linear two-input circuit by applying superposition with \( V_1 \) and \( V_2 \) as inputs or by applying \( V_c \) and \( V_d \) as inputs.

Implication: In a circuit with \( A_2 = -A_1 \), \( A_c = 0 \) we obtain

\[ V_{OUT} = V_d A_d \]
Common-Mode and Differential-Mode Analysis

Depiction of single-ended inputs and common/difference mode inputs

\[ V_{\text{OUT}} = A_1 V_1 + A_2 V_2 \]

\[ V_{\text{OUT}} = V_c A_c + V_d A_d \]
Common-Mode and Differential-Mode Analysis

Extension to differential outputs and symmetric circuits

Theorem: The symmetric differential output voltage for any symmetric linear network excited at symmetric nodes can be expressed as

\[ V_{\text{OUT}} = A_d V_d \]

where \( A_d \) is the differential voltage gain and the voltage \( V_d = V_1 - V_2 \)

Theorem: The differential output for any linear network can be expressed equivalently as

\[ V_{\text{OUT}} = A_1 V_1 + A_2 V_2 \]

or as

\[ V_{\text{OUT}} = V_c A_c + V_d A_d \]

and superposition can be applied to either \( V_1 \) and \( V_2 \) to obtain \( A_1 \) and \( A_2 \) or to \( V_c \) and \( V_d \) to obtain \( A_c \) and \( A_d \)
Common-Mode and Differential-Mode Analysis

Proof for Symmetric Circuit with Symmetric Differential Output:

By superposition, the single-ended outputs can be expressed as

\[ V_{OUT+} = T_{OPA}v_1 + T_{OPB}v_2 \]
\[ V_{OUT-} = T_{ONA}v_1 + T_{ONB}v_2 \]

where \( T_{OPA}, T_{OPB}, T_{ONA} \) and \( T_{ONB} \) are the transfer functions from the A and B inputs to the single-ended + and - outputs.

Taking the difference of these two equations we obtain

\[ V_{OUT} = V_{OUT+} - V_{OUT-} = (T_{OPA} - T_{ONA})v_1 + (T_{OPB} - T_{ONB})v_2 \]

By symmetry, we have

\[ T_{OPA} = T_{ONB} \text{ and } T_{ONA} = T_{OPB} \]

Thus can be express \( V_{OUT} \) as

\[ V_{OUT} = (T_{OPA} - T_{ONA})(v_1 - v_2) \]

or as

\[ V_{OUT} = A_d v_d \]

where \( A_d = T_{OPA} - T_{ONA} \) and where \( v_d = v_1 - v_2 \)
Common-Mode and Differential-Mode Analysis

Consider any output voltage for any linear circuit with two inputs.

\[ V_{OUT} = A_1 V_1 + A_2 V_2 \]

\[ V_{OUT} = V_c A_c + V_d A_d \]

Single-Ended Superposition

Difference-Mode/Common-Mode Superposition
Consider an output voltage for any linear circuit with two inputs.

\[ v_{OUT} = v_c A_c + v_d A_d \]

Difference-Mode/Common-Mode Superposition is almost exclusively used for characterizing Amplifiers that are designed to have a large differential gain and a small common-mode gain.
Performance with Common-Mode Input

Single-Ended Outputs
Tail-Current Bias

Differential Output
Tail Current Bias
Performance with Common-Mode Input

Consider tail-current bias amplifier

No current flows across axis of symmetry in a symmetric circuit

Common-Mode Half-Circuit
Performance with Common-Mode Input

Consider tail-current bias amplifier

\[ v_{\text{OUTC}}(sC+G_1+G_2)+G_{M1}v_1 = G_1v_X \]

\[ v_C = v_1 + v_X \]

\[ v_xG_1 - G_{M1}v_1 = v_{\text{OUTC}} \]

Solving, we obtain

\[ v_{\text{OUTC}} = 0 \quad \text{thus } A_C = 0 \]
Performance with Common-Mode Input

Consider tail-voltage bias amplifier

No current flows across axis of symmetry in a symmetric circuit

Common-Mode Half-Circuit
Performance with Common-Mode Input

Consider tail-voltage bias amplifier

Common-Mode Half-Circuit

\[ V_{OUTC} = A_C \frac{G_{M1}}{sC + G_1 + G_2} \]

This circuit has a rather large common-mode gain and will not reject common-mode signals.
Recall

Applications of Quarter-Circuit Concept to Op Amp Design

consider initially the basic single-ended amplifier

![Quarter Circuit Diagram]
Recall

Single-stage single-input low-gain op amp

Basic Structure

Quarter Circuit

Counterpart Circuit

Practical Implementation
Recall

Small signal model of half-circuit

\[ G = G_1 + G_2 \]
\[ G_M = G_{M1} \]
Recall

**Single-stage low-gain differential op amp**

Quarter Circuit

Single-Ended Output : Differential Input Gain

\[
A(s) = \frac{-g_{m1}}{2} \frac{2}{sC_L + g_{o1} + g_{o3}}
\]

\[
A_o = \frac{2}{g_{o1} + g_{o3}}
\]

\[
GB = \frac{g_{m1}}{2C_L}
\]

Need a CMFB circuit to establish \(V_{b1}\)
Single-stage low-gain differential op amp

\[ A(s) = \frac{-g_{m1}^2}{sC_L + g_{o1} + g_{o3}} \]

\[ A_o = \frac{g_{m1}}{2g_{o1} + g_{o3}} \]

\[ GB = \frac{g_{m1}}{2C_L} \]

What are the number of degrees of freedom?
(assume \(V_{DD}, C_L\) fixed)

Natural Parameters:
\[ \left\{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, V_{B1}, V_{B3} \right\} \]

Constraints: \(I_{D5} \approx 2I_{D3}\)

Net Degrees of Freedom: 4

Need a CMFB circuit to establish \(V_{b1}\)

Practical Parameters:
\[ \left\{ V_{EB1}, V_{EB3}, V_{EB5}, P \right\} \]
Single-stage low-gain differential op amp

Quarter Circuit

Single-Ended Output : Differential Input Gain

\[ A(s) = \frac{g_{m1}}{2} \frac{2}{sC_L + g_{o1} + g_{o3}} \]

\[ A_o = \frac{g_{m1}}{2} \frac{2}{g_{o1} + g_{o3}} \]

\[ GB = \frac{g_{m1}}{2C_L} \]

\[ A_o = \left[ \frac{1}{\lambda_1 + \lambda_3} \right] \left( \frac{1}{V_{EB1}} \right) \]

\[ GB = \left( \frac{P}{V_{DD} C_L} \right) \cdot \left[ \frac{1}{2V_{EB1}} \right] \]

Need a CMFB circuit to establish \( V_{b1} \)
Single-stage low-gain differential op amp

Quarter Circuit

\[ V_{OD} = V_0^+ - V_0^- \]

Differential Output : Differential Input Gain

\[ A(s) = \frac{g_{m1}}{sC_L + g_{o1} + g_{o3}} \]

\[ A_0 = \frac{g_{m1}}{g_{o1} + g_{o3}} \]

\[ GB = \frac{g_{m1}}{C_L} \]

\[ A_0 = \left[ \frac{1}{\lambda_1 + \lambda_3} \right] \left( \frac{2}{V_{EB1}} \right) \]

\[ GB = \left( \frac{P}{V_{DD}C_L} \right) \cdot \left[ \frac{1}{V_{EB1}} \right] \]

Need a CMFB circuit to establish \( V_{B1} \) or \( V_{B2} \)
### Operational Amplifier Small Signal Characteristics in Terms of Quarter Circuit Performance

**Assumptions:** Bias current in quarter circuits same as in Op Amps and $C_L$ is load capacitance on each side of op amp

<table>
<thead>
<tr>
<th></th>
<th>Single-ended Output</th>
<th>Differential Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A(s)$</td>
<td>$A(s) = \frac{-g_{MN}}{2} \frac{2}{sC_L + g_{ON} + g_{OP}}$</td>
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<tr>
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<td>$GB$</td>
<td>$GB = \frac{1}{2} \frac{g_{MN}}{C_L}$</td>
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</table>

Expressions valid for both tail-current and tail-voltage op amp
Expressions valid for both tail-current and tail-voltage op amp

So which one should be used?

- Common-mode input range large for tail current bias
- Improved rejection of common-mode signals for tail current bias
- Extra design degree of freedom for tail current bias
- Improved output signal swing for tail voltage bias (will show later)
Slew Rate

Definition: The slew rate of an amplifier is the maximum rate of change that can occur at an output node.

SR is a nonlinear large-signal characteristic. Input is over-driven hard (some devices in an amplifier usually leave normal operating region).

Magnitude of SR^+ and SR^- usually same and called SR (else SR^+ and SR^- must be given).
Slew Rate

With step input on $V_{\text{IN}}^+$, all tail current ($I_T$) will go to $M_1$ thus turning off $M_2$ thus current through $M_4$ which is $1/2$ of $I_T$ will go to load capacitor $C_L$

The I-V characteristics of any capacitor is

$$I = C \frac{dV}{dt}$$

Substituting $I = I_T/2$, $V = V_{\text{OUT}}^+$, and $C = C_L$ obtain a voltage ramp at the output thus

$$SR^+ = \frac{dV_{\text{OUT}}^+}{dt} = \frac{I_T}{2C_L} = \frac{P}{V_{DD}2C_L}$$
Slew Rate

It can be similarly shown that putting a negative step on the input steer all current to M₂ thus the current to the capacitor C_L will be I_T minus the current from M₂ which is still I_T/2. This will cause a negative ramp voltage on V_OUT⁺ of value

\[ SR^- = \frac{dV_{OUT}^+}{dt} = -\frac{I_T}{2C_L} = -\frac{P}{V_{DD}2C_L} \]

Since the magnitude of SR⁺ and SR⁻ are the same, obtain a single SR for the amplifier of value

\[ SR = \frac{P}{V_{DD}2C_L} \]
Single-stage low-gain differential op amp

Consider single-ended output performance:

Will term this the **reference op amp**
Will make performance comparisons of other op amps relative to this

\[
A(s) = \frac{2}{sC_L + g_{o1} + g_{o3}}
\]

mixed parameters

\[
A_{VO} = \frac{1}{2} \frac{g_{m1}}{g_{o1} + g_{o3}}
\]

\[
g_{m1} \quad 2C_L
\]

\[
GB = \frac{g_{m1}}{2C_L}
\]

\[
SR = \frac{I_T}{2C_L}
\]

practical parameters

\[
A_{v0} = \left[\frac{1}{\lambda_1 + \lambda_3}\right] \left[\frac{1}{V_{EB1}}\right]
\]

\[
GB = \left(\frac{P}{2V_{DD}C_L}\right) \cdot \left[\frac{1}{V_{EB1}}\right]
\]

\[
SR = \frac{P}{2V_{DD}C_L}
\]

Need a CMFB circuit to establish \(V_{b1}\)
Reference Op Amp
single-ended output

\[
A(s) = \frac{g_{m1}}{2} \frac{2}{sC_L + g_{o1} + g_{o3}}
\]

\[
A_{v0} = \frac{1}{2} \frac{g_{m1}}{g_{o1} + g_{o3}}
\]

\[
GB = \frac{g_{m1}}{2C_L}
\]

\[
SR = \frac{I_T}{2C_L}
\]

\[
A_{v0} = \left[ \frac{1}{\lambda_1 + \lambda_3} \right] \left( \frac{1}{V_{EB1}} \right)
\]

\[
GB = \left( \frac{P}{2V_{DD}C_L} \right) \cdot \left[ \frac{1}{V_{EB1}} \right]
\]

\[
SR = \frac{P}{2V_{DD}C_L}
\]

Need a CMFB circuit to establish \( V_{b1} \)
## Amplifier Structure Summary

### Small Signal Parameter Domain

<table>
<thead>
<tr>
<th>Common Source</th>
<th>$A_{vo} = \frac{g_m}{g_o}$</th>
<th>$GB = \frac{g_m}{C_L}$</th>
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### Practical Parameter Domain

<table>
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<tr>
<th>Common Source</th>
<th>$A_{vo} = \left(\frac{2}{\lambda}\right)\left(\frac{1}{V_{EB}}\right)$</th>
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### Small Signal Parameter Domain

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<th>$A_{vo} = \frac{1}{2} \frac{g_{m1}}{g_{o1} + g_{o3}}$</th>
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### Practical Parameter Domain

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</table>
What basic type of amplifier is this op amp?

\[
A(s) = \frac{g_{m1}}{2} \frac{2}{sC_L + g_{o1} + g_{o3}}
\]
What basic type of amplifier is this op amp?

Does it really matter?

\[ A(s) = \frac{g_{m1}}{2} \frac{2}{sC_L + g_{O1} + g_{O3}} \]
Single-stage low-gain differential op amp

Need a CMFB circuit to establish \( V_{B1} \) or \( V_{B2} \)

CMFB amplifies difference between \( V_{B1} \) and average of two signal inputs

Can apply to either \( V_{B1} \) or \( V_{B2} \) but not both
End of Lecture 5
Current Mirrors

• Current mirrors are really just a current amplifier
• Simple current mirror was used to eliminate CMFB and double gain in basic op amp
• Many different current mirrors exist with varying levels of performance
Basic Current Mirror

\[ I_{IN} = \frac{\mu C_{OX} W_1}{2L_1} (V_{GS1} - V_T)^2 \]

\[ I_{OUT} = \frac{\mu C_{OX} W_2}{2L_2} (V_{GS2} - V_T)^2 \]

\[ \frac{I_{OUT}}{I_{IN}} = \frac{W_2}{W_1} \frac{L_1}{L_2} \]

At the output port, small signal equivalent is a one-port

\[ g_{out} = g_{02} \]
Basic Current Mirror

\[ I_{\text{IN}} = \frac{\mu C_{\text{OX}} W_1}{2L_1} (V_{\text{GS1}} - V_T)^2 \]

\[ I_{\text{OUT}} = \frac{\mu C_{\text{OX}} W_2}{2L_2} (V_{\text{GS2}} - V_T)^2 \]

\[ \frac{I_{\text{OUT}}}{I_{\text{IN}}} = \frac{W_2 L_1}{W_1 L_2} \]

At the output port, small signal equivalent is a one-port

\[ g_{\text{out}} = g_{02} \]
Current Mirrors

• More advanced current mirrors exist

• Most offer either improved output impedance or improved signal swing

• Several of these are discussed in the text
USPTO search on Jan 25, 2009
433 patents with “current and mirror” in title since 1976

Searching US Patent Collection...

Results of Search in US Patent Collection db for:
TTL/(current AND mirror): 433 patents.
Hits 1 through 50 out of 433

Next 50 Hits

<table>
<thead>
<tr>
<th>PAT. NO.</th>
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<tbody>
<tr>
<td>1 7,477,095</td>
<td>Current mirror architectures</td>
</tr>
<tr>
<td>2 7,468,625</td>
<td>Semiconductor device including current mirror circuit</td>
</tr>
<tr>
<td>3 7,466,202</td>
<td>High-speed CMOS current mirror</td>
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<tr>
<td>4 7,463,082</td>
<td>Light emitting device and current mirror thereof</td>
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<tr>
<td>5 7,463,014</td>
<td>High impedance current mirror with feedback</td>
</tr>
<tr>
<td>6 7,463,013</td>
<td>Regulated current mirror</td>
</tr>
<tr>
<td>7 7,449,955</td>
<td>Chain-chopping current mirror and method for stabilizing output currents</td>
</tr>
<tr>
<td>8 7,439,796</td>
<td>Current mirror with circuitry that allows for over voltage stress testing</td>
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USPTO search on Jan 25, 2009
36 patents with “current and mirror” in title in 2007 and 2008

Results of Search in US Patent Collection db for:
(TTL/(current AND mirror) AND ISD/20070101->20090101): 36 patents.
Hits 1 through 36 out of 36

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<tr>
<td>9</td>
<td>7,432,696 Apparatus and method for low input voltage current mirror circuit</td>
</tr>
<tr>
<td>10</td>
<td>7,429,854 CMOS current mirror circuit and reference current/voltage circuit</td>
</tr>
<tr>
<td>11</td>
<td>7,425,870 Current mirror circuit</td>
</tr>
<tr>
<td>12</td>
<td>7,423,476 Current mirror circuit having drain-source voltage clamp</td>
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USPTO search on Jan 25, 2009

433 patents with “current and mirror” in title since 1976

36 patents with “current and mirror” in title in 2007 and 2008

Averaged 12.4 patents/year from 1976 to 2006
Averaged 18 patents in 2007 and 2008
Single-stage low-gain differential op amp

- Can eliminate CMFB circuit if only single-ended output is needed by connecting counterpart circuits as a current mirror
- This will double the voltage gain and the GB as well
- Still uses counterpart circuits but terminated in different ways
- Although not symmetric, previous analysis results with specified modifications still nearly apply
Single-stage low-gain differential op amp

Current-Mirror Connected Counterpart Circuit

No CMFB Circuit Needed

\[
A(s) = \frac{g_{m1}}{sC_L + g_{o1} + g_{o3}}
\]

\[
A_o = \frac{g_{m1}}{g_{o1} + g_{o3}}
\]

\[
GB = \frac{g_{m1}}{C_L} \quad SR = \frac{I_T}{C_L}
\]

In terms of practical design space parameters

\[
A_o = \left[ \frac{1}{\lambda_1 + \lambda_3} \right] \left( \frac{2}{V_{E1}} \right)
\]

\[
GB = \left( \frac{P}{V_{DD}C_L} \right) \cdot \left[ \frac{1}{V_{E1}} \right]
\]

\[
SR = \frac{P}{V_{DD}C_L}
\]
Signal Swing

To keep $M_1$ out of Triode Region

$\mathcal{L}_1: \ V_{OUT} > V_{iN} - V_{Tn}$

To keep $M_1$ out of Cutoff

$\mathcal{L}_2: \ V_{iN} > V_{Tn}$

To keep $M_2$ out of Triode Region

$\mathcal{L}_3: \ |V_{OUT} - V_{DD}| > |V_{XX} - V_{DD} - V_{Tp}|$

$V_{XX} - V_{Tp} > V_{OUT}$
Signal Swing

\( L_1: \quad V_{OUT} > V_{IN} - V_{TN} \)

\( L_2: \quad V_{IN} > V_{TN} \)

\( L_3: \quad V_{XX} - V_{TP} > V_{OUT} \)
Signal Swing

\[ \mathcal{L}_1: \ V_{\text{OUT}} > V_{\text{iN}} - V_{Tn} \]
\[ \mathcal{L}_2: \ V_{\text{iN}} > V_{Tn} \]
\[ \mathcal{L}_3: \ V_{XX} - V_{Tp} > V_{\text{OUT}} \]
How do the transfer characteristics relate to the signal swing?

Observe signal swing boundaries are same as operating region changes for transfer characteristics.
Signal Swing

How do the transfer characteristics relate to the signal swing?

For this circuit, high gain and large output signal swing for small $V_{EB1}$.
Signal Swing of Single-Stage Op Amp

For high-gain amplifiers, $V_d$ is inherently very small so are only concerned about output signal swing vs $V_{iC}$.

Generally large swings come at expense of other desirable characteristics.
Signal Swing of Single-Stage Op Amp

What type of signal swing is needed?

Wide $V_{iC}$ and $V_{OUT}$ range

Narrow $V_{iC}$ and wide $V_{OUT}$ range

Narrow $V_{OUT}$ and wide $V_{iC}$ range

Narrow $V_{iC}$ and $V_{OUT}$ range
Signal Swing of Single-Stage Op Amp

What type of signal swing is needed?

Wide $V_{iC}$ and $V_{OUT}$ range

Expected for catalog parts and overall I/O in many applications

Narrow $V_{iC}$ and wide $V_{OUT}$ range

Acceptable when $V_{iC}$ is fixed

Narrow $V_{OUT}$ and wide $V_{iC}$ range

Acceptable when followed by high-gain stage

Narrow $V_{iC}$ and $V_{OUT}$ range

Acceptable when $V_{iC}$ fixed and followed by high-gain stage
Signal Swing of Single-Stage Op Amp

Constraining Equations:

To keep $M_2$ in Saturation:

$$\mathcal{L}_1: \quad V_{OUT} > V_{ic} - V_{T2}$$

To keep $M_4$ in Saturation:

$$\mathcal{L}_2: \quad V_{OUT} < V_{DD} - |V_{EB4}|$$

To keep $M_1$ in Saturation:

$$\mathcal{L}_3: \quad V_{ic} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}|$$

To keep $M_5$ in Saturation:

$$\mathcal{L}_4: \quad V_{ic} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS}$$
Signal Swing of Single-Stage Op Amp

To keep \( M_2 \) in Saturation:
\[
\mathcal{L}_1: \quad V_{\text{OUT}} > V_{\text{ic}} - V_{T2}
\]

To keep \( M_4 \) in Saturation:
\[
\mathcal{L}_2: \quad V_{\text{OUT}} < V_{\text{DD}} - |V_{EB4}|
\]

To keep \( M_1 \) in Saturation:
\[
\mathcal{L}_3: \quad V_{\text{ic}} < V_{\text{DD}} + V_{T1} - |V_{T3}| - |V_{EB3}|
\]

To keep \( M_5 \) in Saturation:
\[
\mathcal{L}_4: \quad V_{\text{ic}} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS}
\]
Signal Swing of Single-Stage Op Amp

Constraining Equations:

\[ \mathcal{L}_1: \quad V_{\text{OUT}} > V_{\text{ic}} - V_{T2} \]

\[ \mathcal{L}_2: \quad V_{\text{OUT}} < V_{\text{DD}} - |V_{EB4}| \]

\[ \mathcal{L}_3: \quad V_{\text{ic}} < V_{\text{DD}} + V_{T1} - |V_{T3}| - |V_{EB3}| \]

\[ \mathcal{L}_4: \quad V_{\text{ic}} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS} \]
Signal Swing of Single-Stage Op Amp

\[ V_{OUT} \]

\[ V_{DD} \]

\[ V_{SS} \]

\[ |V_{EB3}| + |V_{T3}|-V_{T1} \]

\[ V_{T1}+V_{EB1}+V_{EB5} \]
Signal Swing of Single-Stage Op Amp

Signal swings are Important Performance Parameters!!

Constraining Equations:

\[ V_{\text{OUT}} > V_{\text{ic}} - V_{T2} \]
\[ V_{\text{OUT}} < V_{\text{DD}} - |V_{\text{EB4}}| \]
\[ V_{\text{ic}} < V_{\text{DD}} + V_{T1} - |V_{T3}| - |V_{\text{EB3}}| \]
\[ V_{ic} > V_{T1} + V_{\text{EB1}} + V_{\text{EB5}} + V_{\text{SS}} \]
Design space for single-stage op amp

Performance Parameters in Practical Parameter Domain \{ V_{EB1}, V_{EB2}, V_{EB5}, P \}:

\[
A_0 = \left[ \frac{1}{\lambda_1 + \lambda_3} \right] \left( \frac{2}{V_{EB1}} \right)
\]

\[
GB = \left( \frac{P}{V_{DD} C_L} \right) \left[ \frac{2}{V_{EB1}} \right]
\]

\[
SR = \frac{P}{(V_{DD} - V_{SS}) C_L}
\]

- \( V_{OUT} < V_{DD} - |V_{EB3}| \)
- \( V_{OUT} > V_{ic} - V_{T2} \)
- \( V_{ic} < V_{DD} + V_{T1} - |V_{T3}| - |V_{EB3}| \)
- \( V_{ic} > V_{T1} + V_{EB1} + V_{EB5} + V_{SS} \)

Simple Expressions in Practical Parameter Domain
**Design space for single-stage op amp**

**Performance Parameters in Natural Parameter Domain** \{ \frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, I_T \}:

\[
A_{V0} = \frac{\sqrt{4\mu_n C_{OX} \lambda_1 \lambda_3}}{\lambda_1 + \lambda_3} \left( \frac{W_1}{\sqrt{L_1 I_T}} \right) \\
SR = \frac{I_T}{C_L} \\
GB = \left[ \frac{\sqrt{\mu_n C_{OX}}}{C_L} \right] \sqrt{\frac{W_1}{L_1 I_T}} \\
\]

**Complicated Expressions in Practical Parameter Domain**

\[
V_{iC} < V_{DD} + V_{T1} - |V_{T3}| - \frac{\sqrt{I_T}}{\sqrt{\mu_p C_{OX}} \sqrt{W_3}} + \frac{\sqrt{I_T}}{\sqrt{\mu_n C_{OX}} \sqrt{\frac{W_5}{L_5}}} + V_{SS} \\
V_{ic} > V_{T1} + \frac{\sqrt{I_T}}{\sqrt{\mu_n C_{OX}} \sqrt{\frac{W_1}{L_1}}} + \frac{\sqrt{I_T}}{\sqrt{\mu_n C_{OX}} \sqrt{\frac{W_5}{L_5}}} + V_{SS} \\
V_{OUT} < V_{DD} - \frac{\sqrt{I_T}}{\sqrt{\mu_p C_{OX}} \sqrt{\frac{W}{L}}} \\
V_{OUT} > V_{ic} - V_{T2} \\
\]
Measurement and Simulation of Op Amps

• Measurement of $A_v$ is challenging
  – Because it is so large
  – Even harder as $A_{v0}$ becomes larger
  – Offset voltage causes a problem
  – Embed in Feedback Network to Stabilize Operating Point
    • Stability must be managed
    • Use time varying input to distinguish signal information from offset
    • Must be well below first pole frequency
  – Measurement challenges often parallel simulation challenges

• Measurement of GB is easy
• Measurement of $R_0$ is challenging
Single-stage op amps

Question – is the gain achievable with the single-stage op amps considered so far adequate?

\[ A_{v0} = \left[ \frac{1}{\lambda_1 + \lambda_3} \right] \left( \frac{1}{V_{EB1}} \right) \]

If \( \lambda_1 = \lambda_3 = 0.01 \text{V}^{-1} \) and \( V_{EB1} = 0.15 \text{V} \), then

\[ A_{v0} \approx \frac{1}{(0.01 + 0.01)} \frac{1}{0.15} = 333 \]

or, in db, \( A_{v0db} = 20 \log_{10} 333 = 50 \text{db} \)

This is inadequate for many applications!

What can be done about it?
Basic Op Amp Design

- Fundamental Amplifier Design Issues
- Single-Stage Low Gain Op Amps
- Single-Stage High Gain Op Amps
- Other Basic Gain Enhancement Approaches
- Two-Stage Op Amp
Determination of op amp characteristics from quarter circuit characteristics

\[ A_V = \frac{V_O^+}{V_d} = -\frac{G_{M1}}{2sC_L + G_1 + G_2} \]

Small signal differential half-circuit

\[ A_{VO} = \frac{-G_{M1}}{2(G_1 + G_2)} \]

\[ BW = \frac{G_1 + G_2}{C_L} \]

\[ GB = \frac{G_{M1}}{2C_L} \]
Single-Stage High Gain Op Amps

How can the gain of the op amp be increased?

Recall from Quarter-Circuit Concept

\[ A_{VO} = \frac{1}{2} \frac{-G_{M1}}{G_1 + G_2} \]

A possible strategy:
- Increase \( G_{M1} \) or Decrease \( G_1 \) (and \( G_2 \))
- in Quarter Circuit or Both
Single-Stage High-Gain Op Amps

- If the output conductance can be decreased without changing the transconductance, the gain can be enhanced

- Will concentrate on quarter-circuits and extend to op amps