EE 435

Lecture 8:

High-Gain Single-Stage Op Amps
Laboratory Support

Problems observed in laboratory yesterday

• Could not see gain (signals were too small)
  
  Did not know how big of signals to expect
  Amplifier offset made it difficult to see output

• Gain did not agree with expected results
  
  Not operating at right Q-point
  Amplifier was defective

• Buffer amplifier did not have right gain
  
  Voltage on protoboard pin did not agree with voltage on op amp pin

• Sparks fly when connected scope to circuit
  
  Red and black banana jack barrels on terminator were switched
Laboratory Support

Problems observed in laboratory yesterday

• Signal generator was defective because monstrous noise on output
  Scope was not appropriately triggered

• Did not see output waveform from signal generator
  Horizontal time base setting was orders of magnitude off
  Vertical amplifier setting was orders of magnitude off
  **Auto-find function on scope is not your friend !!!!!**

• Signals on scope were too noisy
  Bandwidth limit on scope useful for eliminating high frequency noise from measurement environment
Laboratory Support

Problems observed in laboratory yesterday

• Ground and common were somewhat randomly interconnected

Earth ground corresponds to the third prong on a standard 120 V connector and is connected to a large conducting rod that is driven deeply into the surface of the earth somewhere in our around the building. The chasis (if metal) on test equipment is usually connected to the third prong on the power supply cable and the metal on the benches is usually connected independently to earth ground.

The ground (black) conductor on most test equipment and the outside conductor on BNC connectors is usually connected to the third prong on the power supply cable and thus to earth ground.

Circuit ground is whatever you decide to call it but designers usually connect it to earth ground.

Common on dc power supplies is usually floating at low frequencies relative to earth ground as are the positive and negative terminals of the dc power supplies.

Everything connected to earth ground is connected together and no ac or dc signal source can be connected “between” two earth ground connections !!
Laboratory Support

Offset Voltage

- Systematic Offset Voltage
- Random Offset Voltage

\[ V_{ICQ} \]

\[ V_{OUT} \]
Laboratory Support

Offset Voltage

- Systematic Offset Voltage
- Random Offset Voltage

$$V_{OUT}$$

$$V_{ICQ}$$

Definition: The output offset voltage is the difference between the desired output and the actual output when $$V_{id}=0$$ and $$V_{ic}$$ is the quiescent common-mode input voltage.

$$V_{OUTOFF} = V_{OUT} - V_{OUTDES}$$

Note: $$V_{OUTOFF}$$ is dependent upon $$V_{ICQ}$$ although this dependence is usually quite weak and often not specified
Laboratory Support

Definition: The input-referred offset voltage is the differential dc input voltage that must be applied to obtain the desired output when $V_{ic}$ is the quiescent common-mode input voltage.

Note: $V_{OFF}$ is usually related to the output offset voltage by the expression

$$V_{OFF} = \frac{V_{OUTOFF}}{A_C}$$

Note: $V_{OFF}$ is dependent upon $V_{ICQ}$ although this dependence is usually quite weak and often not specified.
When differential input op amps are biased with symmetric supply voltages, it is generally assumed that the desired quiescent input voltage is 0V and the desired quiescent output voltage is 0V so $V_{\text{OFF}}$ is the differential input voltage needed to make $V_{\text{OUT}}=0V$.

The input offset voltage is comprised of two parts, a systematic component and a random component

$$V_{\text{OFF}} = V_{\text{OFFSYS}} + V_{\text{OSR}}$$
Laboratory Support

\[ V_{OFF} = V_{OFFSYS} + V_{OSR} \]

After fabrication there is no distinction made between \( V_{OFFSYS} \) and \( V_{OSR} \) and simply \( V_{OFF} \) is of concern.

\( V_{OSR} \) is determined entirely by random variations in component values from their ideal value and will only be seen in a simulation if deviations are intentionally introduced (Monte Carlo Analysis if often used for predicting \( V_{OSR} \)).

It is expected that \( V_{OFFSYS} \) should be small (much smaller than \( V_{OSR} \)) and it is the designer’s responsibility to make this small.
It is not necessary to make $V_{\text{OFFSYS}} = 0$ although this can and is often done by making a minor tweak of matching critical parameters after the design of the op amp is almost complete.

$V_{\text{OFF}}$ can also be set to 0 by using a degree of freedom of the amplifier design variables but this is generally an unwise use of degrees of freedom (although some textbooks including Martin and Johns in Sec 5.1 do this!)
By symmetry, to force $V_{\text{OUT}} = 0$, it is necessary to have $V_{D3}=0$

- Making $V_{D3}=0$ sets $|V_{EB3}| = V_{DD} + V_{Tp}$ and results in the use of one degree of freedom!
- Making $V_{EB3}$ so large will severely limit the voltage swing at $V_{\text{OUT}}$
- This shows why it is not wise to use a degree of freedom to make the systematic offset voltage 0
Laboratory Support

Can sweep a voltage in simulator at gate of $M_1$ to make $V_{OUT}=0$

This is the systematic offset voltage

Can simply add the systematic offset voltage to input throughout rest of the design phase and then remove after design is complete or tweak at end of design to eliminate systematic offset.
Laboratory Support

Usually $V_{OFF}$ will change if changes in any design variables are made so re-simulation will be needed to get the correct value of $V_{OFF}$.

If $V_{OFF}$ is not included, ac simulation of open-loop amplifier will usually not give desired results because small-signal models will be developed in simulator at incorrect operating point (often even in incorrect region of operation).

Alternative is to do ac simulations by embedding op amp into a FB configuration that will inherently compensate for offset voltage but issue of compensation must be addressed for amplifiers with two or more poles.
Review from last lecture:

Basic Op Amp Design

• Fundamental Amplifier Design Issues
• Single-Stage Low Gain Op Amps
• Single-Stage High Gain Op Amps
• Other Basic Gain Enhancement Approaches
• Two-Stage Op Amp
Determination of op amp characteristics from quarter circuit characteristics

Small signal differential half-circuit

\[
A_V = \frac{V_O^+}{V_d} = \frac{-G_{M1}}{2sC_L + G_1 + G_2}
\]

\[
A_{VO} = \frac{-G_{M1}}{2(G_1 + G_2)}
\]

\[
BW = \frac{G_1 + G_2}{C_L}
\]

\[
GB = \frac{G_{M1}}{2C_L}
\]
Single-Stage High Gain Op Amps

How can the gain of the op amp be increased?

Recall from Quarter-Circuit Concept

\[ A_{VO} = \frac{1}{2} \cdot \frac{-G_{M1}}{G_1 + G_2} \]

A possible strategy:

- Increase \( G_{M1} \) or Decrease \( G_1 \) (and \( G_2 \))
- in Quarter Circuit or Both
Review from last lecture:

Determination of 2-port parameters

Method 2: Load Termination Approach

express the gain $A(s)$ in form

$$A(s) = \frac{a_0}{sC_L + b_0}$$

observe

$$V_2(g_{o2} + sC_L) + g_{M2}V_{TST} = 0$$

$$A(s) = \frac{V_2(s)}{V_{TST}(s)} = \frac{g_{M2}}{sC_L + g_{o2}}$$

(must express in integer-monic form)
Analysis of Cascode Amplifier

**Review from last lecture:**

\[
\begin{align*}
V_{\text{OUT}}(g_{o2} + sC_L) + g_{m2}V_2 &= V_x g_{o2} \\
V_x(g_{o1} + g_{o2}) + g_{m1}V_1 - g_{m2}V_2 &= V_{\text{OUT}} g_{o2} \\
V_2 &= -V_x \\
V_1 &= V_{\text{IN}}
\end{align*}
\]

\[
\begin{align*}
V_{\text{OUT}}(g_{o2} + sC_L) - g_{m2}V_x &= V_x g_{o2} \\
V_x(g_{o1} + g_{o2}) + g_{m1}V_{\text{IN}} + g_{m2}V_x &= V_{\text{OUT}} g_{o2}
\end{align*}
\]

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{-g_{m1}(g_{o2} + g_{m2})}{sC_L(g_{o1} + g_{o2} + g_{m2}) + g_{o1}g_{o2}} \approx \frac{-g_{m1}g_{m2}}{sC_L g_{m2} + g_{o1}g_{o2}}
\]

for \( A \) large:

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} \approx \frac{-g_{m1}}{sC_L + g_{o1}\left(\frac{g_{o2}}{g_{m2}}\right)}
\]

\( g_{\text{MEQ}} \) and \( g_{\text{OEQ}} \)
High output impedance quarter-circuits

Cascode Amplifier (small-signal equiv)

Quarter Circuit

Review from last lecture:
Review from last lecture:

Telescopic Cascode Op Amp

Needs CMFB Circuit for $V_{B1}$ or $V_{B5}$
Either single-ended or differential outputs
Can connect counterpart as current mirror to eliminate CMFB
Review from last lecture:

Telescopic Cascode Op Amp

Single-ended operation

\[ g_{OQC} = \quad \]  
\[ g_{OCC} = \quad \]  
\[ g_{mQC} = \quad \]
Review from last lecture:

Telescopic Cascode Op Amp

Single-ended operation

\[ A_0 = \frac{-g_{m1}}{2} + \frac{g_{o1}}{g_{m3}} + \frac{g_{o5}}{g_{m7}} \]

\[ GB = \frac{g_{m1}}{2C_L} \]
Telescopic Cascode Op Amp

Review from last lecture:

Standard p-channel Cascode Mirror

- Current-Mirror p-channel Bias to Eliminate CMFB
- Only single-ended output available

Wide-Swing p-channel Cascode Mirror
Review from last lecture:

Telescopic Cascode Op Amp

n-channel inputs

p-channel inputs
Are there other high output impedance circuits that can be used as quarter circuits?
Are there other high output impedance circuits that can be used as quarter circuits?

I recall the regulated cascode circuits have this property.
High output impedance quarter-circuits

Regulated Cascode Amplifier
or “Gain Boosted Cascode”

(A is usually a simple amplifier, often the reference op amp with + terminal connected to the desired quiescent voltage)
Background
Analysis of Regulated Cascode Amplifier

\[
\begin{align*}
V_{\text{OUT}} (g_{o2} + sC_L) + g_{m2} V_2 &= V_X g_{o2} \\
V_X (g_{o1} + g_{o2}) + g_{m1} V_1 - g_{m2} V_2 &= V_{\text{OUT}} g_{o2} \\
V_2 &= -AV_X - V_X \\
V_1 &= V_{\text{IN}}
\end{align*}
\]

\(V_X, V_1 \) and \(V_2\) can be eliminated from these 4 equations.
Background

Analysis of Regulated Cascode Amplifier

\[
V_{\text{OUT}} (g_{o2} + sC_L) + g_{m2} V_2 = V_X g_{o2} \\
V_X (g_{o1} + g_{o2}) + g_{m1} V_1 - g_{m2} V_2 = V_{\text{OUT}} g_{o2} \\
V_2 = -AV_X - V_X \\
V_1 = V_{\text{IN}}
\]

\[
\begin{align*}
V_{\text{OUT}} (g_{o2} + sC_L) - g_{m2} V_X (1 + A) &= V_X g_{o2} \\
V_X (g_{o1} + g_{o2}) + g_{m1} V_{\text{IN}} + g_{m2} V_X (1 + A) &= V_{\text{OUT}} g_{o2}
\end{align*}
\]

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{-g_{m1} (g_{o2} + g_{m2} [1 + A])}{sC_L (g_{o1} + g_{o2} + g_{m2} [1 + A]) + g_{o1} g_{o2}} \approx \frac{-g_{m1} g_{m2} [1 + A]}{sC_L g_{m2} [1 + A] + g_{o1} g_{o2}} = \frac{-g_{m1}}{sC_L + \frac{g_{o1} g_{o2}}{g_{m2} [1 + A]}}
\]

for A large:

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} \approx \frac{-g_{m1}}{sC_L + g_{o1} \left( \frac{g_{o2}}{g_{m2}} \right) \left( \frac{1}{A} \right)}
\]
High output impedance quarter-circuits

Regulated Cascode Amplifier
or “Gain Boosted Cascode”

\[ g_{OEQ} \approx g_{O1} \left[ \frac{g_{O3}}{g_{m3} (1 + A)} \right] \]

\[ g_{mEQ} \approx g_{m1} \]

Output conductance has been decreased even more!

\[ A_v(s) \approx \frac{-g_{m1}}{sC_L + g_{O1} \left( \frac{g_{O3} [1 + A]}{g_{m3}} \right)} \]

\[ A_0 \approx \left( \frac{g_{m1}}{g_{O1}} \right) \cdot \left[ \frac{g_{m3} (1 + A)}{g_{O3}} \right] \]

\[ GB \approx \frac{g_{m1}}{C_L} \]

Same GB as for previous two circuits
Gain-Boosted Telescopic Cascode Op Amp

Needs CMFB Circuit for $V_{b1}$
Either single-ended or differential outputs
Can connect counterpart as current mirror to eliminate CMFB
Use differential op amp to facilitate biasing of cascode device
Gain-Boosted Telescopic Cascode Op Amp

Single-ended operation

\[ g_{OQC} = \]

\[ g_{OCC} = \]

\[ g_{mQC} = \]
Gain-Boosted Telescopic Cascode Op Amp

This is modestly less efficient at generating GB because now power is consumed in both the cascode devices and the boosting amplifier.
Gain-Boosted Telescopic Cascode Op Amp

\[ A_o = \frac{-g_{m1}}{g_{o1} A_1 g_{o3} + g_{o5} A_3 g_{o7}} \]

\[ GB = \frac{g_{m1}}{C_L} \]

This is modestly less efficient at generating GB because now power is consumed in both the cascode devices and the boosting amplifier.

Elimination of need for CMFB Circuit
Gain-Boosted Telescopic Cascode Op Amp

Signal Swing and Power Supply Limitations

A minimum of 5 $V_{DSAT}$ drops between $V_{DD}$ and $V_{SS}$

This establishes a lower bound on $V_{DD}-V_{SS}$ and it will be reduced by the p-p signal swing on the output
Gain-Boosted Telescopic Cascode Op Amp
(with or w/o current mirror counterpart circuits)

Advantages:

Significant increase in dc gain

Limitations:

- Signal swing ($4V_{D_{SAT}}+V_T$ between $V_{DD}$ and $V_{SS}$)
- Reduction in GB power efficiency
  - some current required to bias “A” amplifiers
- Additional pole in “A” amplifier
  - may add requirements for some compensation
- Area Overhead for 4 transistors and 4 amplifiers
  - actually minor concern since performance will usually justify these resources
End of Lecture 8