MOSIS Scalable CMOS (SCMOS) Design Rules
(Revision 8.0)

Updated: October 4, 2004

Half-lambda grid submissions

MOSIS Scalable design rules require that layout is on a 1/2 lambda grid. Any other gridding information may change without warning. We will accept and process a design regardless of its actual grid (as though it were completely design-rule legal) using the standard "recipe" for that design rule set.

The fracture process puts all its data onto a grid. As an example, the mask grid size in the case of the AMI 1.50 micron process is 0.05 micron on the critical layers (P1, P2 and Active) and 0.10 micron on the others, and all points in your layout that do not fall onto these grid points are "snapped" to the nearest grid point. Obviously, half a grid is the largest snap distance, applied to points that fall neatly in the middle.

XP Layer

MOSIS has defined an optional layer (called XP in CIF and numbered 26 in GDSII) to help users tell MOSIS which pads are to be bonded and which are not. The bonding pad layer is named "XP" in all SCMOS technologies. This optional layer lets you call out only those glass cuts that you want MOSIS to use in bonding your project. This allows you to have probe pads within 600 micrometers (~25 mils) of the project edge, which MOSIS will not attempt to bond out.

Geometry on layer XP is used solely to help generate bonding diagrams. It has absolutely no influence on chip fabrication.

MOSIS XP and Pad Layer Checks:

MOSIS discovers the bonding pads in a project as follows:

A. If there is any layout on layer XP, MOSIS assumes that each rectangle on that layer -- either a box (B) or a polygon (P) -- that is at least 70 µm x 70 µm and within 600 micrometers of the project edge represents a bonding pad position.
B. If there is no layout on layer XP, MOSIS assumes that the distinct boxes (B) (but not polygons) of reasonable size and within 600 micrometers of the project edge - not overlapping and not touching - on the overglass cut layer represent bonding pad positions.
C. MOSIS checks that all declared bonding pads (in layer XP) have a glass cut feature under them. A project without these features will be rejected, and the user will receive the message: "Bonding marks (layer XP) without passivation cuts are not allowed."
D. MOSIS verifies that there is a metal pad under each bonding pad and will reject any project that does not have metal under glass cuts with the error message: "Bonding passivation cuts found without metal pads underneath."
E. If you use the XP layer, MOSIS will not look at your glass cut layer to find your bonding pads. Therefore, be sure that the layout on this layer is correct, since the bonding diagram is generated based on these (presumed) bonding pads.

MOSIS CMP and Antenna Rules

Minimum Density Rule

Fine featured processes utilize CMP (Chemical-Mechanical Polishing) to achieve planarity. All proceses accessed by MOSIS at 0.5 micron and below are in this category. Effective CMP requires that the variations in feature density on a layer be restricted. The following fill rules apply to processes without more detailed requirements (as, IBM).

xx.1	Minimum poly layer density	15%
xx.2	Minimum metal layer density (applies separately to each metal layer with a density requirement). For TSMC processes, all metal layers must meet density. For Agilent and AMI processes, all but the top-most metal must meet density.	30%
xx.3	Minimum metal layer density for Cap_Top_Metal (TSMC only)	3%

The density of a layer in any particular region is the total area covered by the drawn features on that layer divided by the area of the region. The smallest unit of applicability of these rules is a 1 mm x 1 mm square.
If requested by the customer, MOSIS fills in the open areas on projects fabricated on the affected processes. MOSIS does not fill for IBM processes. Designs for IBM runs must meet the IBM fill requirements when submitted.

One source of dummy fill tools is CMP Technology, Inc., listed on our Third Party Services page.

The one situation that must be avoided under these minimum density rules is large non-empty regions that are devoid of one (or more) of the minimum density layers

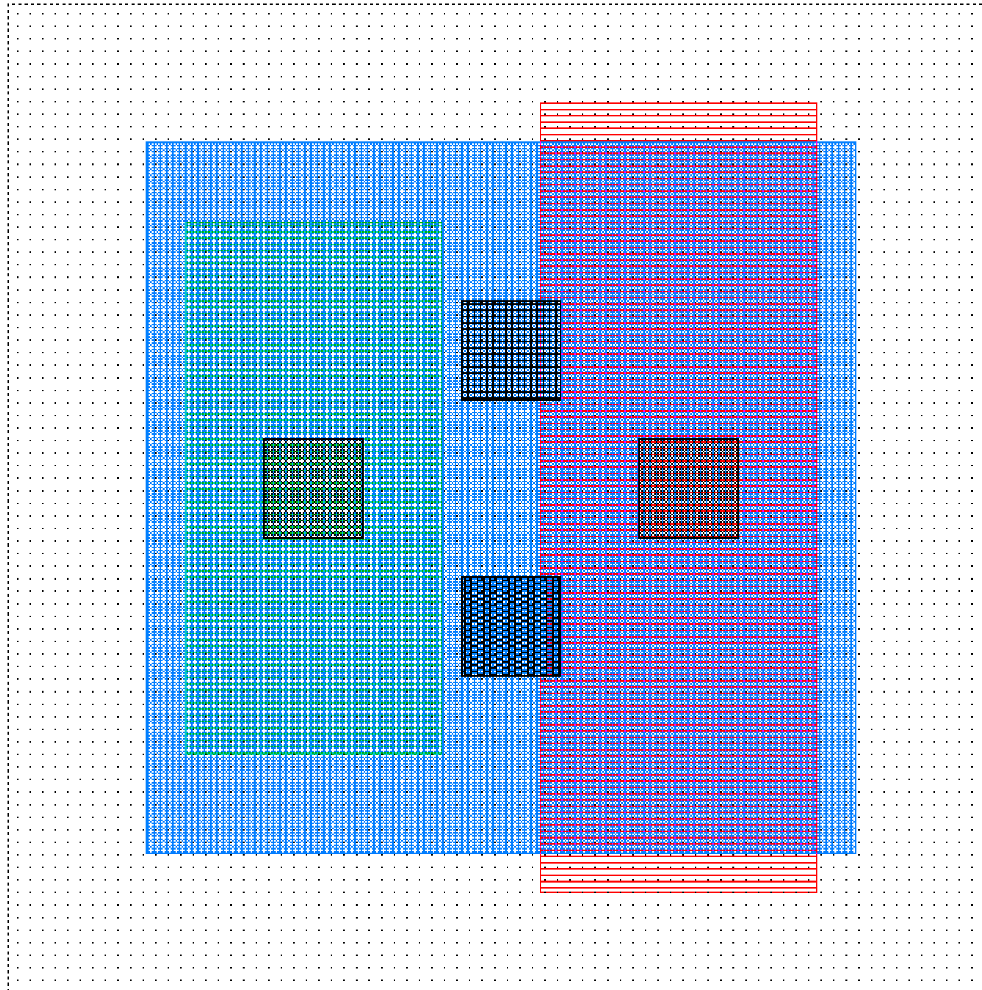
```
DS1 100/50;
(SCMOS 5 x 5 micron fill cell for levels up to metal3);
LCAA; B 65 135  75 125;
LCPG; B 70 200 170 125;
LCCC; B 25  25  75 125;
      B 25  25 170 125;
LCMF; B180 180 125 125;
LCVA; B 25  25 125  90;
LCMS; B180 180 125 125;
LCVS; B 25  25 125 160;
LCMT; B180 180 125 125;
LCX;  B250 250 125 125; (cell outline);
DF;

C 1;
E
```

The cell layout depicted is idealized. The actual layout we generate varies from process to process, based on the foundry's own fill rules. For those foundries that encourage, or at least allow, floating layout in fill cells, we generate only the poly and metal layout; the active, contact and via layers are not filled. For those foundries that require that the fill cells be electrically grounded, we generate the entire stack, so that the cell is electrically connected to the substrate. We also extend the stack upward through as many metal

layers as required (all or all but the topmost). We also size various of the layers to meet process rules and/or to alter the density effect.

Currently, the only MOSIS foundry that requires grounded fill is Agilent/ HP.



Process-Induced Damage (otherwise known as "Antenna Rules") Rules - General Requirements

The "Antenna Rules" deal with process induced gate oxide damage caused when exposed polysilicon and metal structures, connected to a thin oxide transistor, collect charge from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler Nordheim current to flow through the thin oxide. Given the known process charge fluence, a figure of exposed conductor area to transistor gate area ratio is determined which guarantees Time Dependent Dielectric Breakdown (TDDB) reliability requirements for the fabricator. Failure to consider antenna rules in a design may lead to either reduced performance in transistors exposed to process induced damage, or may lead to total failure if the antenna rules are seriously violated.

The polysilicon rules require that the area of the polysilicon over field oxide divided by the area of the transistor gate (thin oxide area) must be less than Np (where Np is a limit that depends on the process and on design targets). For example, a 200 µm long by 1 µm wide polysilicon wire connected to two channel regions of 2 µm X 0.6 µm and 1 µm X 0.6 µm has an antenna ratio of 111. Usually the polysilicon rules are fairly conservative, so the antenna ratio in this example may be in violation of some fabricator's polysilicon antenna rule.

A similar calculation applies to metal wires connected to transistor gates. In this case, you must first obey the Np:1 rule for any polysilicon. Metal antenna rules can be a little more variable depending upon how conservative a fabricator is in dealing with this damage mechanism. The most conservative approach recognizes that process induced damage is a cumulative effect. In this case, you calculate the total area of the poly + metal1 + metal2 + metal3 + ... and divide by the area of the transistor channels connected to this structure. This ratio must be less than Nm.

A less conservative metal antenna rule defines ratios for each metal level (Nm1, Nm2, Nm3, etc.) and recognize that lower levels of metal are protected by inter-level dielectric during the etch process for the metal above. Other metal rules recognize that photoresist covers metal lines during reactive ion etch, so the antenna rule only needs to consider the area of the exposed metal edges. This results in rules defined for area ratio calculations as follows: Ratio = 2[(L_metal+W_metal)*t_metal]/(W_channel*L_channel), where, W_metal, L_metal, and t_metal are the width, length and thickness of the metal line connected to a total channel area defined by W_channel by L_channel.

If metal1 is connected to an active area junction and to a poly structure connected to a transistor channel, then the Nm:1 rule is relaxed. However, the poly Np:1 ratio rule still applies. The reason for this exception is that charge induced current is safely shunted through the junction to the substrate and, therefore, does not cause gate oxide damage. The junction area ratio (A_total/A_junction) must not be more than N_max:1. Note: A_total is the sum of poly and metal area connected to a thin oxide region.

An additional absolute area rule is also imposed for additional safety margin. The total area of exposed conductor that is electrically connected to a gate channel area limited to A_max μm^2. Other constraints may apply, but these constraints are specific to a particular fabricator.

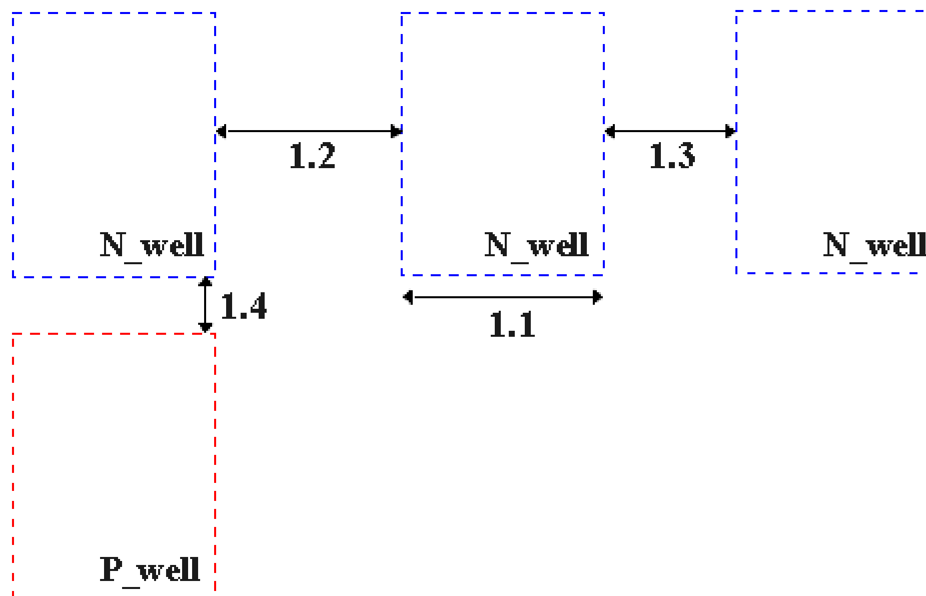
There are layout techniques to help deal with antenna ratio rules. For example, if a design uses a large array of clocked devices connected to a single clock source via a metal1 clock distribution structure then a "cut and link" method can be used to moderate the antenna rule effects. In this method, the metal1 distribution structure is divided up into pieces of metal1 connected to gate structures such that the antenna rule is obeyed. Short links from metal1 to metal2 then back to metal1 connect the clock distribution structure in a way that it prevents the total area of the clock distribution structure from being connected to gate poly structures during metal1 etch. If the metal2 links are the minimum links necessary to make the connection, then the current induced in the metal2 area is very small (Nm2 << metal2 rule).

Specific numbers for the antenna ratio rules are contained in design rules for each fabricator. MOSIS customers can obtain this information in the fabricator rules.

SCMOS Layout Rules - Well

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
1.1	Minimum width	10	12	12
1.2	Minimum spacing between wells at different potential	9 [1]	18 [2]	18
1.3	Minimum spacing between wells at same potential	6 [3]	6 [4]	6
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0	0

Exceptions for AMIS C30 0.35 micron process:
[1] Use lambda=16 for rule 1.2 only when using SCN4M or SCN4ME
[2] Use lambda=21 for rule 1.2 only when using SCN4M_SUBM or SCN4ME_SUBM
[3] Use lambda=8 for rule 1.3 only when using SCN4M or SCN4ME
[4] Use lambda=11 for rule 1.3 only when using SCN4M_SUBM or SCN4ME_SUBM

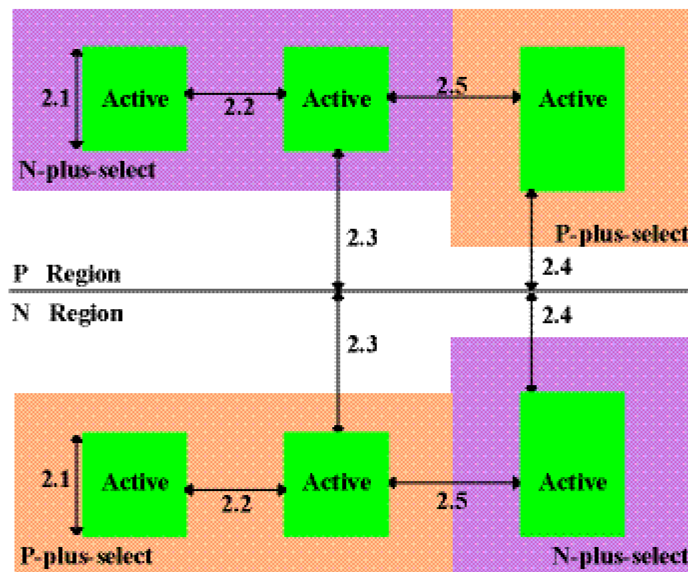


SCMOS Layout Rules - Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
2.1	Minimum width	3 *	3 *	3
2.2	Minimum spacing	3	3	3
2.3	Source/drain active to well edge	5	6	6
2.4	Substrate/well contact active to well edge	3	3	3
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.	4	4	4

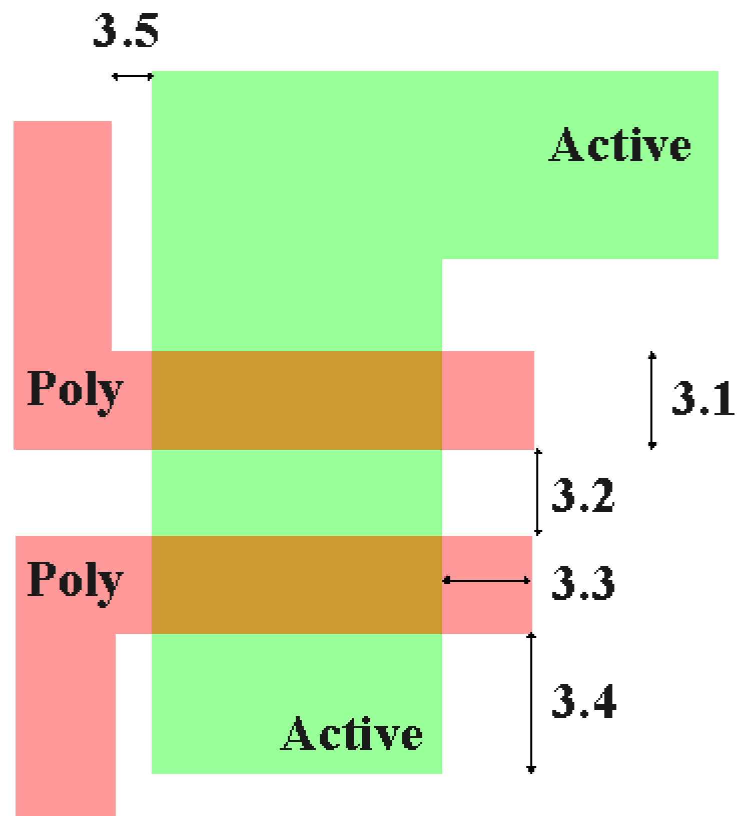
* Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for AMIS designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.

Process	Design Technology	Design Lambda (micrometers)	Minimum Width (lambda)
AMI_ABN	SCNA, SCNE	0.80	5
AMI_C5F/N	SCN3M, SCN3ME	0.35	9
AMI_C5F/N	SCN3M_SUBM, SCN3ME_SUBM	0.30	10



SCMOS Layout Rules - Poly

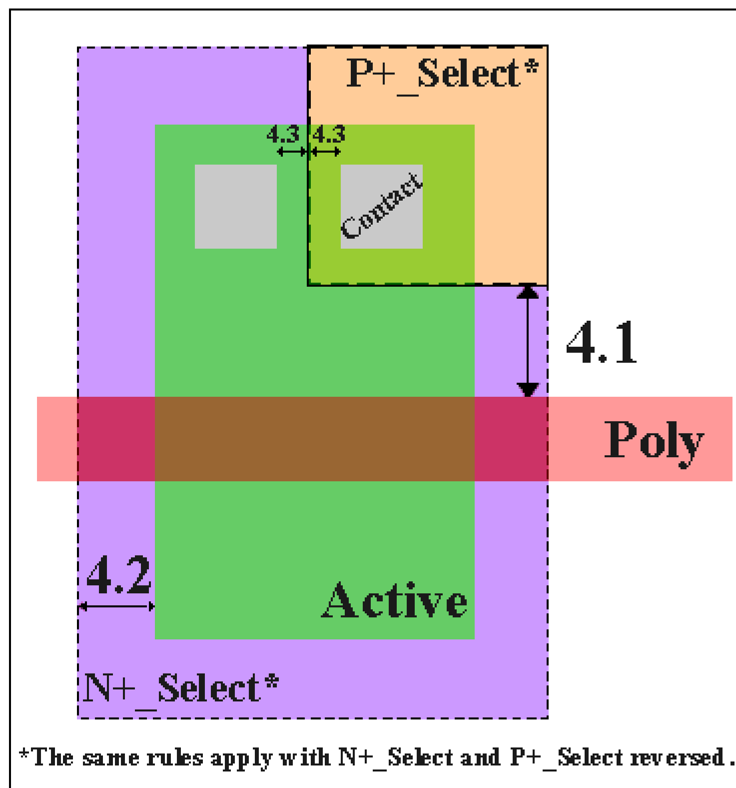
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1



SCMOS Layout Rules - Select

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	3	3
4.2	Minimum select overlap of active	2	2	2
4.3	Minimum select overlap of contact	1	1	1.5
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must not overlap) (not illustrated)	2	2 [1]	4

Exception for AMIS C30 0.35 micron process:
[1] Use lambda=3 for rule 4.4 only when using SCN4M_SUBM or SCN4ME_SUBM



SCMOS Layout Rules - Contact to Poly

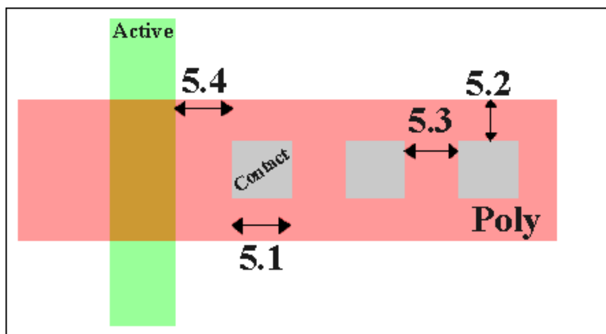
On 0.50 micron process (and all finer feature size processes), it is required that all features on the insulator layers (CONTACT, VIA, VIA2) must be of the single standard size; there are no exceptions for pads (or logos, or anything else); large openings must be replaced by an array of standard sized openings. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.
If your design cannot tolerate 1.5 lambda contact overlap in 5.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 5.1, 5.3, and 5.4, still apply and are unchanged.

Simple Contact to Poly

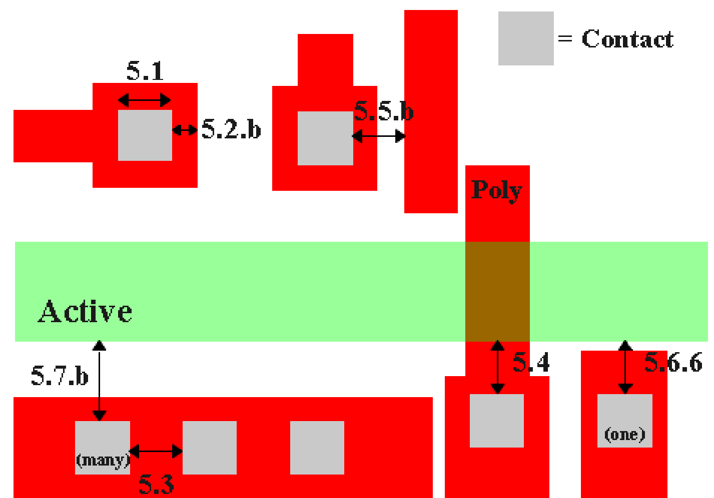
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.1	Exact contact size	2x2	2x2	2x2
5.2	Minimum poly overlap	1.5	1.5	1.5
5.3	Minimum contact spacing	2	3	4
5.4	Minimum spacing to gate of transistor	2	2	2

Alternative Contact to Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.2.b	Minimum poly overlap	1	1	1
5.5.b	Minimum spacing to other poly	4	5	5
5.6.b	Minimum spacing to active (one contact)	2	2	2
5.7.b	Minimum spacing to active (many contacts)	3	3	3



Simple Poly to Contact



Alternative Contact to Poly

SCMOS Layout Rules - Contact to Active

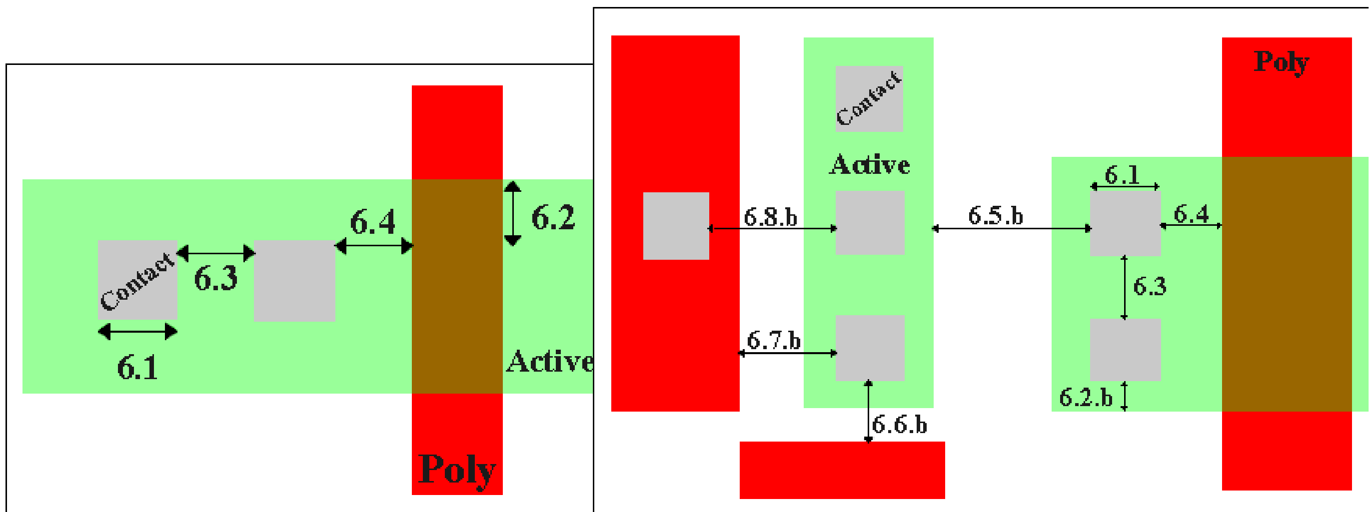
If your design cannot handle the 1.5 lambda contact overlap in 6.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 6.1, 6.3, and 6.4, still apply and are unchanged. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

Simple Contact to Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
6.1	Exact contact size	2x2	2x2	2x2
6.2	Minimum active overlap	1.5	1.5	1.5
6.3	Minimum contact spacing	2	3	4
6.4	Minimum spacing to gate of transistor	2	2	2

Alternative Contact to Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
6.2.b	Minimum active overlap	1	1	1
6.5.b	Minimum spacing to diffusion active	5	5	5
6.6.b	Minimum spacing to field poly (one contact)	2	2	2
6.7.b	Minimum spacing to field poly (many contacts)	3	3	3
6.8.b	Minimum spacing to poly contact	4	4	4

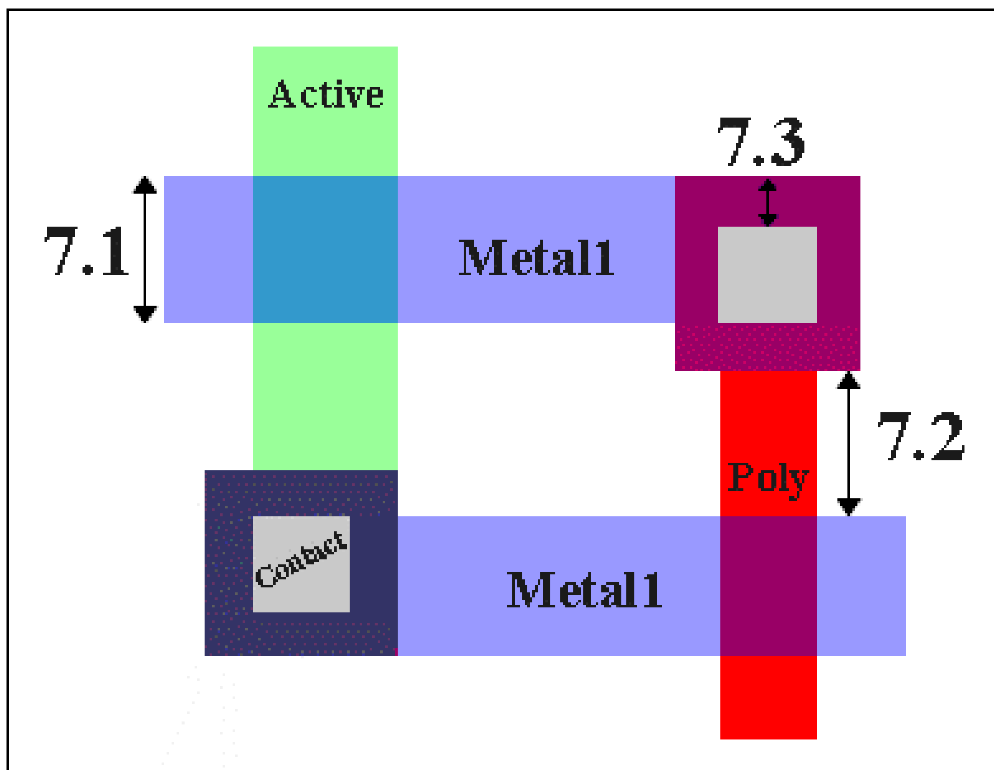


Simple Contact to Active

Alternative Contact to Active

SCMOS Layout Rules - Metal1

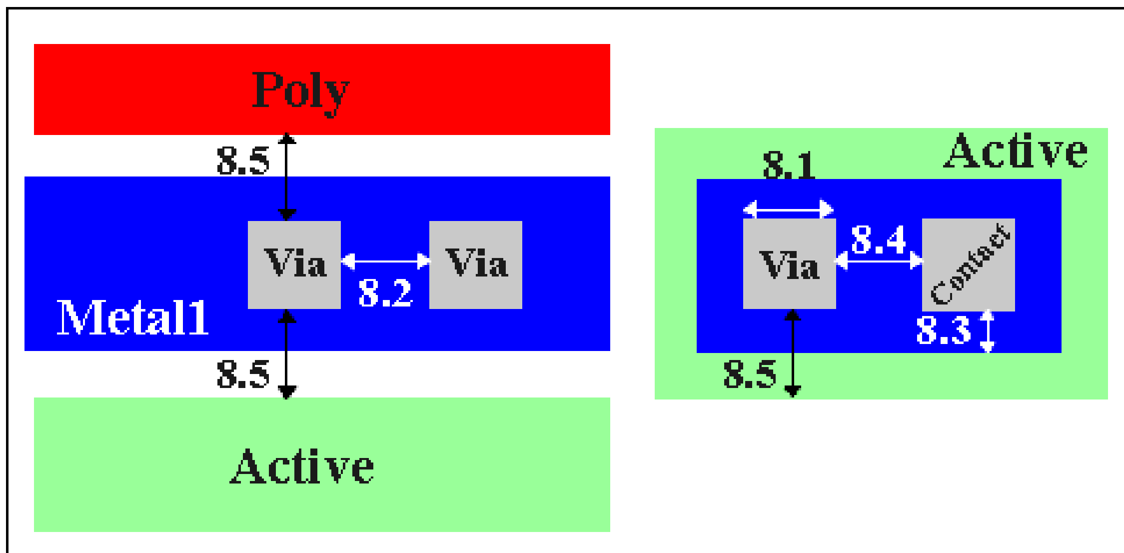
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
7.1	Minimum width	3	3	3
7.2	Minimum spacing	2	3	3
7.3	Minimum overlap of any contact	1	1	1
7.4	Minimum spacing when either metal line is wider than 10 lambda	4	6	6



SCMOS Layout Rules - Via

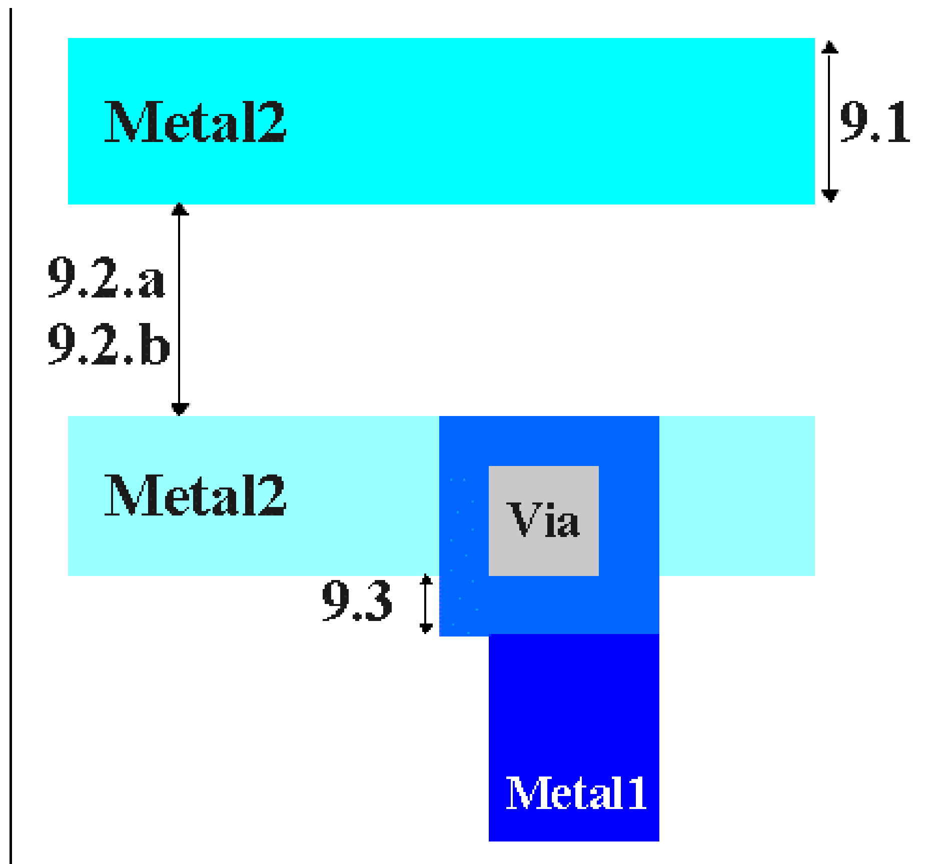
Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
8.1	Exact size	2 x 2	n/a	n/a	2 x 2	2 x 2	3 x 3
8.2	Minimum via1 spacing	3	n/a	n/a	3	3	3
8.3	Minimum overlap by metal1	1	n/a	n/a	1	1	1
8.4	Minimum spacing to contact for technology codes mapped to processes that do not allow stacked vias (SCNA, SCNE, SCN3M, SCN3MLC)	2	n/a	n/a	2	2	n/a
8.5	Minimum spacing to poly or active edge	2	n/a	n/a	2	2	n/a



SCMOS Layout Rules - Metal2

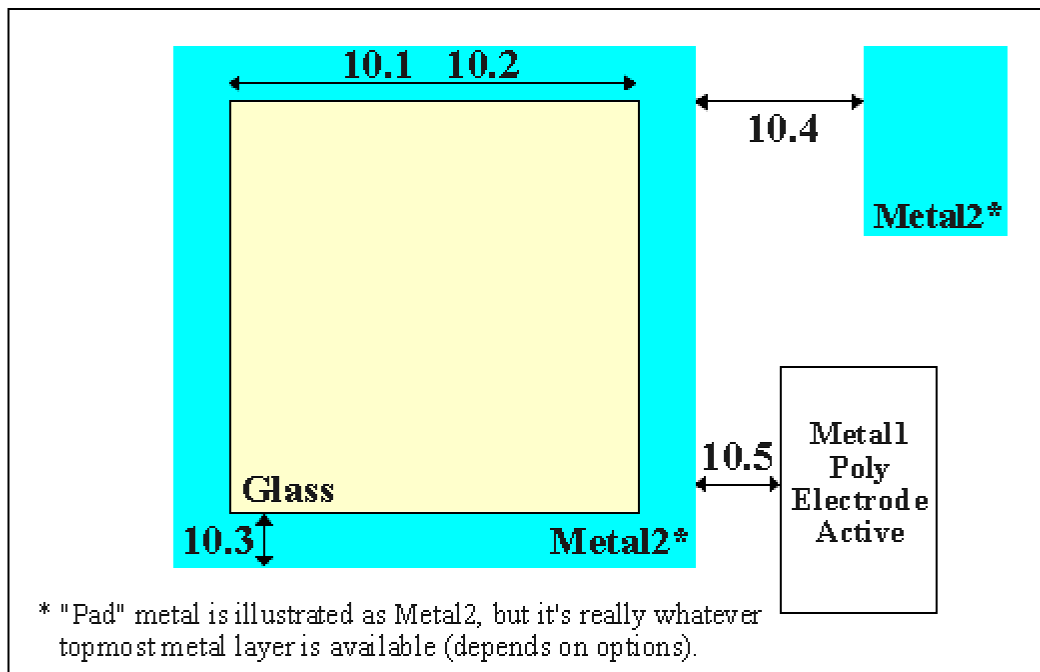
Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
9.1	Minimum width	3	n/a	n/a	3	3	3
9.2	Minimum spacing	3	n/a	n/a	3	3	4
9.3	Minimum overlap of via1	1	n/a	n/a	1	1	1
9.4	Minimum spacing when either metal line is wider than 10 lambda	6	n/a	n/a	6	6	8



SCMOS Layout Rules - Overglass

Note that rules in this section are in units of microns. They are not "true" design rules, but they do make good practice rules. Unfortunately, there are no really good generic pad design rules since pads are process-specific.

Rule	Description	Microns
10.1	Minimum bonding passivation opening	60
10.2	Minimum probe passivation opening	20
10.3	Pad metal overlap of passivation	6
10.4	Minimum pad spacing to unrelated metal	30
10.5	Minimum pad spacing to active, poly or poly2	15

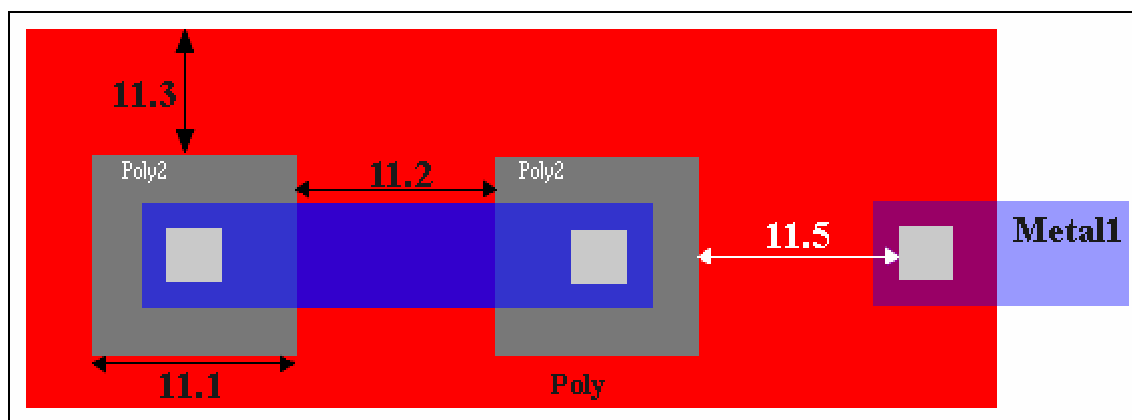


SCMOS Layout Rules - Poly2 for Capacitor

The poly2 layer is a second polysilicon layer (physically above the standard, or first, poly layer). The oxide between the two polys is the capacitor dielectric. The capacitor area is the area of coincident poly and electrode.

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
11.1	Minimum width	3 [1]	7 [2]	n/a
11.2	Minimum spacing	3 [3]	3 [4]	n/a
11.3	Minimum poly overlap	2 [5]	5 [6]	n/a
11.4	Minimum spacing to active or well edge (not illustrated)	2	2	n/a
11.5	Minimum spacing to poly contact	3	6	n/a
11.6	Minimum spacing to *unrelated metal*	2	2	n/a

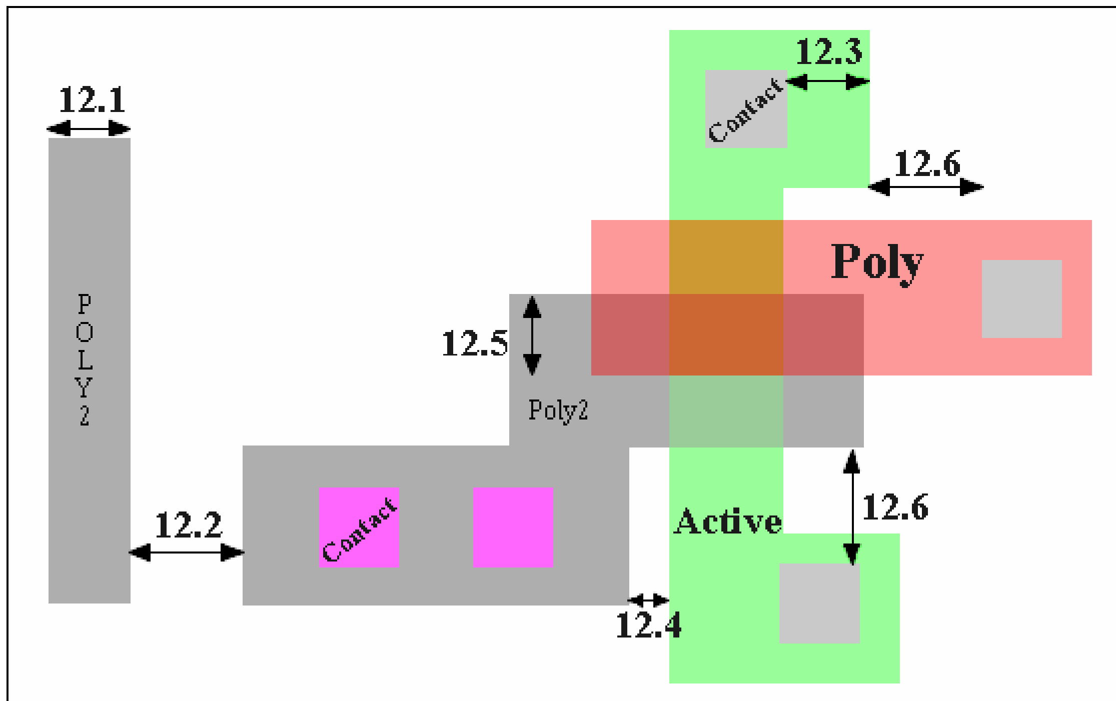
Exceptions for AMIS C30 0.35 micron process:
[1] Use lambda=8 for rule 11.1 only when using SCN4ME
[2] Use lambda=10 for rule 11.1 only when using SCN4ME_SUBM
[3] Use lambda=4 for rule 11.2 only when using SCN4ME
[4] Use lambda=4 for rule 11.2 only when using SCN4ME_SUBM
[5] Use lambda=5 for rule 11.3 only when using SCN4ME
[6] Use lambda=6 for rule 11.3 only when using SCN4ME_SUBM



SCMOS Layout Rules - Poly2 for Transistor
Same poly2 layer as for caps

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
12.1	Minimum width	2	2	n/a
12.2	Minimum spacing	3 [1]	3 [2]	n/a
12.3	Minimum electrode gate overlap of active	2	2	n/a
12.4	Minimum spacing to active	1	1	n/a
12.5	Minimum spacing or overlap of poly	2	2	n/a
12.6	Minimum spacing to poly or active contact	3	3	n/a

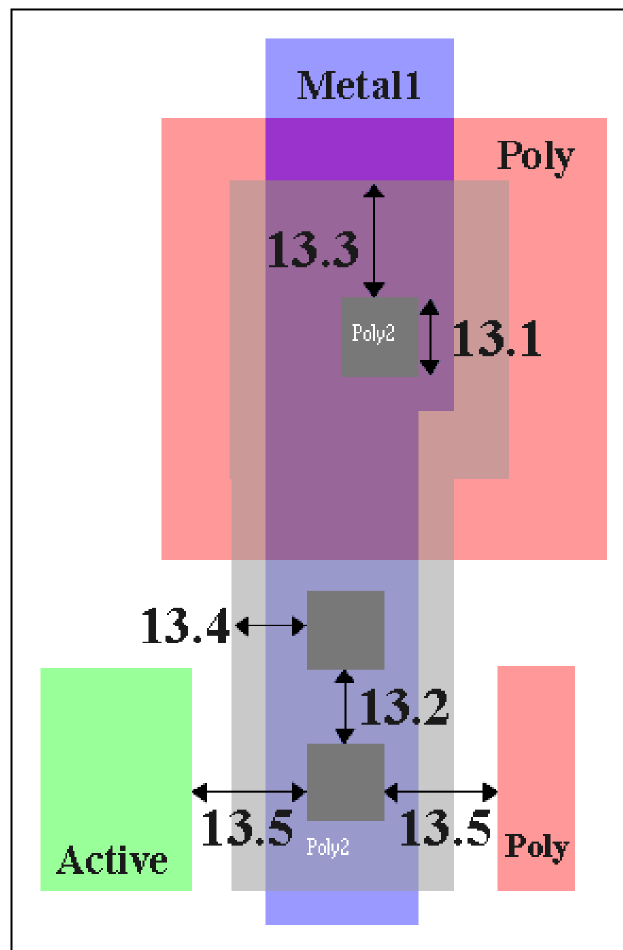
Exceptions for AMIS C30 0.35 micron process:
[1] Use lambda=4 for rule 12.2 only when using SCN4ME
[2] Use lambda=4 for rule 12.2 only when using SCN4ME_SUBM



SCMOS Layout Rules - Poly2 Contact

The poly2 is contacted through the standard contact layer, similar to the first poly. The overlap numbers are larger, however.
Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

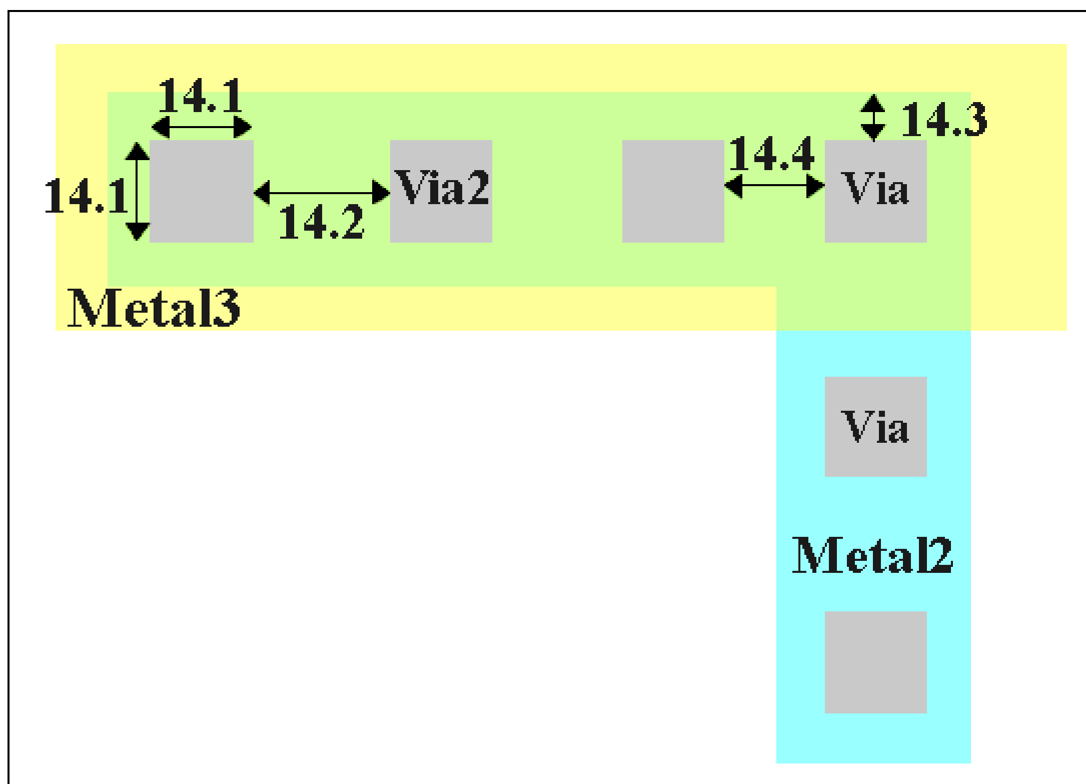
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
13.1	Exact contact size	2 x 2	2 x 2	n/a
13.2	Minimum contact spacing	2	3	n/a
13.3	Minimum Poly2 overlap (on capacitor)	3	3	n/a
13.4	Minimum Poly2 overlap (not on capacitor)	2	2	n/a
13.5	Minimum spacing to poly or active	3	3	n/a



SCMOS Layout Rules - Via2

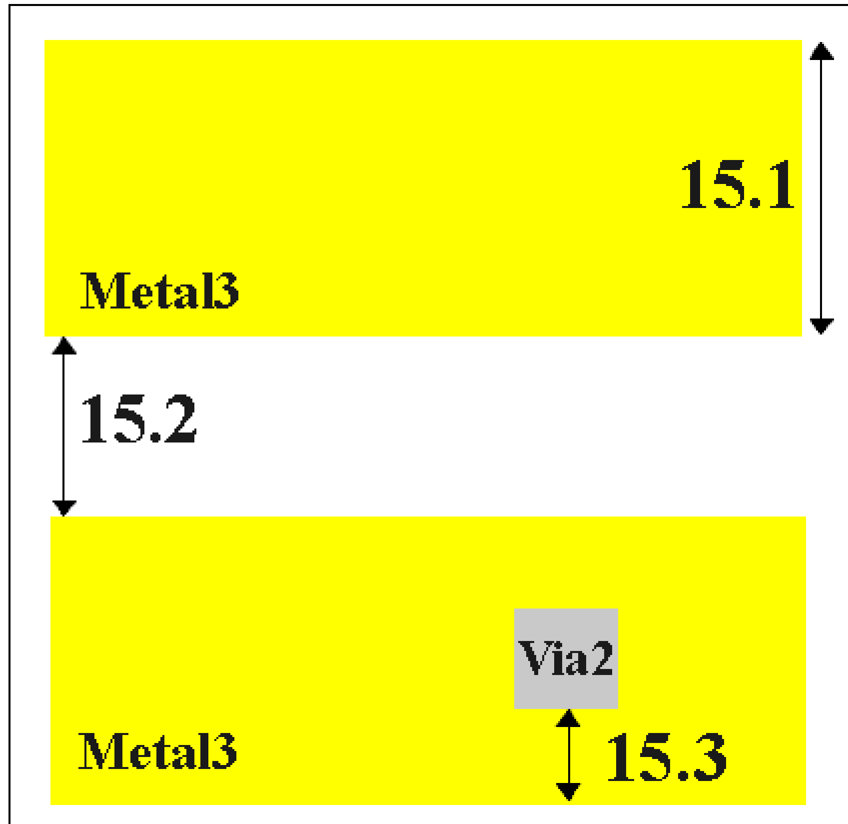
Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda					
		3 Metal Process			4+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
14.1	Exact size	2x2	2x2	n/a	2x2	2x2	3x3
14.2	Minimum spacing	3	3	n/a	3	3	3
14.3	Minimum overlap by metal2	1	1	n/a	1	1	1
14.4	Minimum spacing to via1 for technology codes that do not allow stacked vias (SCNA, SCNE, SCN3M, SCN3ME, SCN3MLC)	2	2	n/a	2	2	n/a
14.5	Via2 may be placed over contact						



SCMOS Layout Rules - Metal3

Rule	Description	Lambda					
		3 Metal Process			4+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
15.1	Minimum width	6	5	n/a	3	3	3
15.2	Minimum spacing to metal3	4	3	n/a	3	3	4
15.3	Minimum overlap of via2	2	2	n/a	1	1	1
15.4	Minimum spacing when either metal line is wider than 10 lambda	8	6	n/a	6	6	8

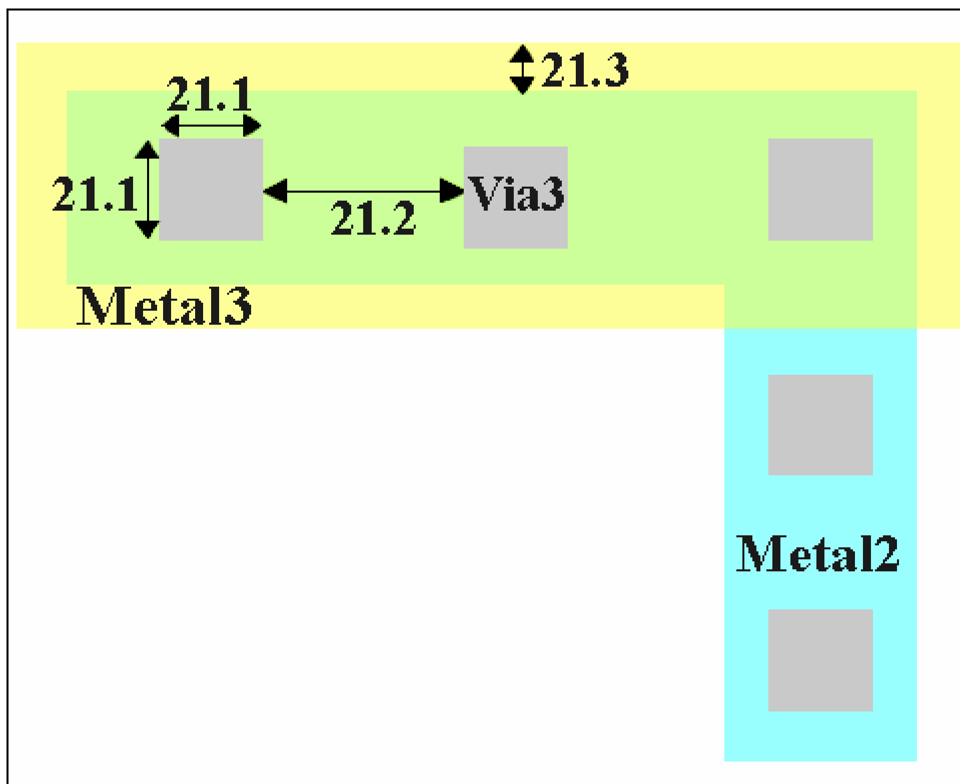


SCMOS Layout Rules - Via3

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

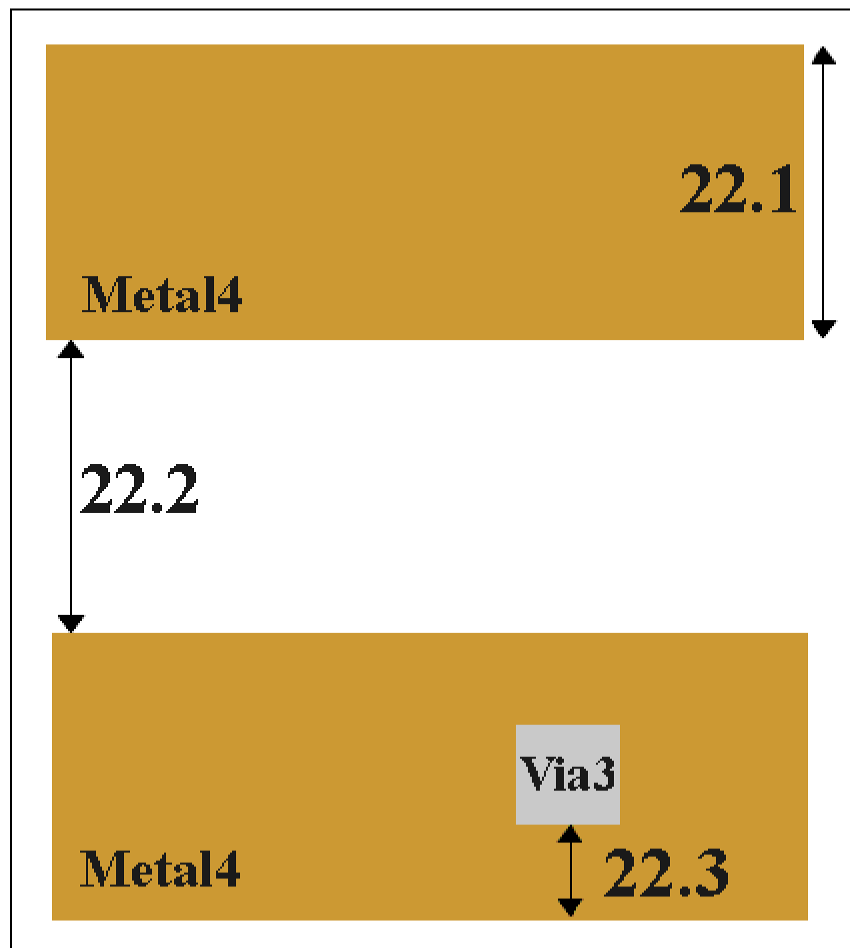
Rule	Description	Lambda					
		4 metal Process			5+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
21.1	Exact size	2x2	2x2	n/a	n/a	2x2	3x3
21.2	Minimum spacing	3	3 *	n/a	n/a	3	3
21.3	Minimum overlap by Metal3	1	1	n/a	n/a	1	1

Exception: Use lambda=4 for rule 21.2 only when using SCN4M_SUBM for Agilent/HP GMOS10QA 0.35 micron process



SCMOS Layout Rules - Metal4

Rule	Description	Lambda					
		4 Metal Process			5+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
22.1	METAL4 width	6	6	n/a	n/a	3	3
22.2	METAL4 space	6	6	n/a	n/a	3	4
22.3	METAL4 overlap of VIA3	2	2	n/a	n/a	1	1
22.4	Minimum spacing when either metal line is wider than 10 lambda	12	12	n/a	n/a	6	8



SCMOS Layout Rules - Via4
(SUBM and DEEP)

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda					
		5 Metal Process			6+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
25.1	Exact size	n/a	2x2	3x3	n/a	2x2	3x3
25.2	Minimum spacing	n/a	3	3	n/a	3	3
25.3	Minimum overlap by Metal4	n/a	1	1	n/a	1	1

SCMOS Layout Rules - Metal5
(SUBM and DEEP)

Any designer using the SCMOS rules who wants the TSMC Thick_Top_Metal must draw the top metal to comply with the TSMC rules for that layer.

Rule	Description	Lambda					
		5 Metal Process			6+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
26.1	Minimum width	n/a	4	4	n/a	3	3
26.2	Minimum spacing to Metal5	n/a	4	4	n/a	3	4
26.3	Minimum overlap of Via4	n/a	1	2	n/a	1	1
26.4	Minimum spacing when either metal line is wider than 10 lambda	n/a	8	8	n/a	6	8

SCMOS Layout Rules - High Res

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
27.1	Minimum HR width	4	4	n/a
27.2	Minimum HR spacing	4	4	n/a
27.3	Minimum spacing, HR to contact (no contacts allowed inside HR)	2	2	n/a
27.4	Minimum spacing, HR to external active	2	2	n/a
27.5	Minimum spacing, HR to external poly2	2	2	n/a
27.6	Resistor is poly2 inside HR; poly2 ends stick out for contacts, the entire resistor must be outside well and over field			
27.7	Minimum poly2 width in resistor	5	5	n/a
27.8	Minimum spacing of poly2 resistors (in a single HR region)	7	7	n/a
27.9	Minimum HR overlap of poly2	2	2	n/a

SCMOS Layout Rules - Via5 (SUBM and DEEP)

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda		
		6 Metal Process		
		SCMOS	SUBM	DEEP
29.1	Exact size	n/a	3 x 3	4 x 4
29.2	Minimum spacing	n/a	4	4
29.3	Minimum overlap by Metal5	n/a	1	1

SCMOS Layout Rules - Metal6 (SUBM and DEEP)

Any designer using the SCMOS rules who wants the TSMC Thick_Top_Metal must draw the top metal to comply with the TSMC rules for that layer.

Rule	Description	Lambda		
		6 Metal Process		
		SCMOS	SUBM	DEEP
30.1	Minimum width	n/a	5	5
30.2	Minimum spacing to Metal6	n/a	5	5
30.3	Minimum overlap of Via5	n/a	1	2
30.4	Minimum spacing when either metal line is wider than 10 lambda	n/a	10	10

SCMOS Layout Rules - DEEP_N_WELL for SCMOS_DEEP (and SUBM)

The DEEP_N_WELL layer provides access to the DNW layer in the TSMC 0.18 and 0.25 processes. This provides a layering sometimes called "triple-well" in which an n-well sits in the p-substrate, and then a p-well sits fully inside of the n-well; it is then possible to construct NMOS devices inside of that isolated p-well. The isolated p-well is surrounded by a fence of standard N_WELL (around its periphery), and by DEEP_N_WELL underneath. The N_WELL fence makes direct electrical contact with the DEEP_N_WELL plate beneath it.

DEEP_N_WELL is available in technology codes SCN5M_SUBM, SCN5M_DEEP, SCN6M_SUBM and SCN6M_DEEP but only where these are to be fabricated on TSMC foundry runs. To gain a better understanding of this layer, the TSMC vendor-rule design rule documentation should be studied.

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
31.1	Minimum Width, Deep_N_Well	n/a	30	34
31.2	Minimum Spacing, Deep_N_Well to Deep_N_Well	n/a	50	56
31.3	Minimum extension, N_Well beyond Deep_N_Well edge	n/a	15	17
31.4	Minimum overlap, N_Well over Deep_N_Well edge	n/a	20	23
31.5	Minimum spacing, Deep_N_Well to unrelated N_Well	n/a	35	39
31.6	Minimum spacing, N+Active in isolated P-well, to N_Well	n/a	5	6
31.7	Minimum spacing, external N+Active to Deep_N_Well	n/a	30	34
31.8	Minimum spacing, P+Active in N_Well to its Deep_N_Well	n/a	10	13