The Basics of Testing Operation Amplifiers: Three Methods

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Purpose

- This paper will provide information on three operational amplifier test methods which have a proven track record.

- Frequently we get questions about how to test opamps. This paper will serve as a teaching tool that we can use to help people quickly learn the various methods.

- The presentation will discuss the tradeoffs and how to make the best test circuit choice.

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Test Method Outline

- Overview of the three test circuits.

- Iq (Quiescent Current)

- Vos (Input Offset Voltage)

- PSRR (Power Supply Rejection Ratio)

- CMRR (Common Mode Rejection Ratio)

- Ib, Ios (Input Bias Current, Input Offset Current)

- Aol (DC Open Loop Gain)

- Putting it all together

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Method 1 – Self Test Circuit

- The "Self Test" method uses the DUT itself to perform the test. It is sometimes called the false summing junction method.
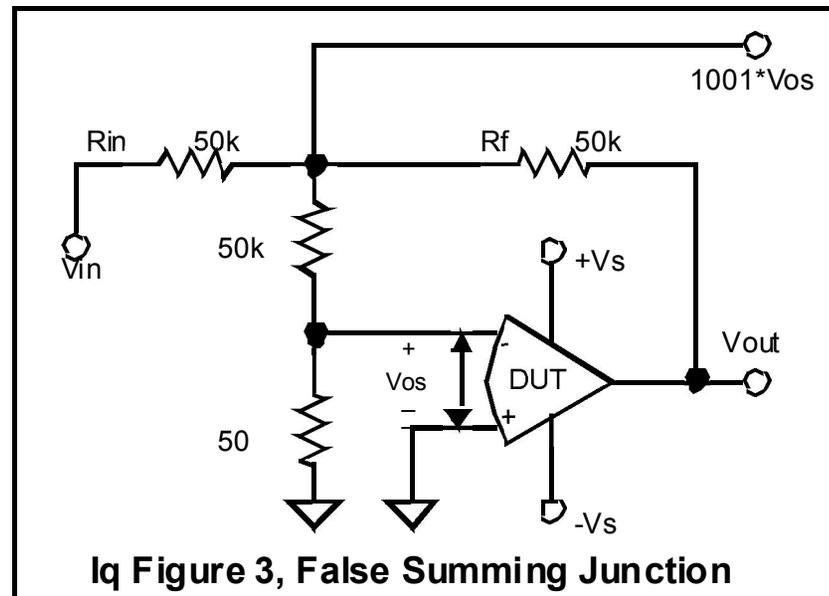
Iq Figure 3, False Summing Junction

TEXAS INSTRUMENTS

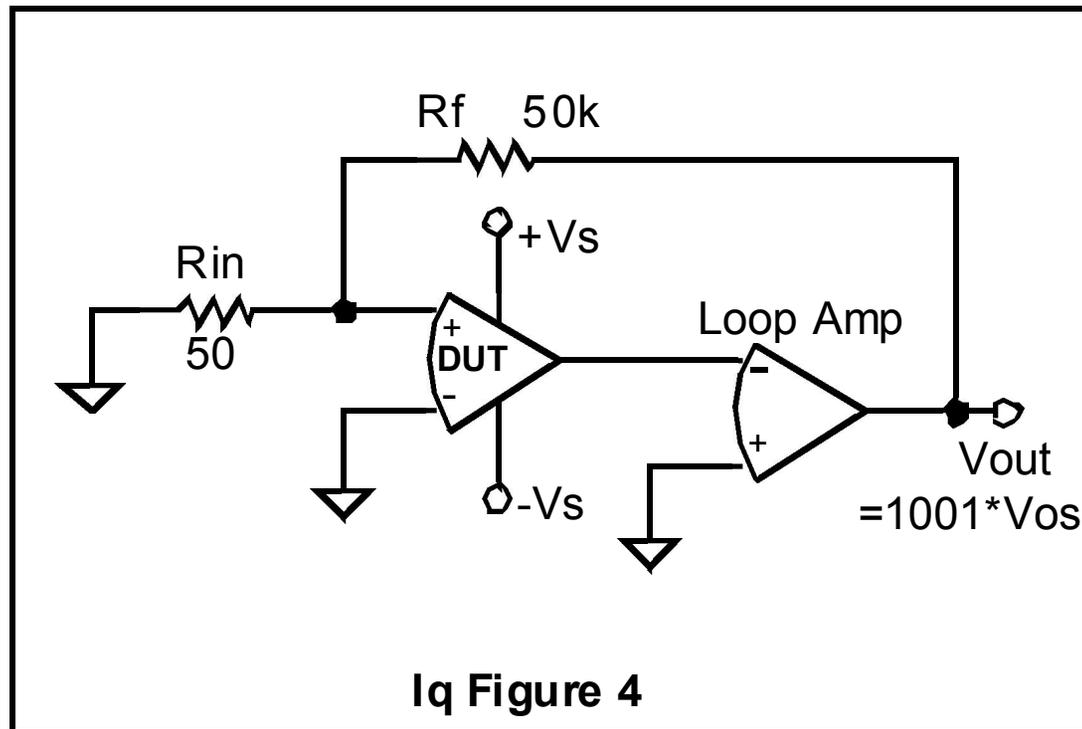# Method 1 - Self Test Circuit

- Advantages
  - Simplicity of design
  - Most stable of the three methods

- Disadvantages
  - Can be slower
  - Low Iq parts are difficult to test

Continued

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Method 2 – Two Amp Loop

- The "Two Amp Loop" method uses another "Loop Amplifier" to perform the tests.

Iq Figure 4

Method 2 – Two Amp Loop
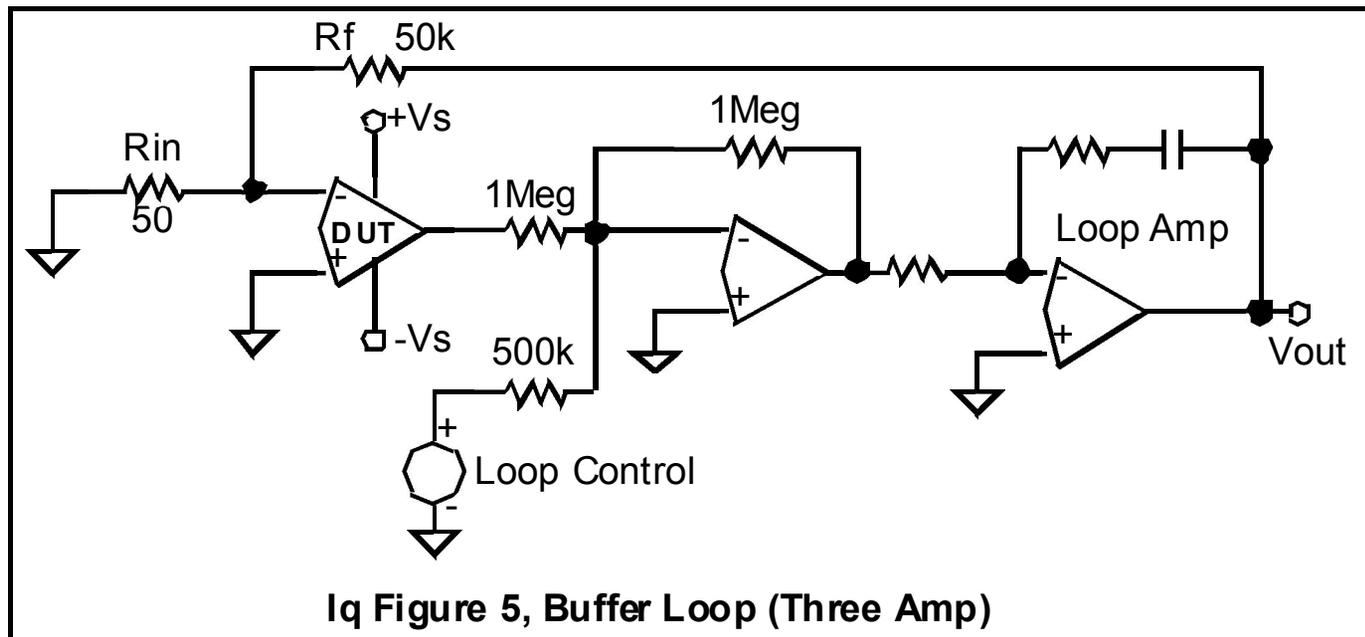
- ## Advantages
  - Accurate control of DUT output voltage
  - Usually faster testing

- ## Disadvantages
  - Stability – Compensation <u>must</u> be correct
  - Not useful for DUTs with variable gain/phase

Continued

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Method 3 – Three Amp Loop

- The "Three Amp Loop" method uses two additional amplifier to perform the tests.

Iq Figure 5, Buffer Loop (Three Amp)

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Method 3 – Three Amp Loop

- ## Advantages
    - Accurate control of DUT output voltage
    - Usually faster testing
    - DUT power supplies can be > Loop amps

- ## Disadvantages
    - Stability – Compensation <u>must</u> be correct
    - Not useful for DUTs with variable gain/phase
    - There is always a 1Meg load on the DUT
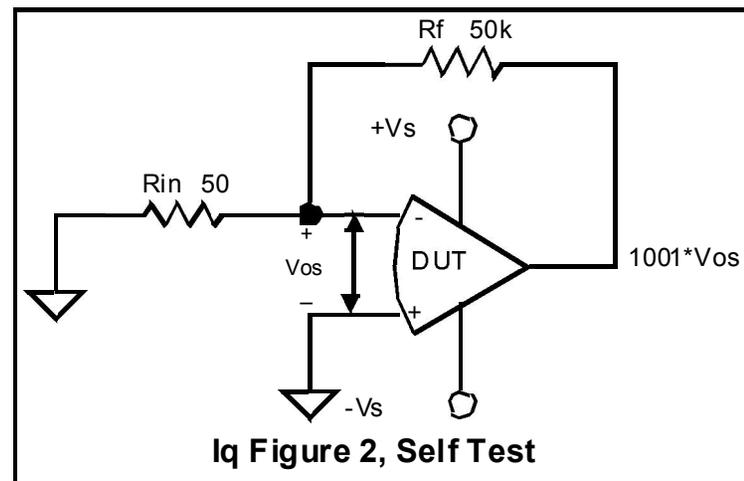
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Iq (Quiescent Current)

- Definition - the current consumed by the part with the output current equal to zero

- This circuit satisfies this requirement. Ib- will generally be very small and not contribute any significant error to the quiescent current measurement. However, this circuit doesn't allow testing other device parameters and is therefore not very useful.

Iq Figure 1

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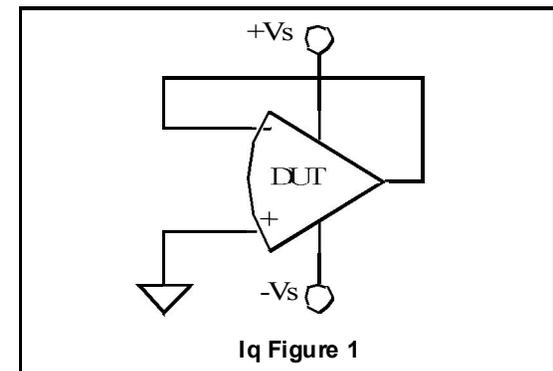
Iq (Quiescent Current)

- This circuit is more practical, but still only allows two parameters to be easily tested.

Rf   50k

+Vs

Rin   50

-

DUT   1001*Vos

Vos

+

-Vs

Iq Figure 2, Self Test

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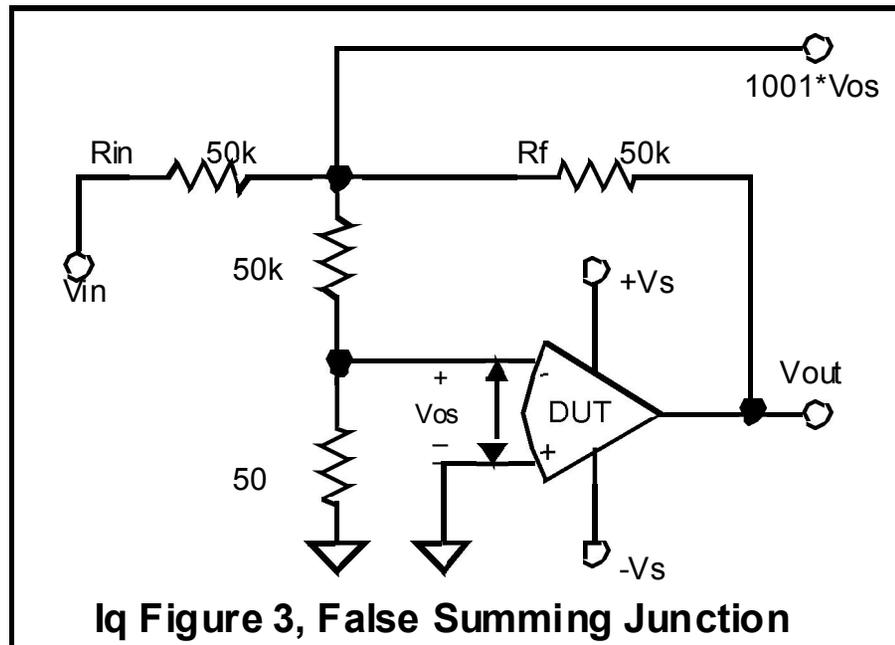
Iq (Quiescent Current)

Figure 3 represents a more practical circuit for measuring the quiescent current in very low quiescent current parts. In this implementation the output can be adjusted to zero output current by controlling Vin, not always and easy task
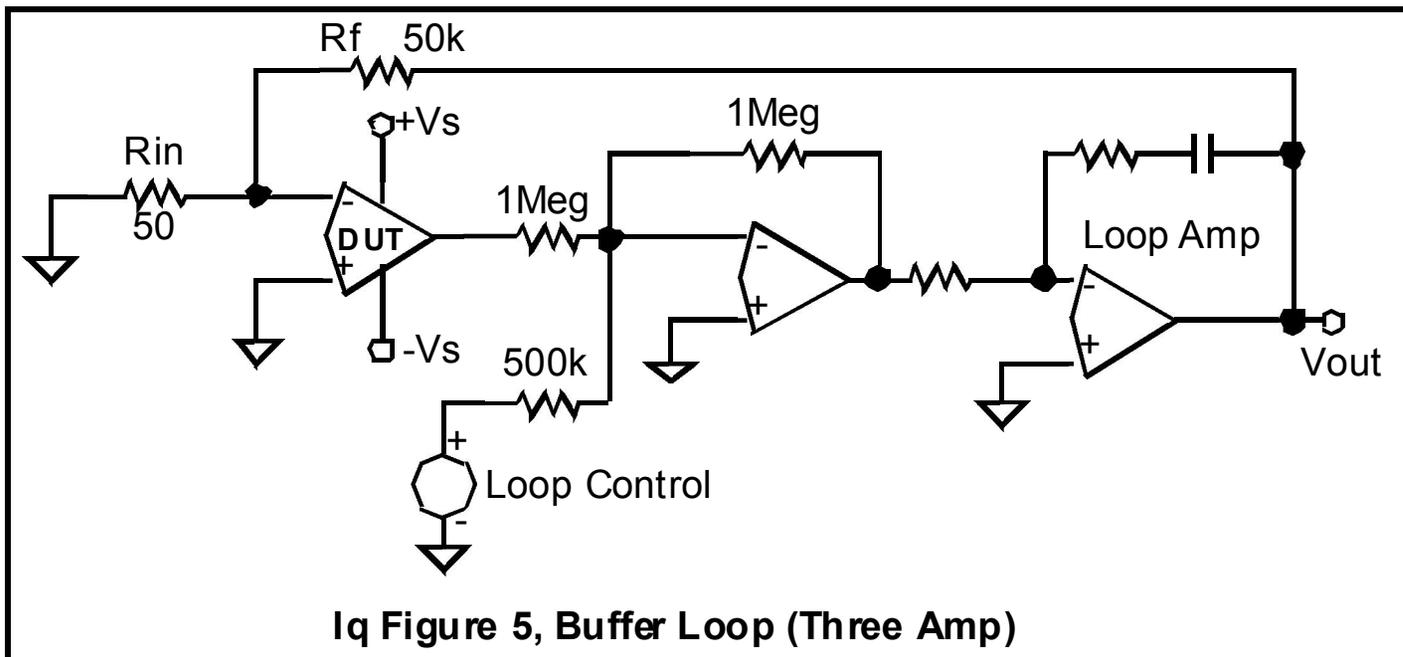

Iq Figure 3, False Summing Junction

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Iq (Quiescent Current)

The three amp loop in Figure 5 can also be used to measure Iq, but care must be taken as there is always a 1 Meg ohm resistor at the output of the DUT.

Iq Figure 5, Buffer Loop (Three Amp)

Continued

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a1   The three amp loop in Figure 5 can also be used to measure Iq, but care must be taken as there is always a 1 Meg ohm resistor at the output of the DUT.
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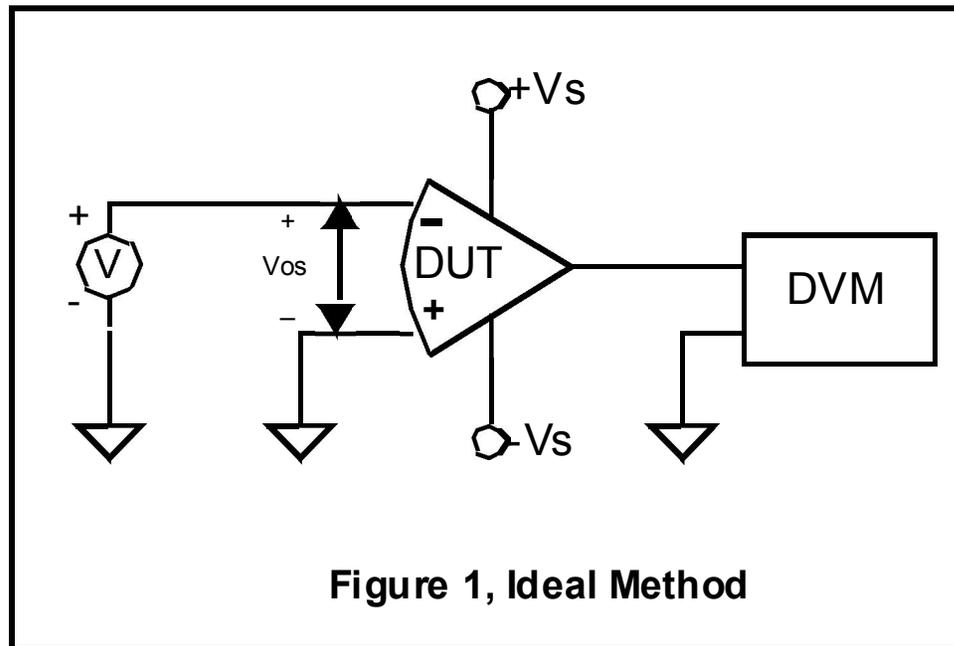
Vos – Input Offset Voltage

Definition – "the differential dc input voltage required to provide zero output voltage with no input signal or source resistance."

Figure 1, Ideal Method

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a3 The Input Offset Voltage, Vos, is variously defined as, "the differential dc input voltage required to provide zero output voltage with no input signal or source resistance," or "the differential dc input voltage require to provide zero output voltage, with no other input signal and zero resistance in either input terminal path to ground," or "the differential dc input voltage required to provide zero voltage at the output of an operational amplifier when the input bias current is zero." This would suggest an "ideal" theoretical method for testing the Input Offset Voltage which is impractical. The definition would suggest that one should connect a low output, variable voltage source with high accuracy and resolution to the input of the operational amplifier and adjust the input voltage until the output voltage is zero. Then the input offset voltage would simply be the inverse of the input voltage applied. There are two serious problems with this method. With operational amplifiers with very high open loop gain, the resolution of the voltage source would have to be less than a microvolt to guarantee any degree of repeatability and an iterative approach would need to be used to drive the output to zero. This would be costly in time if it could ever be achieved. Noise in the system, coupling into the voltage source and operational amplifier, would make the measurement and control next to impossible in a high speed automated test environment.

Graeme, Jerald G., Tobey, Gene E., Huelsman, Lawrence P., "Operational Amplifers, Design and Applications", McGraw Hill Book Company, New York, p 454, 1971

Wait, John V., Huelsman, Lawrence P., Korn, Granino A., ôIntroduction to Operational Amplifier Theory and Applications,ö McGraw Hill Book Company, New York, p 101, 1975

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Vos – Input Offset Voltage

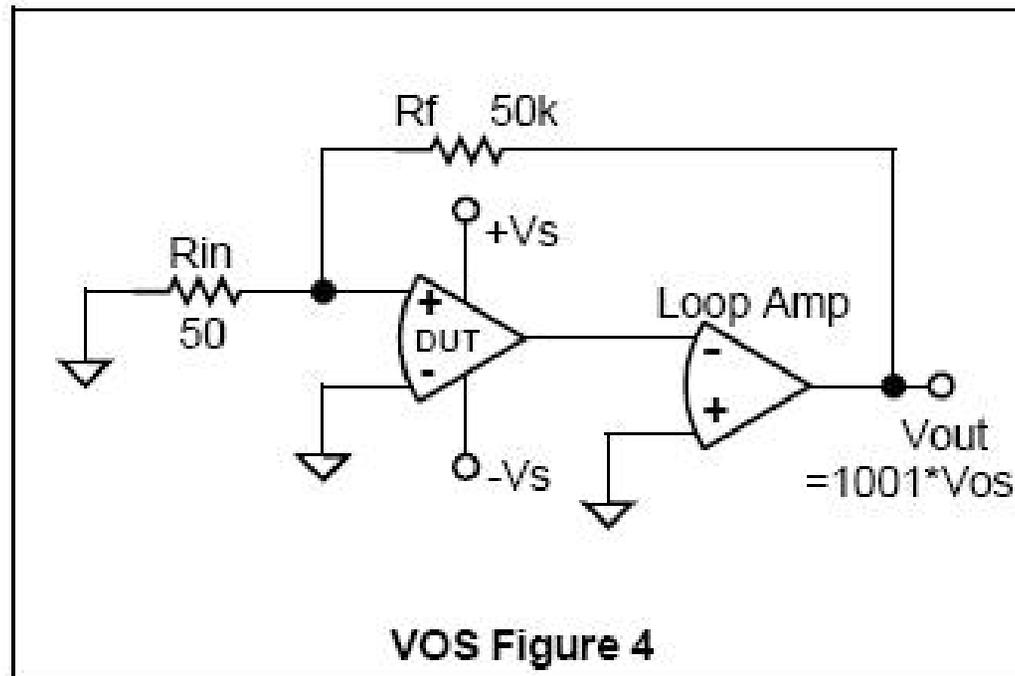This shows the configuration for measuring Vos using the "false summing junction" method.

VOS Figure 3, False Summing Junction

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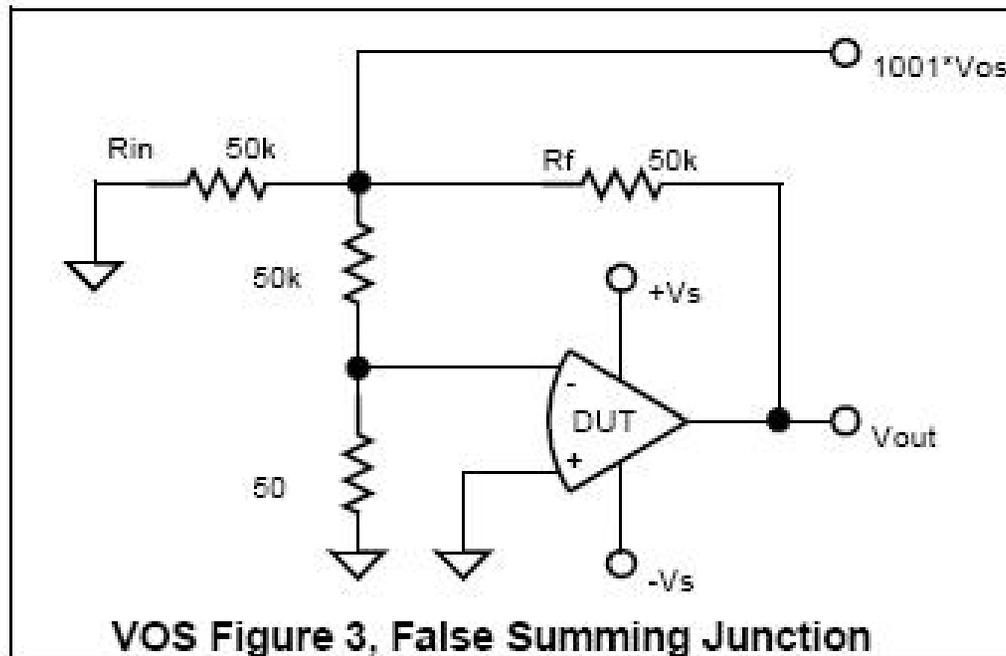
Vos – Input Offset Voltage

Offset voltage is easy to measure with the two amplifier loop.

VOS Figure 4

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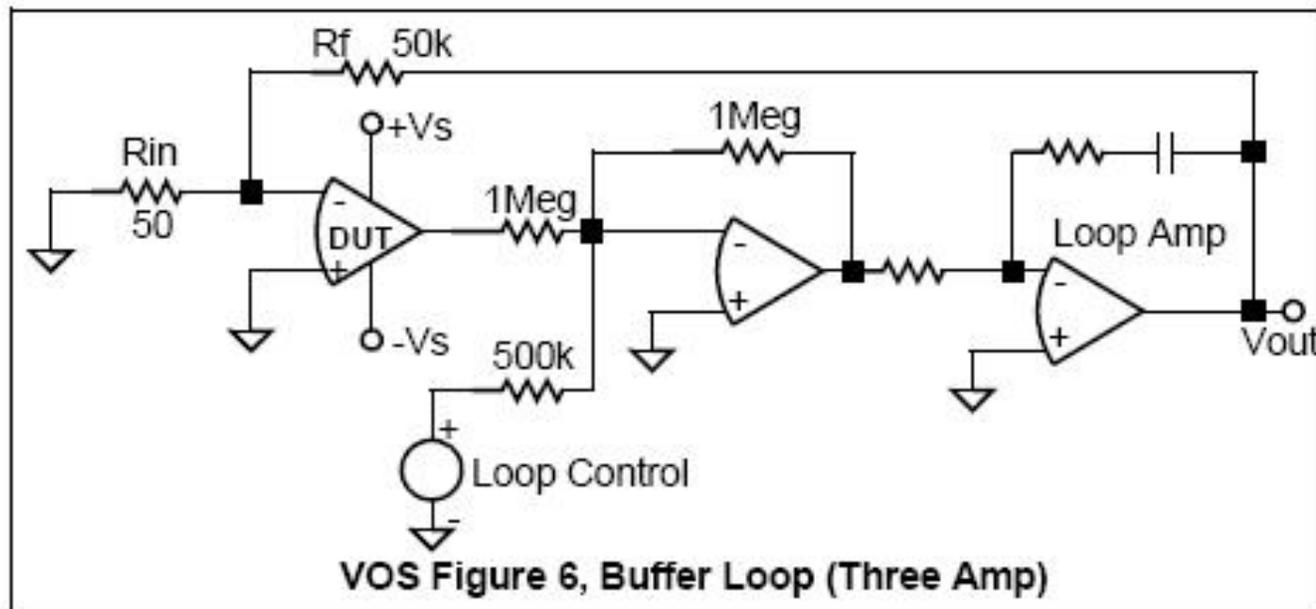
Vos – Input Offset Voltage

The three amplifier loop must be kept stable by the appropriate selection of resistor and capacitor on the far right amplifier.
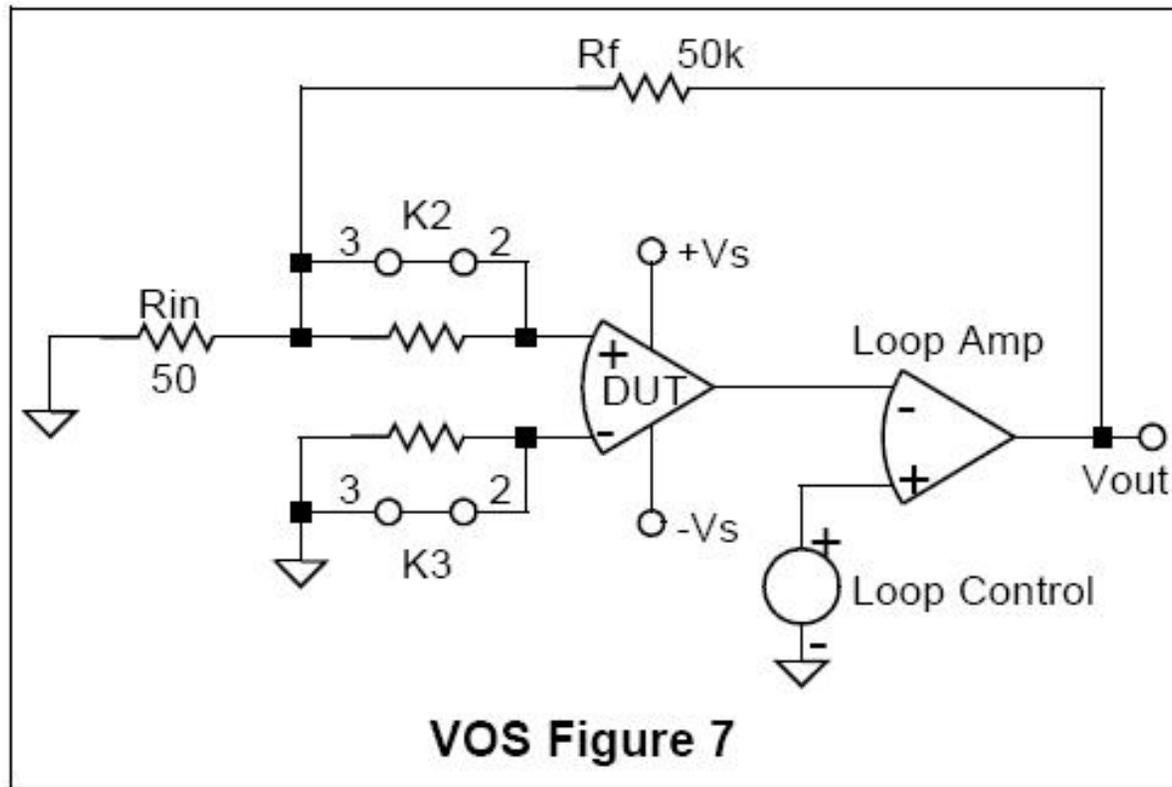

VOS Figure 6, Buffer Loop (Three Amp)

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Vos – Input Offset Voltage "Errors"

Sources of error may not be obvious!

VOS Figure 7

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Vos – Input Offset Voltage "Errors"

This shows sources of error due to Thermal EMF.

VOS Figure 8, Sources of Error

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Vos – Input Offset Voltage "Errors"

A. Thermally Generated EMFs caused by:

– Relay Contacts

– Solder Joints

– SWAP Block Pogo Pin Connections

– Automated handler contacts and sockets.

B. Leakage currents caused by:

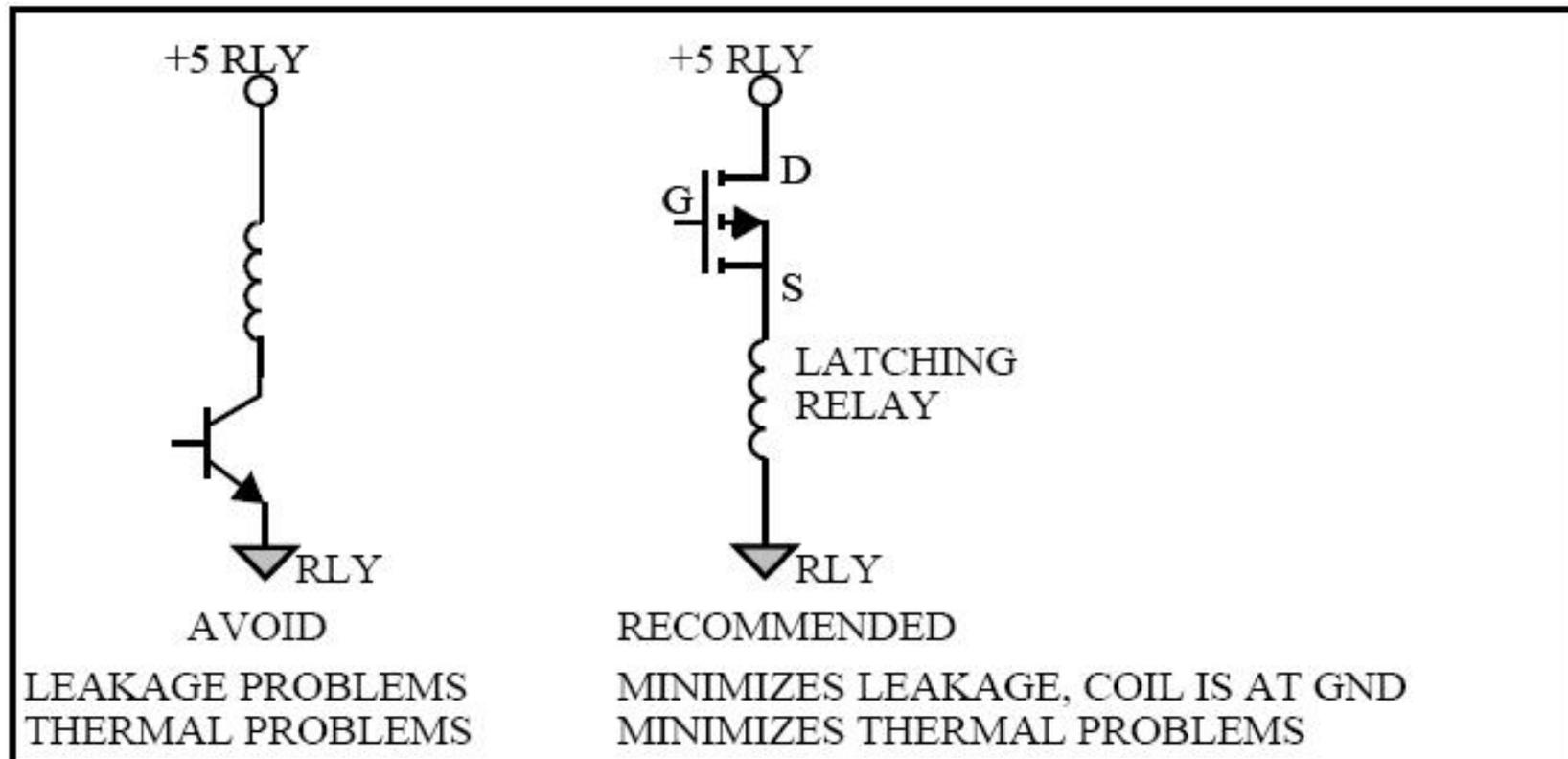– Power Supplies

– Relay Control and supply traces.

C. Noise

– Environment

– Testers

– components, for example: resistor noise

Continued

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Practical Design Considerations for Test Boards

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Practical Design Considerations for Test Boards

Design Considerations for Solder Selection

● Sn 99-Ag 1	+3.2 µV/°C
● Sn 63-Pb 37	-3.2 µV/°C
● Sn 50-Pb 50	-3.1 µV/°C
● Sn 18-Pb 82	-2.8 µV/°C
● Sn 40-Cd 60	+0.01 µV/°C
● Sn 81-Bi 19	0.0 µV/°C

Bismuth and Cadmium solders have the best performance
Their cost is high.

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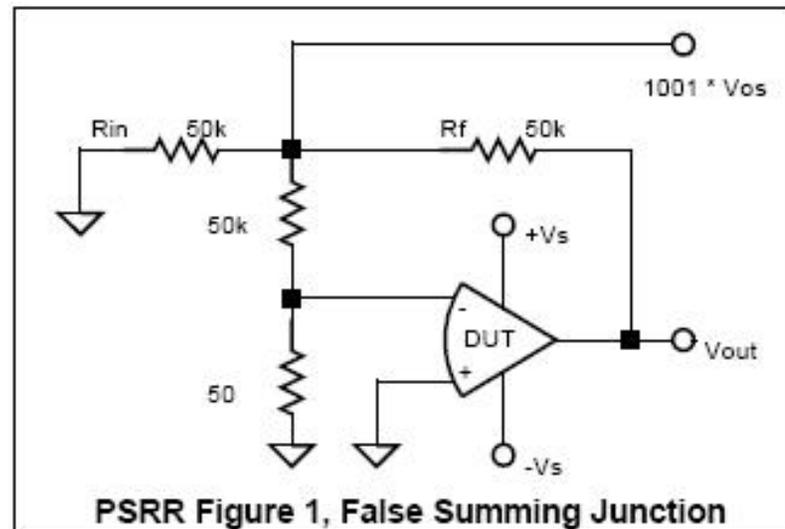# PSRR- Power Supply Rejections Ratio

Definition - the ratio of the absolute value of the change in the supply voltages divided by the change in the input offset voltage of the op amp. Simply it is Operational Amplifiers ability to reject changes in the power supply voltages over a specified range. Since the offset voltage is needed to make this measurement, the techniques already developed for measuring Vos can be used.

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PSRR- Power Supply Rejections Ratio

This test can be accomplished in all three test loop circuits by setting the power supplies, +Vs and -Vs to the minimum supply voltage for the DUT. Then measure 1001 * Vos. The supplies should then be programmed to the maximum voltage for the DUT. Then measure 1001*Vos again. Now we can calculate PSRR.

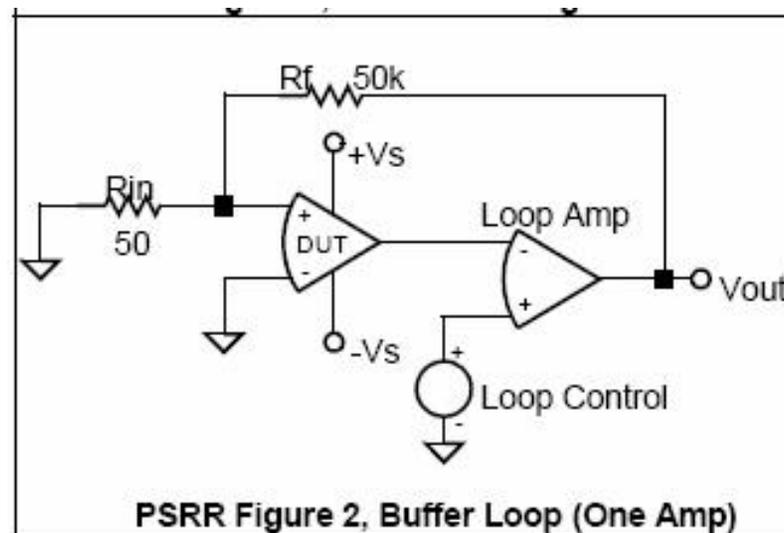PSRR Figure 1, False Summing Junction

Continued

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PSRR- Power Supply Rejections Ratio

Measuring PSRR with this method is the same as the self-test loop.

PSRR Figure 2, Buffer Loop (One Amp)

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PSRR- Power Supply Rejections Ratio

PSRR - Equations

$$PSRR = \frac{\Delta V_{Supply}}{\Delta V_{OS}}$$

$$PSRR(dB) = 20 \times \log\left(\frac{\Delta V_{Supply}}{\Delta V_{OS}}\right)$$
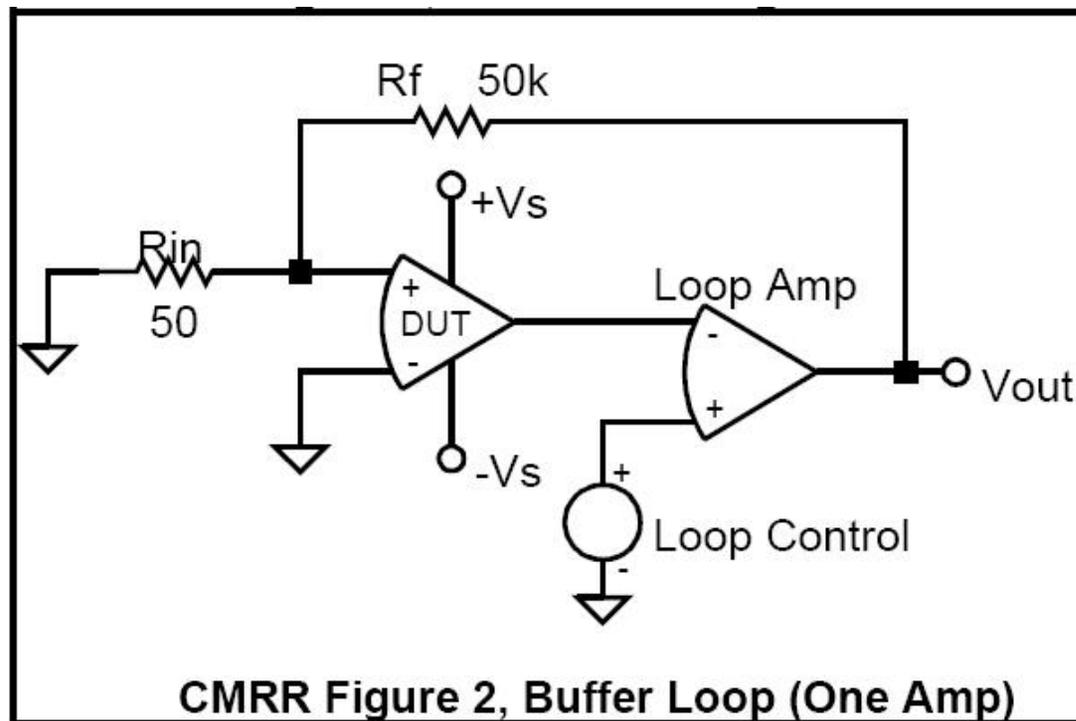
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CMRR- Common Mode Rejections Ratio

Definition - the ratio of the differential voltage gain to the common-mode voltage gain. It is the op amp's ability to reject common mode voltages over a specified range. Since the offset voltage is needed to make this measurement, the techniques already developed for measuring Vos can be used

CMRR Figure 1, False Summing Junction
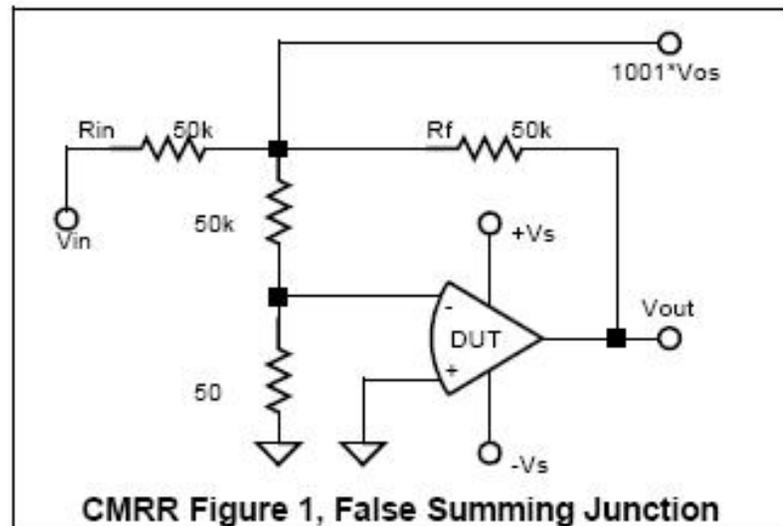
CMRR- Common Mode Rejections Ratio

The CMRR measurement with the two amp loop is made the same way as the self-test loop method.

CMRR Figure 2, Buffer Loop (One Amp)

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CMRR- Common Mode Rejections Ratio

CMRR - Equations

$$CMRR = \frac{\Delta V_{Input}}{\Delta V_{OS}}$$

$$CMRR(dB) = 20 \times \log\left(\frac{\Delta V_{Input}}{\Delta V_{OS}}\right)$$

Continued

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**a6**   It may be desirable to make all measurements with respect to ground. This can be accomplished by keeping the non-inverting input tied to ground, and moving the power supplies in a tracking fashion positively or negatively to apply effective common mode voltages to the amplifier. The output must be driven to the midpoint of the supplies to eliminate any Aol errors to corrupt the CMRR measurement using this technique.
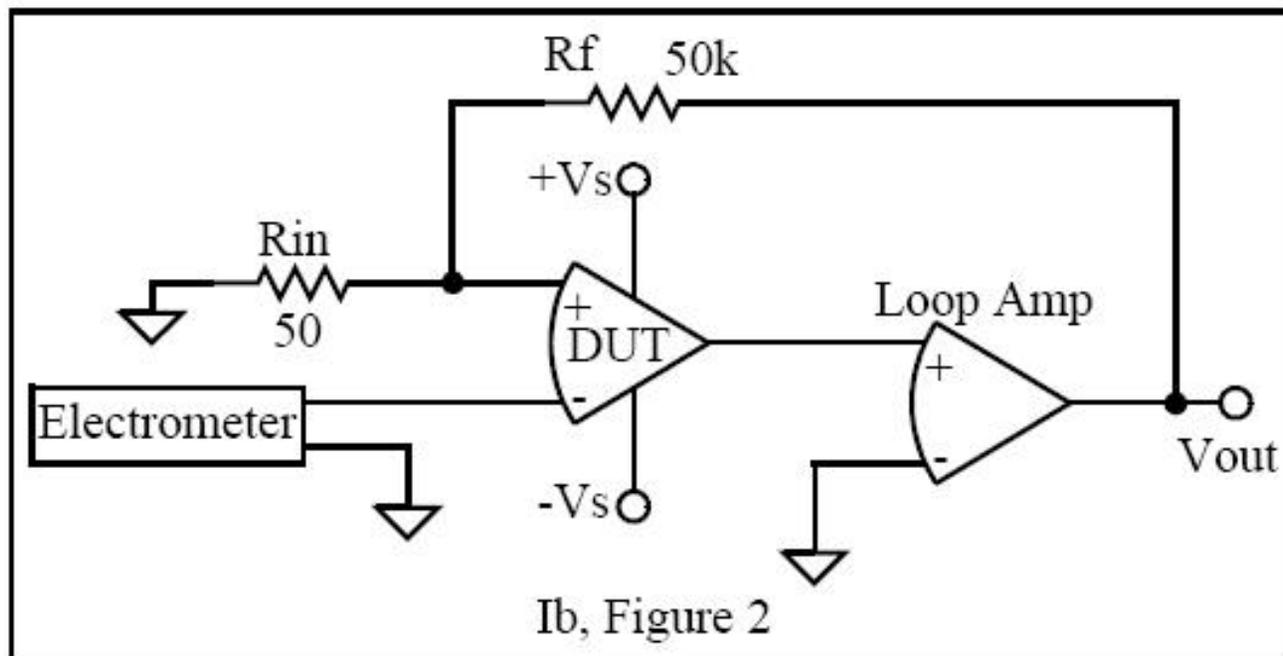a0873033, 4/11/2008

Ib+ Input Bias Current

An+ electrometer can be used in this configuration because the amplifier is stable.
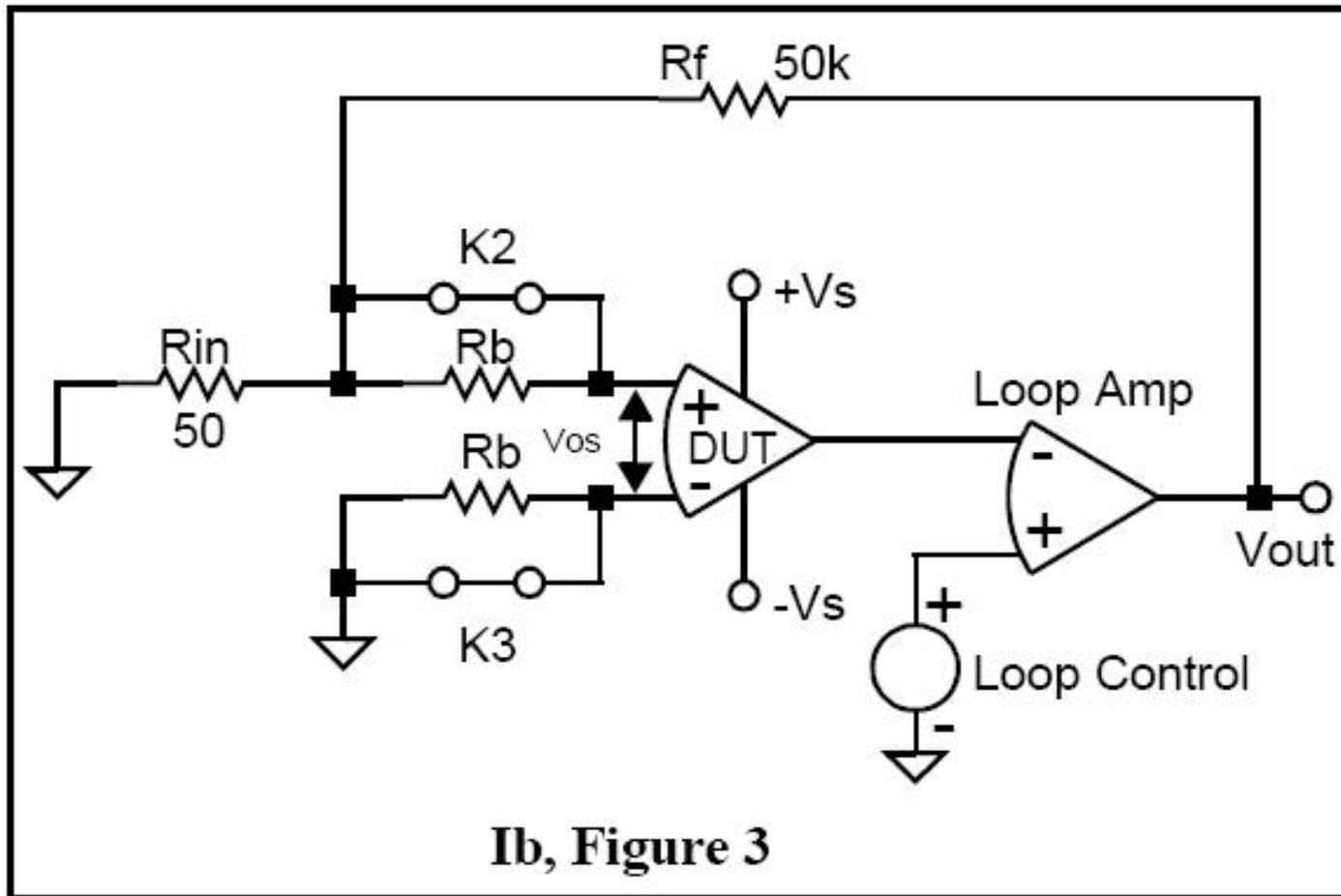

Ib, Figure 1
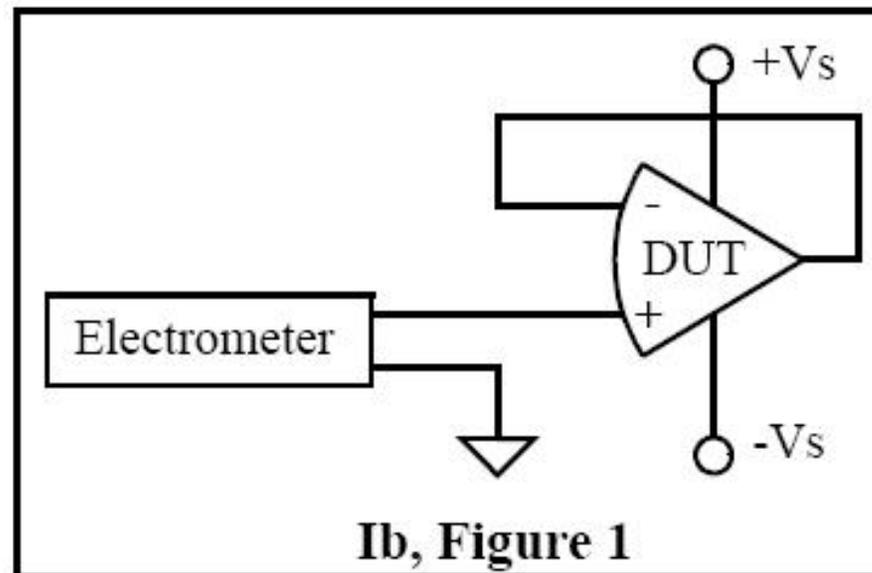
Ib- Input Bias Current

 Ib-, which is usually hard to measure, can be measured with an electrometer in this configuration because the loop amp keeps the DUT stable.

Ib, Figure 2

Ib - Input Bias Current

Ib, Figure 3

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Ib - Input Bias Current

For the Vos measurement

$$Vout = \left(\frac{R_{in} + R_f}{R_{in}}\right)V_{os}$$

$$\therefore V_{os} = \frac{Vout}{\left(\frac{R_{in} + R_f}{R_{in}}\right)}$$

Continued

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Ib - Input Bias Current

When the relay is opened, the Vos reading will be due to the Vos of the DUT plus R * Ib.

$$Vos(Ib) = Vos(Opamp) + (Ib \times Rb)$$

So the Vout that we measure is:

$$\therefore V_{out} = \left(\frac{R_{in} + R_f}{R_{in}}\right) \times (Vos(Opamp) + (Ib \times Rb))$$

We now solve for Ib:

$$\frac{V_{out}}{\left(\dfrac{R_{in} + R_f}{R_{in}}\right)} = (Vos(Opamp) + (Ib \times Rb))$$

Continued

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Ib - Input Bias Current

Rearrange some more:

$$\frac{V_{out}}{\left(\dfrac{R_{in}+R_f}{R_{in}}\right)}-Vos(Opamp) = Ib \times Rb$$
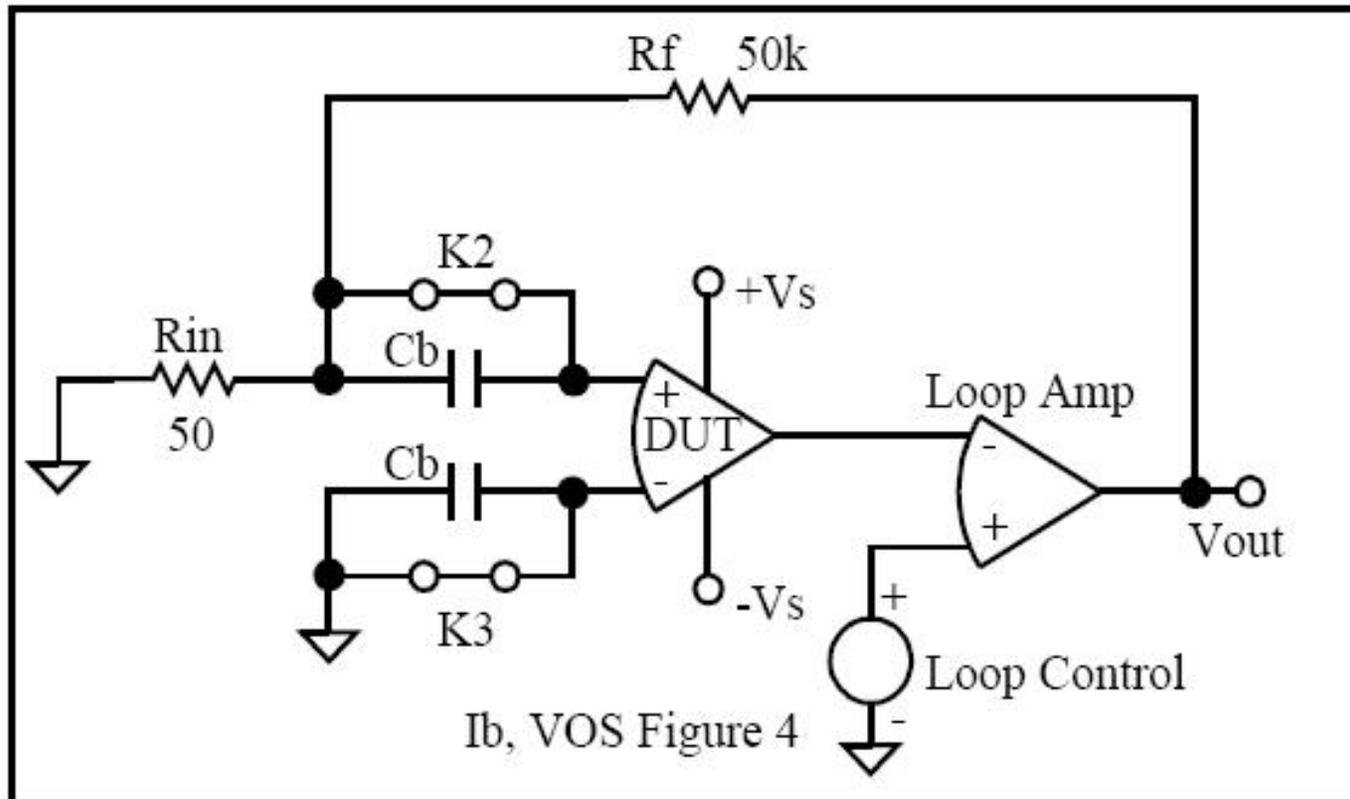
We then rearrange to get our final answer:

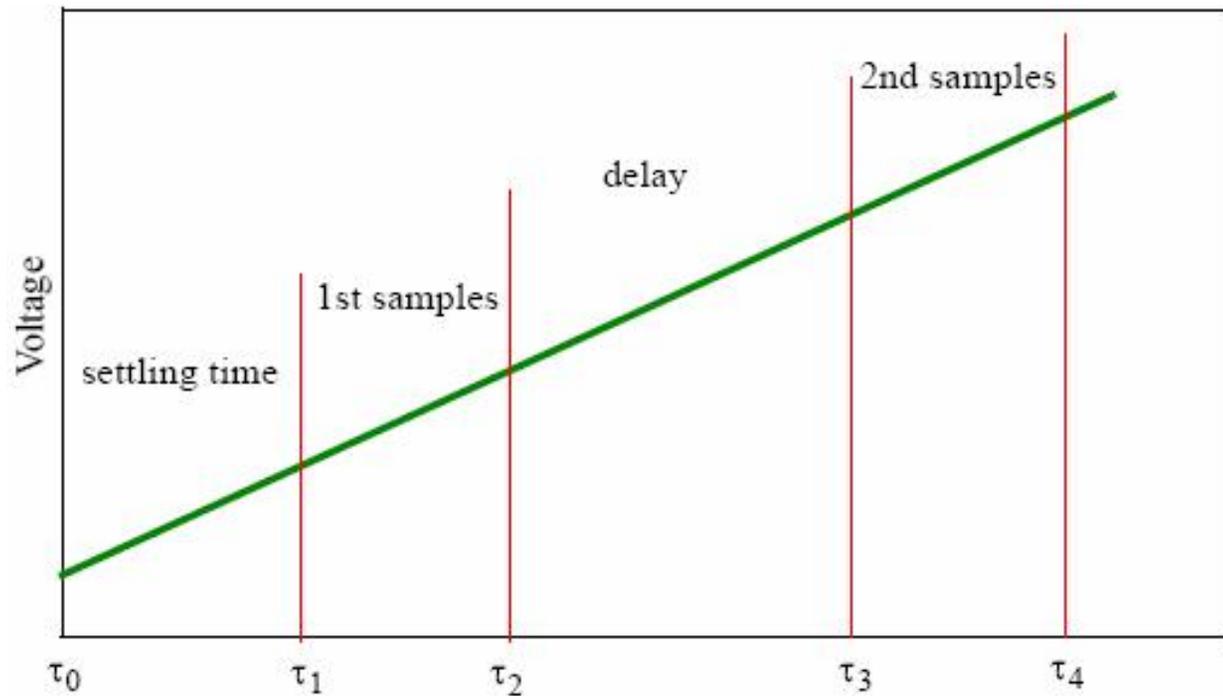$$Ib = \frac{\dfrac{V_{out}}{\left(\dfrac{R_{in}+R_f}{R_{in}}\right)}-Vos(Opamp)}{Rb}$$

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Ib - Input Bias Current

Ib, VOS Figure 4

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Ib - Input Bias Current
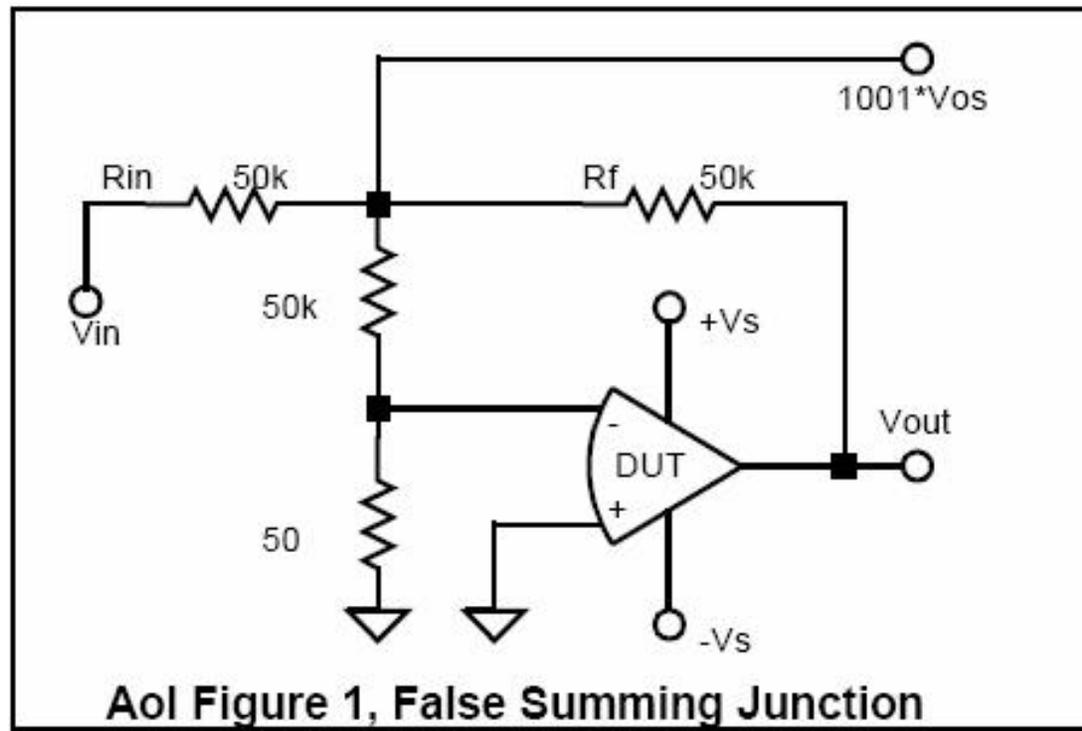

Ib, Figure 5

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Ib - Input Bias Current

$$i = C \times \frac{dv}{dt}$$

Bias current is then calculated by the following equation:

$$ib = Cb \times \frac{deltaV/loopGain}{\tau 1 - \tau 3}$$

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AoI – DC Open Loop Gain

Aol Figure 1, False Summing Junction

AoI – DC Open Loop Gain

Our method to measure AoI using Figure 1 is as follows:

1. Connect the appropriate load to the DUT (Rload)

2. Force Vin to set Vout(pos) to the PDS specification for positive swing.

3. Measure V(1) which is 1001 * (Vos + Vin(pos))

$$\therefore \text{Vin(pos)} = \left(\frac{V(1)}{1001}\right) - \text{Vos}$$

Continued

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AoI – DC Open Loop Gain

4. Then, force Vin to set Vout(neg) to the PDS specification for negative swing

5. Measure V(2) which is 1001 * (Vos + Vin(neg))

$$\therefore Vin(neg) = \left(\frac{V(2)}{1001}\right) - Vos$$

6. Calculate $Aol = 20 \times log\left(\frac{Vout(pos) - Vout(neg)}{Vin(pos) - Vin(neg)}\right)$

Continued

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Aol – DC Open Loop Gain

Substitute the values measured for Vin(pos) and Vin(neg).

$$Aol = 20 \times log\left(\frac{Vout(pos) - Vout(neg)}{\left(\frac{V(1)}{1001}\right)-Vos - \left(\left(\frac{V(2)}{1001}\right)-Vos\right)}\right)$$
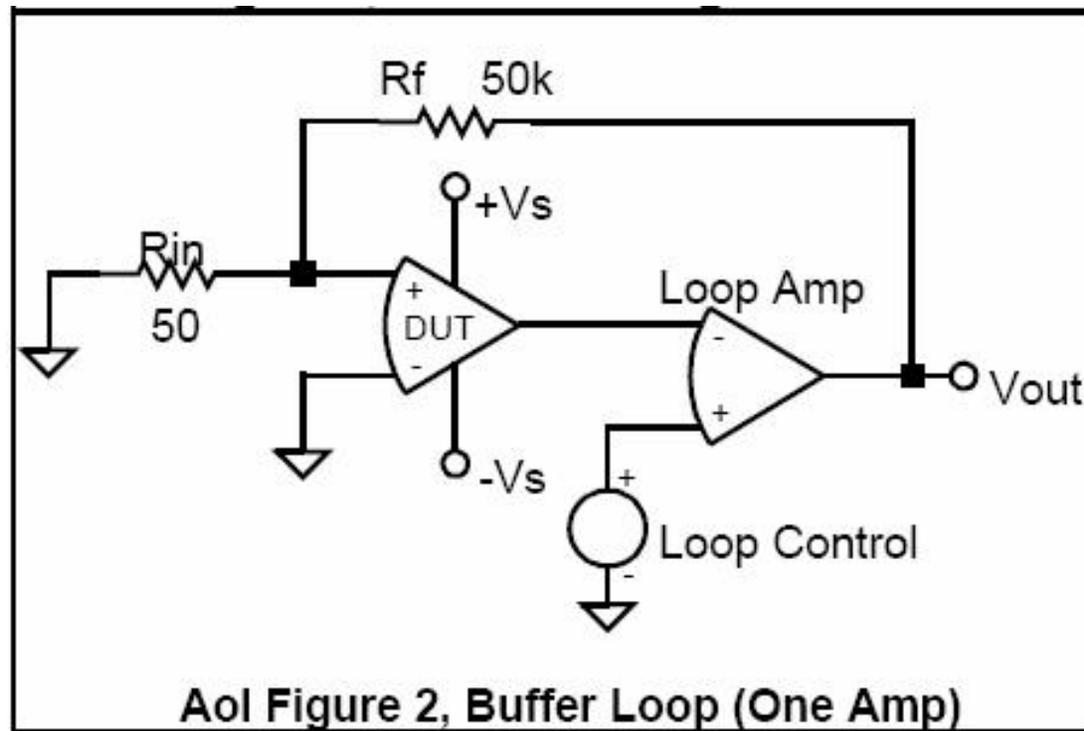
Notice that Vos drops out of the equation..

$$Aol = 20 \times log\left(\frac{Vout(pos) - Vout(neg)}{\left(\frac{V(1)}{1001}\right)-Vos - \left(\left(\frac{V(2)}{1001}\right)-Vos\right)}\right)$$

Continued

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AoI – DC Open Loop Gain
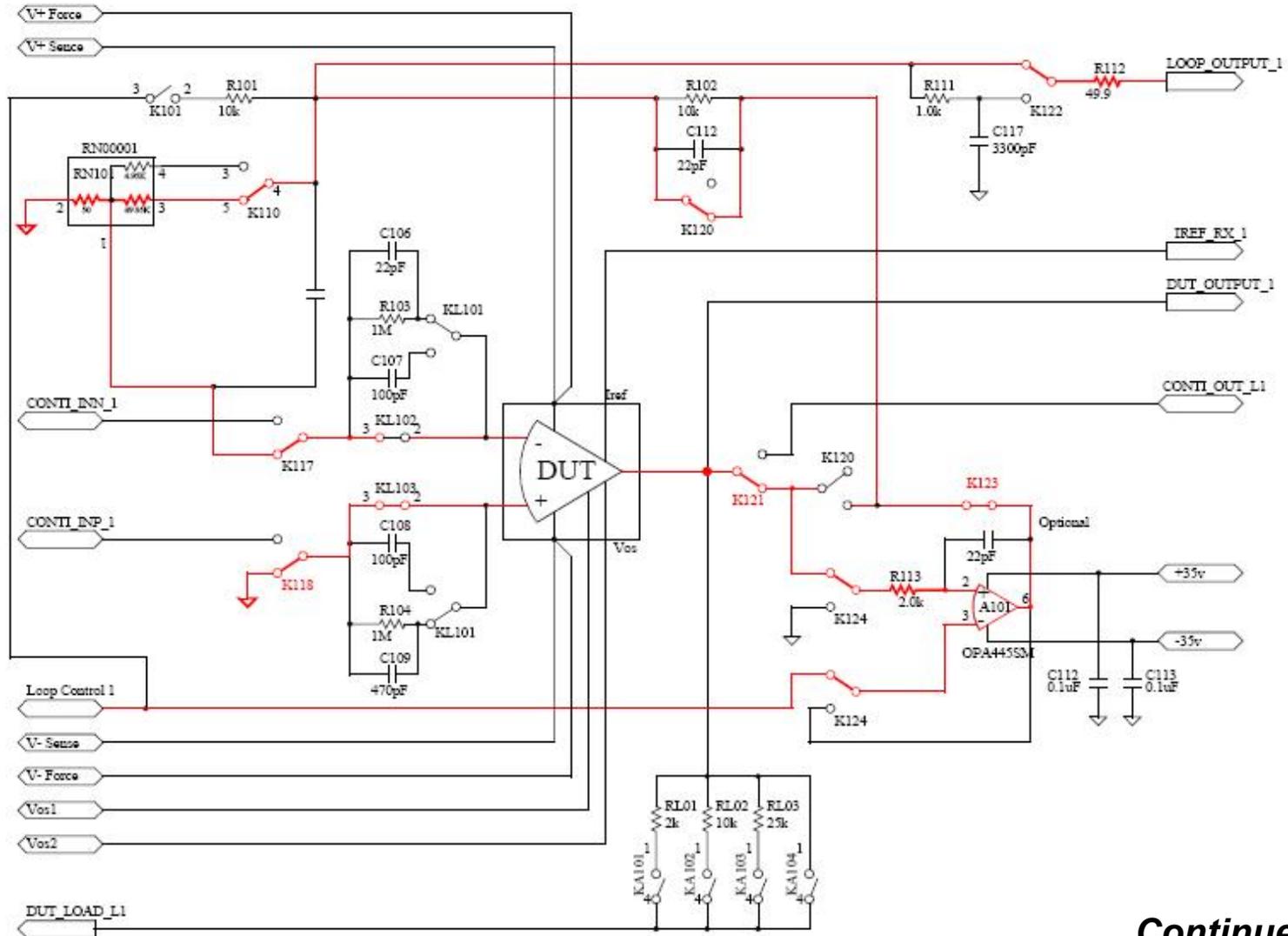

Aol Figure 2, Buffer Loop (One Amp)

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Putting it all together

The nice thing about the "Self-Test" method and the "Two Amp Loop" is that they can live together easily on the same test board.

- Advantages
  - Stability is never an issue
  - Both methods can be used on the same part
  - Comparison is easy.
- Disadvantage
  - Requires more board space / components
  - Requires more programming

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Putting it all together – Two Amp

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Putting it all together – Self Test

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Conclusions

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Method 1 - Self Test Circuit

- ## Advantages
  - – Simplicity of design
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- ## Disadvantages
  - – Can be slower
  - – Low Iq parts are difficult to test

Continued

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Method 2 – Two Amp Loop

- ## Advantages
  - Accurate control of DUT output voltage
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- ## Disadvantages
  - Stability – Compensation <u>must</u> be correct
  - Not useful for DUTs with variable gain/phase

Continued

TEXAS INSTRUMENTS

Method 3 – Three Amp Loop

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Continued

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