
CHAPTER 4

CIRCUIT SIMULATION

4.0 INTRODUCTION

Computer simulation of a circuit entails using a computer to predict, or simulate, the performance of a circuit or system. The circuit which is simulated may include anywhere from a few components to several hundred thousand. Many different types of computer programs are used for simulations of integrated circuits, depending on the type of analysis required and the size of circuit involved.

The major emphasis in this chapter is on the use of the SPICE simulation program for circuit simulation, and, in particular, on a discussion of the active device models used in SPICE and the interrelationship between these models and the device models discussed in Chapter 3. The simulation program SPICE was selected because of its long-term acceptance and use, as well as its widespread availability to both industrial and academic groups. The reader should have access to and be familiar with the SPICE User's Guide¹ and the basic use of SPICE.

In the design of state-of-the-art integrated circuits; circuit simulations comprise only a small portion of the overall use of the computer. The discussion of a circuit simulation program is included in this chapter because of the challenging nature of circuit simulation. Many students and even practicing engineers experience more problems with circuit simulation than with most of the other sophisticated CAD tools used for VLSI design. These problems largely result from unfamiliarity with the capabilities, limitations, and uses of the simulators.

4.1 CIRCUIT SIMULATION USING SPICE

The circuit simulation program called SPICE is the result of a continuing effort, which has spanned nearly 20 years, by a large group of individuals at the University of California at Berkeley. It was initially written in FORTRAN; later

versions in that language are nearly 18,000 lines long. A C-Language version of SPICE was practically introduced in 1987, and now both the FORTRAN and C versions are widely used. SPICE has been adapted to a large number of different hardware configurations and is used in both industry and academia. Although there are several competing programs, some of which may offer advantages in some respects, none are as universally accepted as SPICE.

SPICE utilizes a modified nodal analysis approach. It can be used for nonlinear-dc, nonlinear-transient, and linear-ac analysis problems. It also includes modules for more specialized analysis such as noise analysis, temperature analysis, etc. The inputs can be constant or time varying. For the nonlinear-dc and nonlinear-transient analyses, the program includes the nonlinear effects of all devices specified by the user. For the ac analysis, the dc operating point is internally determined. From the dc operating point, the small signal equivalent circuit of each device is obtained. The resulting linear network is analyzed using the appropriate matrix manipulations. The small signal analysis *includes no nonlinear effects* of the devices.

A block diagram showing the fundamental operation of SPICE appears in Fig. 4.1-1. The subroutine READIN reads the SPICE input file. ERRCHK verifies that the input syntax is correct. Temperature effects are handled in SPICE by repeating the entire analysis for each temperature. The subroutines DCTRAN, DCOP and ACAN perform the bulk of the manipulations. DCTRAN and DCOP are used for dc transfer characteristics, dc operating point calculations, and transient analysis. ACAN performs the small signal ac analysis.

Documentation about the program SPICE is required for utilizing the program. At a minimum, the IC designer needs the following two documents available from Berkeley to effectively use SPICE for MOS IC design.

1. "SPICE User's Guide"¹
2. "The Simulation of MOS Integrated Circuits Using SPICE"²

These publications, along with other relevant documentation^{3-12,22,23} are listed in the references. The SPICE source code⁶ contains good comments and serves as the ultimate reference document on the program.

One of the strong points of SPICE is its inclusion of respectable models for the basic active devices, specifically, the diode, BJT, JFET, and MOSFET. The user can create generic models for the active devices that correspond to, and are consistent with, the process parameters and design rules of the process used for a specific design. This model library may actually contain numerous generic device models for a given process, each of which contains as little or as much information as needed for the desired emphasis in the simulation. The designer can then use geometric parameters and specific model name references to specify the complete model for each active device in the circuit being analyzed.

To run SPICE¹, the user must first create a file, sometimes referred to as a SPICE deck, which contains a complete description of the circuit (including device models) along with a description of the excitation and the type of analysis desired. This file is accessed when the SPICE program runs.

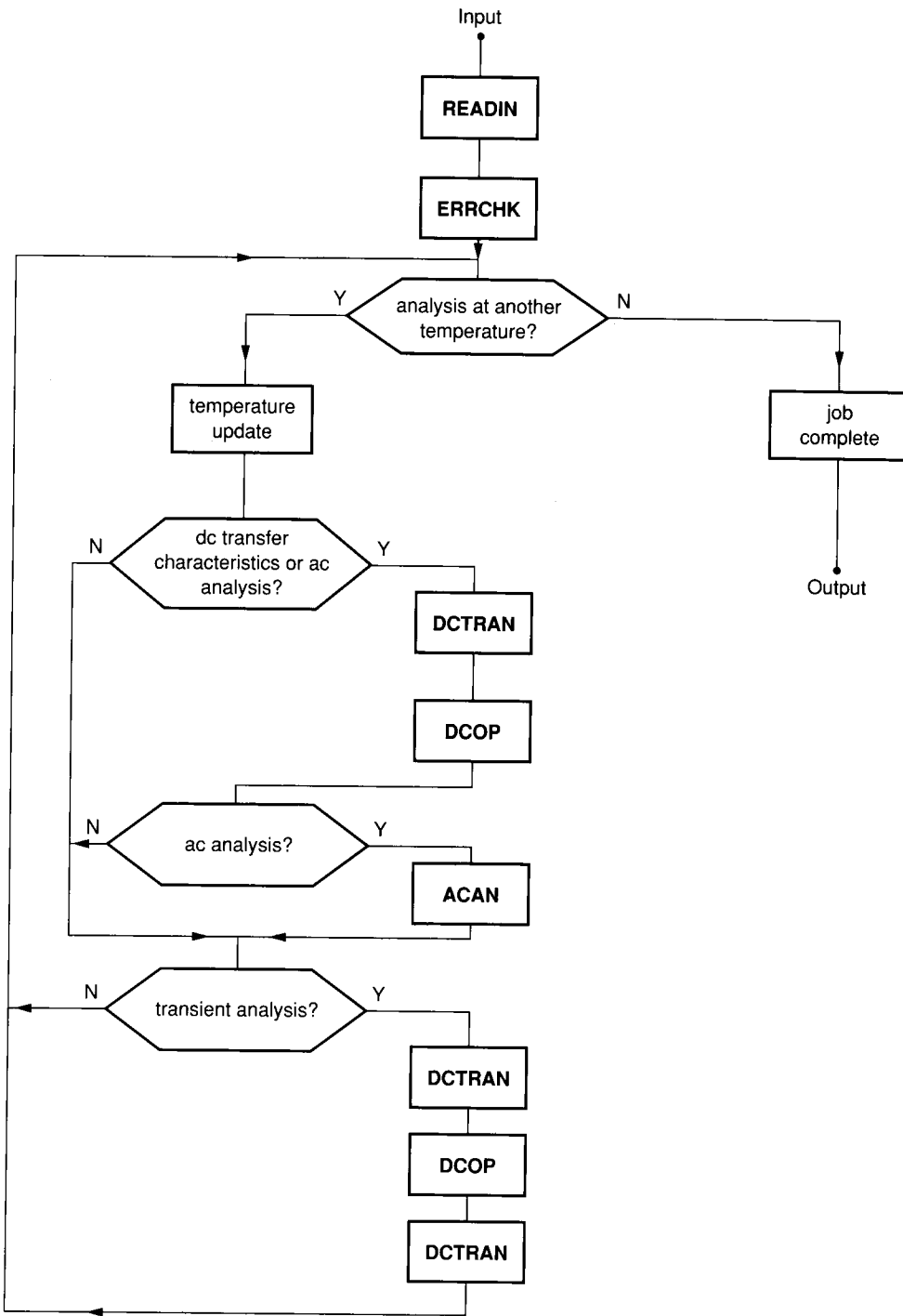


FIGURE 4.1-1
Simplified SPICE functional flowchart (boldface mnemonics indicate names of major subroutines).

The designer must be familiar with the device models used in any computer simulation. In the following sections the device models of the active devices used in SPICE are discussed. These models are related to those used for hand calculations that were introduced in Chapter 3. Each section is self-contained.

4.2 MOSFET MODEL

SPICE Version 2G has three different MOSFET models, designated as Level 1, Level 2, and Level 3. Version 3 of SPICE also contains a fourth MOSFET model, the BSIM model⁷⁻¹². The BSIM model is a process-oriented model which places a major emphasis on short channel devices. The discussion here will be restricted to the Level 1, Level 2, and Level 3 models. The Level 1 model is basically the same as introduced in Chapter 3 and is termed the Shichman-Hodges model; it closely follows the work of Sah¹³. The Level 1 model is the simplest model and is useful for verifying that no errors occurred in the hand calculations. In some applications the Level 1 model may be adequate for computer simulations.

The Level 2 model differs from the Level 1 model both in its method of calculating the effective channel length (λ effects) and the transition between the saturation and ohmic regions. A time-consuming polynomial rooting routine is required for the Level 2 model to determine the transition point between the linear and saturation regions. The Level 2 model offers improvements in performance which are particularly significant for short channel devices.

The Level 3 model is termed a semi-empirical model. Several empirical parameters (parameters not obviously related to or motivated by the device physics of the MOSFET) are introduced in the Level 3 model. These parameters may offer improvements in fit of the model. The Level 3 model also offers a reduction in time required to calculate the transition point between the linear and saturation regions of operation.

The Level 1, Level 2, and Level 3 device models can be found respectively in subroutines MOSEQ1, MOSEQ2, and MOSEQ3 of the SPICE source code. Subroutine MODCHK is used for some of the hierarchical parameter definitions. The terminal voltages of the MOSFET are passed to these subroutines, and the nodal currents are returned along with the small signal model parameters at the operating point. In each interval of time in a transient analysis, nodal currents are comprised of two parts. The first is the dc current obtainable from the large signal device model. The second is the charge current associated with the parasitic capacitances in the devices. This latter current plays a major role in high-frequency transient analyses.

Temperature effects can also be modeled in SPICE. The functional form of the temperature-dependent device parameters will be discussed later.

Individual MOSFETS are modeled by a two-step process in SPICE. The device element line (card) in the SPICE deck contains information about the nodal location of the device in the circuit as well as geometrical information about the device and optional initial condition variables. In the device element line, reference is made to a specific device *model*. The .MODEL line (card) in the SPICE deck contains generic information about the electrical characteristics

of devices formed in a process based upon the characterizing process parameters. Each device has a separate device element line. Typically, many devices will reference a single .MODEL line.

A simplified flowchart of MOSEQ1, MOSEQ2 and MOSEQ3 is shown in Figure 4.2-1. The large signal currents in Quadrant 1 of the $I_D - V_{DS}$ plane are calculated from the expression:

$$I_G = I_B = 0 \quad (4.2-1)$$

$$I_D = \begin{cases} I_{\text{CUTOFF}} & V_{GS} < V_{TH} \\ I_{\text{OHMIC}} & V_{GS} > V_{TH} \quad V_{DS} < V_{DSAT} \\ I_{\text{SAT}} & V_{GS} > V_{TH} \quad V_{DS} > V_{DSAT} \end{cases} \quad (4.2-2)$$

$$I_D = \begin{cases} I_{\text{OHMIC}} & V_{GS} > V_{TH} \quad V_{DS} < V_{DSAT} \\ I_{\text{SAT}} & V_{GS} > V_{TH} \quad V_{DS} > V_{DSAT} \end{cases} \quad (4.2-3)$$

$$I_D = \begin{cases} I_{\text{SAT}} & V_{GS} > V_{TH} \quad V_{DS} > V_{DSAT} \end{cases} \quad (4.2-4)$$

where it is assumed that the drain and source are designated so that $V_{DS} \geq 0$. The parameter V_{TH} denotes the threshold voltage which was denoted by V_T in Chapter 3. V_{DSAT} is a parameter that characterizes the transition between the ohmic and saturation regions. Operation in Quadrant 3 of the $I_D - V_{DS}$ plane is characterized by the same equations, where the drain and source designations are internally made so that $V_{DS} \geq 0$.

The small signal parameters are calculated from the derivatives of I_D with respect to V_{GS} , V_{DS} , and V_{BS} as explained in Sec. 3.1. In what follows, the expressions used for I_D for the Level 1 and Level 2 models are given along with a description of each of the parameters that appear in the model; the default values used in SPICE are given if the parameter is not specified. The parameters are summarized in Appendix 4A.

Some parameters in the model may be specified in more than one way. For example, the transconductance parameter K' , introduced in Sec. 3.1, may be entered directly or calculated from the expression $K' = \mu_0 C_{ox}$. A hierarchical convention has been adopted in SPICE to avoid ambiguity. If a parameter is specified, that value will be used. If a parameter is not specified but can be calculated from other parameters that are specified (or have a nonzero default value), the calculated value will be used. If a parameter is not specified and at least one of the other parameters which can be used to calculate it is not specified and defaults to zero, the default value of the original parameter is adopted. A summary of the Level 1 and Level 2 large signal models follows. The parameters used in these models are defined in the Appendices of this chapter.

4.2.1 Level 1 Large Signal Model

$$I_{\text{CUTOFF}} = 0 \quad (4.2-5)$$

$$I_{\text{OHMIC}} = K' \frac{W}{L_{\text{eff}}} \left([V_{GS} - V_{TH}] - \frac{V_{DS}}{2} \right) V_{DS} \quad (4.2-6)$$

$$I_{\text{SAT}} = \frac{K'}{2} \frac{W}{L_{\text{eff}}} (V_{GS} - V_{TH})^2 \quad (4.2-7)$$

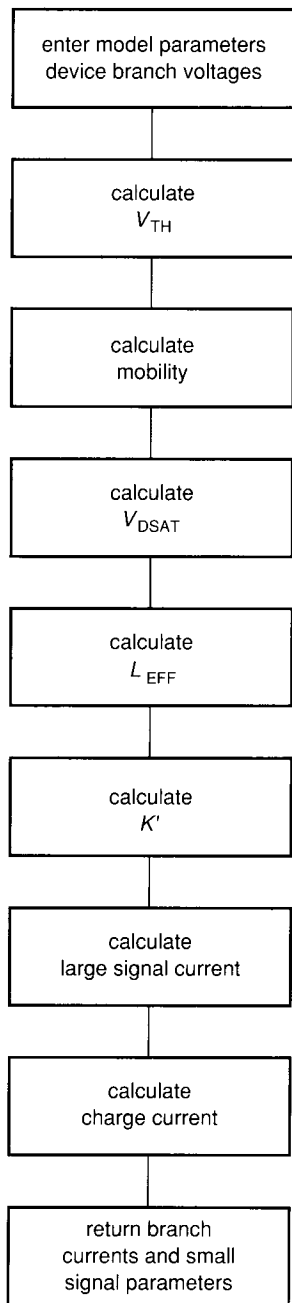


FIGURE 4.2-1 Simplified Flowchart of SPICE Subroutines MOSEQ1, MOSEQ2, and MOSEQ3.

where V_{DSAT} is given by

$$V_{DSAT} = V_{GS} - V_{TH} \quad (4.2-8)$$

and the regions of operation are as defined in Eqs. 4.2-1 – 4.2-4.

The parameters V_{TH} and L_{eff} represent the threshold voltage and effective length of the device, respectively, and are given by

$$V_{TH} = V_{T0} + \gamma \left[\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right] \quad (4.2-9)$$

and

$$L_{eff} = \frac{L_{adj}}{1 + \lambda V_{DS}} \quad (4.2-10)$$

where V_{T0} is the zero bias threshold voltage, γ is the bulk threshold parameter, ϕ is the surface potential, and λ is the channel length modulation parameter. λ is a SPICE input parameter. V_{T0} , γ , and ϕ can either be entered directly or be internally calculated, as discussed later. The parameter K' , if not entered, can be calculated from the expression

$$K' = \mu_0 C_{ox} \quad (4.2-11)$$

where μ_0 is the nominal channel mobility (if μ_0 is not entered, the default value will be used) and C_{ox} is the gate oxide capacitance density which can be calculated from the gate oxide thickness, T_{ox} , by the expression

$$C_{ox} = \epsilon_{ox} / T_{ox} \quad (4.2-12)$$

where ϵ_{ox} is the dielectric constant of SiO_2 . The parameter L_{adj} represents the adjusted length which is the drawn length reduced by the lateral diffusion on the drain and source, LD .

$$L_{adj} = L - 2 \times LD \quad (4.2-13)$$

The parameters in V_{TH} , if not input, are calculated from

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_{SUB}}}{C_{ox}} \quad (4.2-14)$$

$$\phi = \frac{2kT}{q} \ln \left(\frac{N_{SUB}}{n_i} \right) \quad (4.2-15)$$

and

$$V_{T0} = V_{FB} + \gamma\sqrt{\phi} + \phi \quad (4.2-16)$$

where ϵ_{si} is the dielectric constant of silicon, N_{SUB} is the substrate doping, q is the charge of an electron, and n_i is the intrinsic carrier concentration of silicon. N_{SUB} is a SPICE input parameter and n_i and ϵ_{si} are physical constants defined in Appendix 4A. The flatband voltage, V_{FB} , is given by

$$V_{FB} = \phi_{ms} - \frac{qN_{ss}}{C_{ox}} \quad (4.2-17)$$

where the input parameter, N_{ss} , is the effective surface state density and ϕ_{ms} is the semiconductor work function difference. ϕ_{ms} is calculated internally from

$$\phi_{ms} = W_{FN} - \frac{\phi}{2} \tag{4.2-18}$$

where the parameter W_{FN} is an internal function of physical constants characteristic of the materials involved, TPG (which specifies the types of materials used to construct the device), and temperature.

4.2.2 Level 2 Large Signal Model†

$$I_{CUTOFF} = \begin{cases} 0 & \text{NFS} = 0 \\ I_{\text{weak inversion}} & \text{NFS} \neq 0 \end{cases} \tag{4.2-19}$$

$$I_{OHMIC} = \frac{K'_2 W}{L_{eff}} \left[\left(V_{GS} - V_{TH}^* - \eta \frac{V_{DS}}{2} \right) V_{DS} \right] + I_{BSO} \tag{4.2-20}$$

$$I_{SAT} = \frac{K'_2 W}{2L_{eff}} \left[(V_{GS} - V_{TH}^*)^2 (2 - \eta) \right] + I_{BSS} \tag{4.2-21}$$

where the cutoff transition region is determined by

$$V_{TH} = V_{T0} + \gamma \left[\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right] - \gamma \alpha \sqrt{\phi - V_{BS}} + (\phi - V_{BS}) \frac{\pi}{4} \frac{\epsilon_{si}}{C_{ox} L_{adj}} (\text{DELTA}) \tag{4.2-22}$$

The parameter L_{adj} is defined by (4.2-13). The parameters DELTA and α will be discussed later.

The parameter V_{MAX} is used to characterize the saturation/ohmic transition region as specified in (4.2-3) and (4.2-4); it denotes the maximum drift velocity of carriers in the channel. If the parameter V_{MAX} is not input, the saturation/ohmic transition region is determined by

$$V_{DSAT} = \frac{(V_{GS} - V_{TH}^*)}{\eta} + \frac{1}{2} \left[\frac{\gamma_s}{\eta} \right]^2 \cdot \left\{ 1 - \left[1 + 4 \left(\frac{\gamma}{\eta} (1 - \alpha) \right)^{-2} \left(\frac{V_{GS} - V_{TH}^*}{\eta} + \phi - V_{BS} \right) \right]^{\frac{1}{2}} \right\} \tag{4.2-23}$$

If V_{MAX} is input, V_{DSAT} is obtained from solution of a complicated fourth-order polynomial. V_{MAX} essentially reduces the value of V_{DSAT} and hence the saturation current in a manner more consistent with experimental measurements. If

†See SPICE source code for the SPICE Model of the MOSFET in weak inversion. The accuracy of the weak inversion MOSFET Models has been questioned by some individuals. 14-15

V_{MAX} is input, computational time for calculating V_{DSAT} does increase. Additional details about V_{MAX} can be found in the paper by Vladimerescu and Liu.²

The parameters η , V_{TH}^* , I_{BSO} and I_{BSS} are given by the following equations:

$$\eta = 1 + \frac{\pi}{4} \frac{\epsilon_{si}}{C_{ox} L_{adj}} (\text{DELTA}) \quad (4.2-24)$$

$$V_{TH}^* = V_{T0} - \gamma \sqrt{\phi} + (\phi - V_{BS}) \frac{\pi}{4} \frac{\epsilon_{si}}{C_{ox} L_{adj}} (\text{DELTA}) \quad (4.2-25)$$

$$I_{BSO} = -\frac{2 K_2' W}{3 L_{eff}} \frac{\gamma_s}{\eta} \left[(\phi + V_{DS} - V_{BS})^{\frac{3}{2}} - (\phi - V_{BS})^{\frac{3}{2}} \right] \quad (4.2-26)$$

$$I_{BSS} = \frac{K_2' W}{L_{eff}} \left[\left[(V_{GS} - V_{TH}^*) (1 - \eta) - \frac{\eta}{2} (V_{DSAT} - (V_{GS} - V_{TH}^*)) \right] \right. \\ \left. (V_{DSAT} - (V_{GS} - V_{TH}^*)) - \frac{2 \gamma_s}{3 \eta} \left[(V_{DSAT} - V_{BS} + \phi)^{\frac{3}{2}} - (\phi - V_{BS})^{\frac{3}{2}} \right] \right] \quad (4.2-27)$$

The parameter K_2' is obtained from the expression

$$K_2' = K' \frac{\mu_s}{\mu_o} \quad (4.2-28)$$

where μ_s is the effective surface mobility. If not input, K' is determined from (4.2-11). The parameter DELTA is a SPICE input parameter and is used to characterize width reduction (see Problem 4.17) where the effective width, W_{eff} , is given by $W_{eff} = W(2 - \eta)$.

The parameters V_{T0} , L_{adj} , and ϕ are determined as for the Level 1 model. The parameter γ_s is given by

$$\gamma_s = \gamma(1 - \alpha) \quad (4.2-29)$$

The parameter α is given by:

$$\alpha = \frac{1}{2} \frac{XJ}{L_{adj}} \left[\sqrt{1 + \frac{2W_S}{XJ}} + \sqrt{1 + \frac{2W_D}{XJ}} - 2 \right] \quad (4.2-30)$$

where

$$W_S = X_D \sqrt{\phi - V_{BS}} \quad (4.2-31)$$

$$W_D = X_D \sqrt{\phi - V_{BS} + V_{DS}} \quad (4.2-32)$$

and where XJ is a SPICE input parameter representing the metallurgical junction depth.

The parameter L_{eff} is defined by the expression

$$L_{eff} = L_{adj}(1 - \lambda V_{DS}) \quad (4.2-33)$$

If not specified as an input parameter, λ is calculated from the expression

$$\lambda = \frac{X_D}{L_{adj} V_{DS}} \left[\sqrt{\left(\frac{X_D V_{MAX}}{2\mu_s} \right)^2 + (V_{DS} - V_{DSAT})} - \frac{X_D V_{MAX}}{2\mu_s} \right] \quad (4.2-34)$$

The parameter X_D is given by the expression

$$X_D = \sqrt{\frac{2\epsilon_{si}}{qN_{SUB}}} \quad (4.2-35)$$

The effective surface mobility, μ_s , is given by

$$\mu_s = \begin{cases} \mu_0 \left[\frac{UCRIT \cdot \epsilon_{si}}{C_{ox}(V_{GS} - V_{TH})} \right]^{UEXP} & \text{for Level 1} \\ \mu_0 \left[\frac{UCRIT \cdot \epsilon_{si}}{C_{ox}(V_{GS} - V_{TH} - UTRA \cdot V_{DS})} \right]^{UEXP} & \text{for Level 3} \end{cases} \quad (4.2-36)$$

The parameters UCRIT, UTRA and UEXP are SPICE input parameters used to characterize mobility degradation.

4.2.3 High-Frequency MOSFET Model

The high-frequency MOSFET model is obtained from the dc model by adding the identifiable parasitic capacitances to the dc model previously discussed. Parasitic device capacitors in SPICE are essentially modeled as in Section 3.1.3 of Chapter 3. Those capacitors that are voltage independent are modeled by

$$C = \frac{\epsilon A}{t} \quad (4.2-37)$$

where ϵ is the dielectric constant (permittivity), A is the area of the intersection of the two plates and t is the dielectric thickness. The voltage independent capacitors are comprised of those that are operation-region dependent and those that are not.

The operation-region independent capacitors are comprised of those overlap capacitors that appear on the periphery of the MOSFET. A top view of these parasitic capacitors appears in Fig. 4.2-2. All are essentially rectangular in shape.

The effective area of the overlap component of the gate-source capacitance is $W \cdot LD$ where W is the channel width and LD is the lateral diffusion of the source. From (4.2-37) the gate-source overlap capacitor, C_{GSOL} , can be expressed as

$$C_{GSOL} = \frac{\epsilon LD \cdot W}{t} \quad (4.2-38)$$

$$\lambda = \frac{X_D}{L_{adj} V_{DS}} \left[\frac{V_{DS} - V_{DSAT}}{4} + \left\{ 1 + \left(\frac{V_{DS} - V_{DSAT}}{4} \right)^2 \right\}^{1/2} \right]$$

missing V_{MAX} notation

in (4.2-34) parameter X_D is given by $X_D = \sqrt{\frac{2\epsilon_{si}}{qN_{SUB}}}$ for Level 1

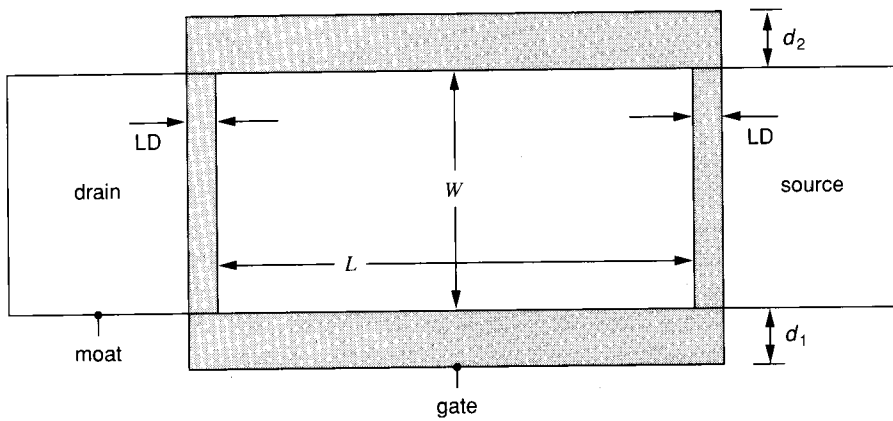


FIGURE 4.2-2

Top view of operation-region independent, or overlap (shaded) capacitors, in MOS transistors.

or

$$C_{GSOL} = C_{GSO}W \quad (4.2-39)$$

where $C_{GSO} = \epsilon LD/t$ represents the overlap capacitance per unit width of the gate. C_{GSO} serves as an input parameter in SPICE to model the overlap capacitance. Since the dielectric thickness is the same as the gate oxide thickness, this parasitic has an area capacitance density of C_{ox} . If C_{GSO} is not entered in SPICE, C_{GSOL} is calculated from

$$C_{GSOL} = (C_{ox})(LD)W \quad (4.2-40)$$

where C_{ox} is calculated via either the entered or defaulted value of the gate oxide thickness, T_{ox} . The gate-drain overlap capacitance is modeled in the same manner.

From Fig. 4.2-2, it follows that the gate-bulk overlap capacitance is linearly proportional to L and dependent upon d_1 and d_2 . The dielectric thickness, however, is not constant for this parasitic. The dielectric thickness of the gate-bulk overlap is essentially equal to the gate oxide thickness on the sides adjacent to the channel and equal to the height of the field oxide on the sides farthest from the channel. Although it cannot be modeled by (4.2-37), it is voltage independent. Since it is proportional to L , it is modeled by

$$C_{GBOL} = C_{GBO}L \quad (4.2-41)$$

where C_{GBO} represents the total gate-bulk capacitance per unit length of the device. C_{GBO} serves as an input parameter in SPICE to characterize the gate-bulk overlap. Since field oxide thickness is not considered in the MOSFET model, and since d_1 and d_2 are layout dependent, the C_{GBO} parameter must be entered if the effects of gate-bulk overlap are to be included in the model. It is common practice to assume that $d_1 = d_2 = d$ where d is the minimum overlap of the poly over the moat. With this assumption, any bulk-substrate capacitance associated with a larger gate polysilicon region is accounted for by adding an additional parasitic capacitance to the circuit schematic from gate to substrate.

Those capacitors that are voltage dependent are the pn junction capacitors. They occur between bulk and source, bulk and drain, and bulk and channel. They are modeled as in Chapter 3 by

$$C = \frac{C_{j0}A}{(1 - V_F/\phi_B)^n} \quad \text{for } V_F < FC \cdot \phi_B \quad (4.2-42)$$

where C_{j0} is the zero-bias junction capacitance density. FC is called the forward bias capacitance coefficient ($FC \approx .5$) which defines the region where (4.2-42) is valid, ϕ_B is the barrier potential, n is a constant that characterizes the junction type, A is the junction cross-sectional area, and V_F is the forward bias on the junction (which is usually negative for MOS devices). The modeling of the junction capacitors is complicated somewhat by the actual geometry of the pn junction. A cross section of a pn diffused junction is shown in Fig. 4.2-3. The junction is not planar. The impurity concentrations in the p and n type materials at the bottom of the junctions are different than the concentrations along the sidewalls causing the grading coefficient, n , to vary as a function of position. Although the sidewall capacitances become negligible for large structures, they may actually dominate for small or narrow junctions. The total junction capacitance associated with the "reverse biased" (actually for $V_F < FC \cdot \phi_B$) junction of either the source or drain is thus

$$C_{RB, \text{TOTAL}} = \frac{CJ \cdot A}{[1 - (V_F/\phi_B)]^{MJ}} + \frac{CJSW \cdot P}{[1 - (V_F/\phi_B)]^{MJSW}} \quad (4.2-43)$$

where CJ is the zero-bias bottom capacitance area density, $CJSW$ is the zero-bias sidewall capacitance per unit length of the perimeter, MJ is the bottom junction

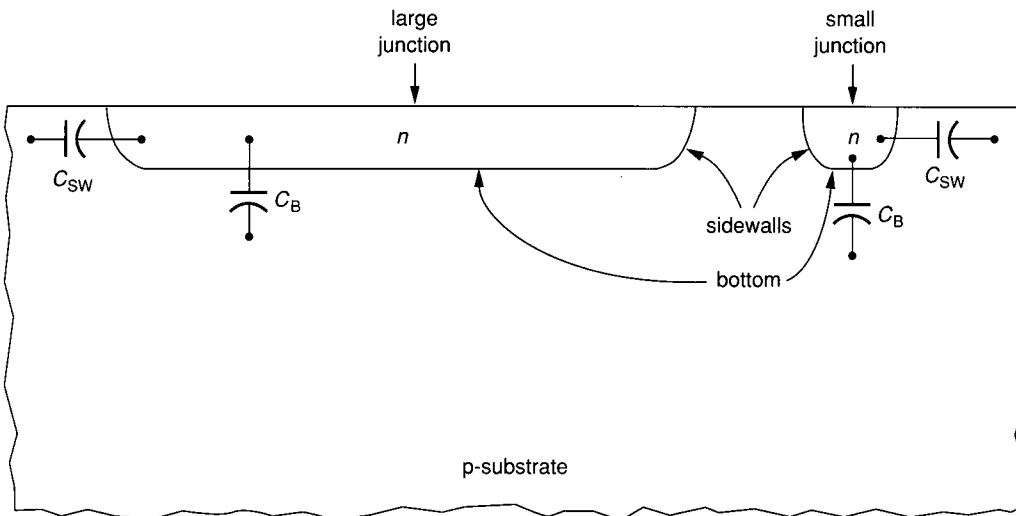


FIGURE 4.2-3 Cross section of diffused region showing parasitic junction capacitors.

grading coefficient, FC is the forward bias coefficient (which defines the region where (4.2-43) remains valid), and MJSW is the sidewall grading coefficient. A is the junction bottom area and P is the junction sidewall perimeter. The parameters FC, CJ, CJSW, MJ, MJSW and ϕ_B can be entered in SPICE on the .MODEL card (line). The parameters A and P for the drain and source junctions must be entered on the device card (line). If not input, CJ is calculated internally from N_{SUB} (if input), under the assumption of a step graded junction, from the expression

$$CJ = \sqrt{\frac{\epsilon_{si} q N_{SUB}}{2\phi_B}} \quad (4.2-44)$$

As an alternative to specifying the drain and source geometries and the junction capacitance density, the user can specify the overriding parameters C_{BD} and C_{BS} which represent the total zero-bias bottom capacitance of the bulk-drain and bulk-source junctions, respectively. These are then used in place of $CJ \cdot A$ in (4.2-43).

Under forward bias ($V_F > FC \cdot \phi_B$), the total junction capacitances are modeled by

$$C_{FB, TOTAL} = \frac{CJ \cdot A}{(1 - FC)(1 + MJ)} \left[1 - FC(1 + MJ) + \frac{V_{BS}}{\phi_B} MJ \right] \\ + \frac{CJSW \cdot P}{(1 - FC)(1 + MJSW)} \left[1 - FC(1 + MJSW) + \frac{V_{BS}}{\phi_B} MJSW \right] \quad (4.2-46)$$

This approximation represents a linear continuation of the reverse-bias capacitance which agrees functionally and in the first derivative at the transition point, $V_F = FC \cdot \phi_B$ (see Problem 3.31 of Chapter 3).

Finally, the operation-region dependent capacitances associated with the channel region itself must be considered. These are essentially distributed capacitances; as such they are more difficult to model. Furthermore, to ease calculations these parasitics are subsequently lumped internally and added to the operation-region independent components of the gate-source, gate-drain, gate-bulk, source-bulk, and drain-bulk capacitors discussed previously. Depending on the operating region, some of the channel capacitances are voltage independent and are modeled by (4.2-37), while others are actually junction capacitances modeled by (4.2-42). The user need not enter any additional parameters; the parasitic channel capacitances are calculated internally from the parameters that characterize the operation-region independent capacitors discussed above. The user is, however, at the mercy of the approximations employed in SPICE to model the channel capacitances. Some industrial groups are not satisfied with the channel capacitance modeling in SPICE and have made modifications which they believe offer some improvements. The exact formulation of the channel capacitances is quite involved and beyond the scope of this text. Details can be found in references 16 and 17, as well as in the SPICE source code itself⁶. The total parasitic capacitances (fixed plus voltage dependent) associated with the lumped approximation used in SPICE are basically as indicated in Fig. 4.2-4.

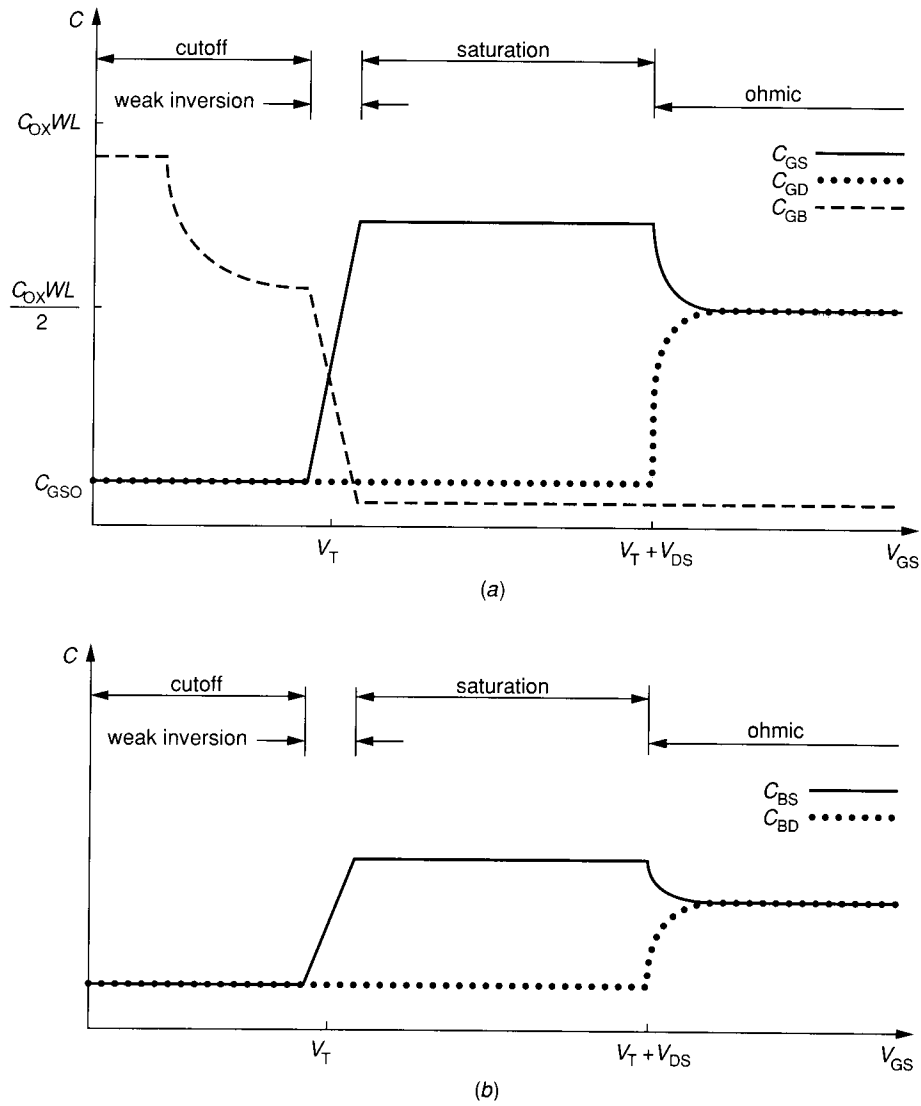


FIGURE 4.2-4 Lumped parasitic capacitances for MOSFET as a function of operating point: (a) Associated with gate charge, (b) Associated with bulk charge.

4.2.4 Noise Model of the MOSFET

There are four noise-current generators modeled in the MOSFET device model in SPICE.¹⁸ Two of these represent thermal noise associated with the parasitic series resistances in the drain and source. These are modeled by spectral densities of

$$S_{\text{IRD}} = \frac{4kT}{\text{RD}} \quad (4.2-47)$$

and

$$S_{\text{IRS}} = \frac{4kT}{\text{RS}} \quad (4.2-48)$$

respectively, where k is Boltzmann's constant, T is the temperature in °K, and RD and RS represent the drain and source parasitic resistances.

The other two noise-current generators are modeled as current sources from drain to source. One represents white shot noise and the other flicker ($1/f$) noise. These are characterized in the saturation region by spectral densities of¹

$$S_{\text{W}} = \frac{8kTg_{\text{m}}}{3} \quad (4.2-49)$$

and

$$S_{\text{f}} = \frac{(K_{\text{F}})I_{\text{DQ}}^{A_{\text{F}}}}{fC_{\text{ox}}WL_{\text{eff}}} \quad (4.2-50)$$

where K_{F} and A_{F} are user enterable parameters, g_{m} is the small signal transconductance gain at the Q-point, I_{DQ} is the quiescent drain current, L_{eff} is the effective channel length and f is frequency in Hz. All noise sources are assumed to be uncorrelated. S_{W} and S_{f} add to obtain the overall noise spectral density as discussed in Sec. 3.1.8.

4.2.5 Temperature Dependence of the MOSFET

Several of the parameters that characterize the MOSFET are temperature dependent. Specifically, SPICE models the temperature dependence of the parameters K' , V_{T0} , μ_{o} , ϕ , ϕ_{B} , I_{S} , J_{S} , C_{BD} , C_{BS} , CJ, CJSW, K_{F} and A_{F} . The basic equations used to characterize the temperature dependence in most situations are given below. See Reference 9 and subroutine TMPUPD of the SPICE source code for additional details.

$$K'(T) = \left(\frac{T}{T_1}\right)^{\frac{3}{2}} K'(T_1) \quad (4.2-51)$$

$$\mu_{\text{o}}(T) = \left(\frac{T}{T_1}\right)^{\frac{3}{2}} \mu_{\text{o}}(T_1) \quad (4.2-52)$$

$$I_S(T) = I_S(T_1) e^{\left[\frac{EG(T)}{V_i(T)} - \frac{EG(T_1)}{V_i(T_1)} \right]} \quad (4.2-53)$$

$$J_S(T) = J_S(T_1) e^{\left[\frac{EG(T)}{V_i(T)} - \frac{EG(T_1)}{V_i(T_1)} \right]} \quad (4.2-54)$$

$$\phi(T) = \phi(T_1) \cdot (T/T_1) + \phi_{BF}(T) \quad (4.2-55)$$

$$\phi_B(T) = \phi_B(T_1) \cdot (T/T_1) + \phi_{BF}(T) \quad (4.2-56)$$

$$C_{BD}(T) = C_{BD}(T_1) \cdot [1 + \theta_C(T)] \quad (4.2-57)$$

$$C_{BS}(T) = C_{BS}(T_1) \cdot [1 + \theta_C(T)] \quad (4.2-58)$$

$$CJ(T) = CJ(T_1) \cdot [1 + \theta_C(T)] \quad (4.2-59)$$

$$CJSW(T) = CJSW(T_1) \cdot [1 + \theta_C(T)] \quad (4.2-60)$$

$$\kappa_F(T) = \kappa_F(T_1) \cdot [\phi_B(T)/\phi_B(T_1)] \quad (4.2-61)$$

$$A_F(T) = A_F(T_1) \cdot [\phi_B(T)/\phi_B(T_1)] \quad (4.2-62)$$

where T_1 is any reference temperature in °K, $V_i = kT/q$, and the parameters EG , ϕ_{BF} , and θ_C are defined respectively by the equations

$$EG(T) = [1.16 - (.000702T^2)/(T + 1108)] \text{volts} \quad (4.2-63)$$

$$\phi_{BF}(T) = -3V_i \ln(T/T_1) - EG(T) + \{EG(T_1)\} \cdot (T/T_1) \quad (4.2-64)$$

and

$$\theta_C(T) = MJ \cdot \{0.0004(T - T_1) + 1 - [\phi_B(T)/\phi_B(T_1)]\} \quad (4.2-65)$$

4.3 DIODE MODEL

Individual diodes are modeled by a two-step process in SPICE.^{1,3,5} The device element line (card) contains information about the nodal location of the device in the circuit as well as geometrical information (relative junction cross-sectional area) and optional initial condition variables useful in transient analyses. In the device element line, reference is made to a specific device model. The .MODEL line (card) contains generic information about the electrical characteristics of devices formed in the process based upon the characterizing process parameters. Each diode has a separate device element line. Typically many devices will reference a single .MODEL line. Most of the diode modeling information can be found in subroutines DIODE and MODCHK in the SPICE source code. As is the case for all device models in SPICE, the small signal parameters which characterize the small signal operation of the diode are calculated from the appropriate derivatives. A philosophy distinctly different from that used for characterizing MOS processes has been adopted for characterizing the process used to fabricate diodes. This difference lies in that the characteristics of a specific

“reference diode” are specified in the .MODEL line. The size of the reference diode is conceptually arbitrary although it is advised to select a reference that is geometrically similar in size and shape to those devices that will be modeled. In the device element line (card) the *relative area* of the reference diode used to characterize the model is specified.

The diode is modeled as the series combination of a resistor, r_s , and a non-ideal diode, D2, shunted by a parasitic capacitor C_D , as indicated in Fig. 4.3-1. The resistor, r_s , accounts for both the series resistance of the diode as well as high-level injection effects.^{3,19} It is assumed to be an ideal resistor. In this section, emphasis will be placed upon the model of the series diode, D2, of Fig. 4.3-1b. As indicated in Fig. 4.3-1b, the current of diode D2 is modeled as the sum of a dc (large signal) current, denoted by I_{DC} , and a current that flows through a parasitic shunting capacitance associated with the pn junction. The large signal current and parasitic capacitance current will be considered separately in the following sections.

4.3.1 Large Signal Diode Current

The large signal diode current, I_{DC} in Fig. 4.3-1b, is modeled by that given in the standard diode equation

$$I_{DC} = I_S A_n (e^{V_D/(nV_t)} - 1) \quad (4.3-1)$$

where, as discussed in Chapter 3,

$$V_t = \frac{kT}{q} \quad (4.3-2)$$

I_S = saturation current

and

n = emission coefficient.

The parameter A_n represents the *normalized* cross-sectional area of the junction. It is a dimensionless parameter that is entered on the device element line; it represents the ratio of the cross-sectional area of the device on the device element

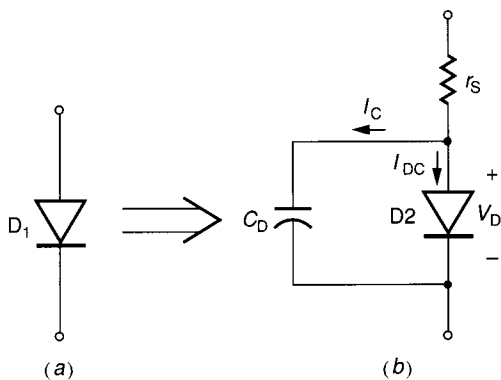


FIGURE 4.3-1
Diode model in SPICE: (a) Physical two-terminal device, (b) Equivalent circuit.

line to the reference model which is characterized on the .MODEL line. If not specified, SPICE adopts a default value of $A_n = 1$. The reverse breakdown voltage, BV , is not of major concern in VLSI design since BV generally exceeds the maximum voltages which will be permitted in VLSI circuits.

4.3.2 High-Frequency Diode Model

At high frequencies the parasitic junction capacitance of the diode plays a major role in the performance of the diode. The junction capacitance also affects the transient response. In the following the capacitance is defined by the expression

$$C_D = \frac{dQ}{dV_D} \quad (4.3-3)$$

C_D thus represents the small signal parasitic capacitance. In general, C_D is strongly a function of the instantaneous dc operating point of the diode. Although the model for C_D will be given here, the charge Q is regularly used internally in SPICE for transient analysis.

As discussed in Chapter 3 and Section 4.2, the characterization of a junction capacitor under reverse bias is different from the characterization under forward bias. Under reverse bias (actually for $V_D < FC \cdot \phi_B$), the capacitance is modeled by the equation

$$C_D = \frac{C_{j0}A_n}{[1 - (V_D/\phi_B)]^m} + \frac{\tau I_S A_n}{n V_t} e^{V_D/(nV_t)} \quad (4.3-4)$$

where I_S , A_n , n , and V_t are as previously defined, and the remaining parameters are defined by

- C_{j0} = zero-bias junction capacitance
- ϕ_B = capacitance barrier potential
- m = grading coefficient
- τ = transit time
- FC = coefficient for forward/reverse bias transition

As was the case for I_S , it should be noted that C_{j0} is the zero-bias junction capacitance of the specific area device referred to by the .MODEL line. Although the first term on the right-hand side of (4.3-4) is essentially functionally equivalent to that used in the model of the junction capacitance for the MOSFET, (4.2-42) of Section 4.2, it should be emphasized that in SPICE C_{j0} represents the capacitance density in (4.2-42), whereas C_{j0} represents the capacitance of the reference diode itself in (4.3-4).

The second term on the right-hand side of (4.3-4) arises from the charge stored in the junction due to minority carrier injection. The transit time, τ , characterizes this capacitance.

For $V_D > FC \cdot \phi_B$, SPICE models the capacitance, C_D , with the equation

$$C_D = \frac{C_{j0}A_n}{(1 - FC)^{(1+m)}} \left(1 - FC \left[1 + m \right] + \frac{mV_D}{\phi_B} \right) + \frac{\tau I_S A_n}{n V_t} e^{V_D/(nV_t)} \quad (4.3-5)$$

The first term on the right-hand side of (4.3-5) represents a continuous and differentiable linear extension of the first term on the right-hand side of (4.3-4) across the boundary $V_D = FC \cdot \phi_B$. The second terms on the right-hand side, of Eqs. 4.3-4 and 4.3-5 are identical.

4.4 BJT MODEL

The SPICE model of the BJT is based upon a modified Gummel–Poon model.^{20,21} Simulations based upon the simpler Gummel–Poon model discussed in Chapter 3 can also be readily made by setting the appropriate Ebers–Moll parameters to zero as will be discussed later in this section. Use of the Ebers–Moll model in the early stages of a simulation may be useful for verifying theoretical hand calculations.

The bipolar junction transistor is modeled by two input lines (cards) in SPICE. The device line (card) is used for indicating the nodal connections of the BJT in a circuit. It is also used to reference a specific model, by name, which contains process information. An optional normalized parameter on the device line, A_n , is used to indicate the ratio of the area of the emitter to the emitter area of the device of the referenced model. An optional initial condition parameter can also be included on the device line if desired.

The second input line (card) that is used to model the BJT is the .MODEL line. SPICE version 2G.6 provides for user entry of up to 40 parameters on the .MODEL line for characterizing the device. As was the case with the diode, a user-selected reference transistor is used to characterize the bipolar process. The BJT model information is contained primarily in subroutines MODCHK and BJT in the SPICE source code. MODCHK does preprocessing of some of the input parameters (e.g., the reciprocals of some parameters are actually used as variables in the source code rather than the parameters themselves). The model itself basically appears in subroutine BJT.

As is the case for the other semiconductor models in SPICE, the BJT model is characterized by four types of input parameters. These are 1) large signal or dc parameters, 2) charge storage or capacitance parameters, 3) noise parameters, and 4) temperature characterization parameters.

The small signal low-frequency model used in SPICE is obtained from a symbolic differentiation of the large signal current equations evaluated at the dc operation point. As is the case for all small signal analyses in SPICE, the small signal model of the BJT is linear and thus the small signal simulation gives no distortion information. (Distortion information at a specific frequency can be obtained from a much more time consuming transient response with a sinusoidal excitation of fixed frequency and amplitude.) To obtain reliable distortion information, it is crucial that the transient analysis interval is long enough to guarantee essentially steady state operation.

A series resistance is modeled in series with each lead of the BJT as indicated in Fig. 4.4-1. These resistances are input parameters in SPICE. In the model discussion that follows, all formulation is relative to transistor T2 (denoted by nodes C , B , and E) in this figure; specifically, V_{BE} and V_{CE} represent the base–emitter and collector–emitter voltages of T2 rather than the actual base–emitter and collector–emitter voltages of the device (denoted by nodes C_A , B_A , and E_A)

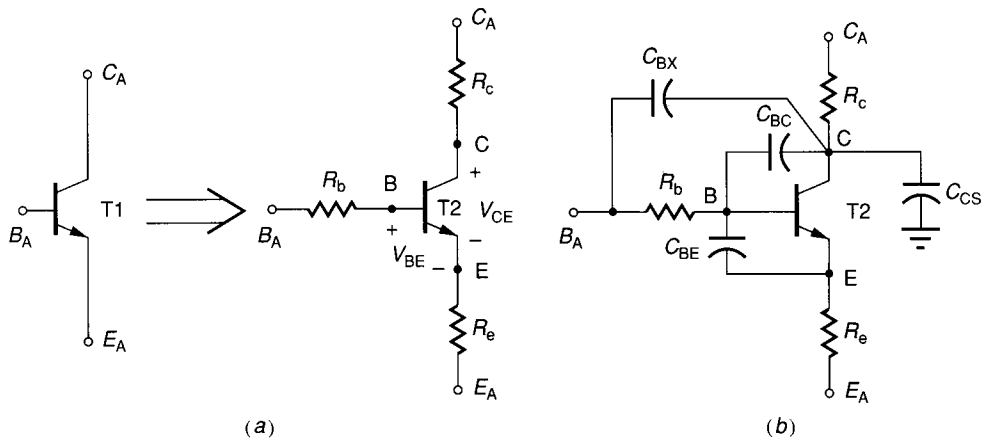


FIGURE 4.4-1 Modeling of the BJT in SPICE: (a) dc modeling, (b) High-frequency modeling.

which is to be modeled, T1. In the model that follows, junction breakdown voltages will not be discussed in detail since, with the exception of the reverse base-emitter breakdown, voltage levels in bipolar integrated circuits are usually considerably below the breakdown voltages of the BJT.

4.4.1 Large Signal BJT Model

The collector current and base current are characterized by the equations

$$I_C = \frac{I_S A_n}{Q_B} (e^{V_{BE}/(NF \cdot V_t)} - 1) - I_S A_n \left(\frac{1}{Q_B} + \frac{1}{BR} \right) (e^{V_{BC}/(NR \cdot V_t)} - 1) - I_{SC} A_n (e^{V_{BC}/(NC \cdot V_t)} - 1) \quad (4.4-1)$$

$$I_B = \frac{I_S A_n}{BF} (e^{V_{BE}/(NF \cdot V_t)} - 1) + \frac{I_S A_n}{BR} (e^{V_{BC}/(NR \cdot V_t)} - 1) + I_{SE} A_n (e^{V_{BE}/(NE \cdot V_t)} - 1) + I_{SC} A_n (e^{V_{BC}/(NC \cdot V_t)} - 1) \quad (4.4-2)$$

where $V_t = kT/q$

- A_n = normalized emitter area ratio
- I_S = saturation current
- I_{SE} = B-E leakage saturation current
- I_{SC} = B-C leakage saturation current
- NF = forward current emission coefficient
- NR = reverse current emission coefficient
- NE = B-E leakage current emission coefficient
- NC = B-C leakage current emission coefficient
- BF = ideal maximum forward β
- BR = ideal maximum reverse β

and

$$Q_B = \left[\frac{1}{1 - (V_{BC}/V_{AF}) - (V_{BE}/V_{AR})} \right] \left[\frac{1 + \sqrt{1 + 4\left\{ (I_S/I_{KF})\left(e^{V_{BE}/(NF \cdot V_T)} - 1\right) + (I_S/I_{KR})\left(e^{V_{BC}/(NR \cdot V_T)} - 1\right) \right\}}}{2} \right] \quad (4.4-3)$$

The parameters in (4.4-3) are defined as

$$\begin{aligned} V_{AF} &= \text{Forward Early Voltage} \\ V_{AR} &= \text{Reverse Early Voltage} \\ I_{KF} &= \text{Corner for forward current gain roll-off} \\ I_{KR} &= \text{Corner for reverse current gain roll-off} \end{aligned}$$

This completes the large signal model of the BJT. A discussion of the characterizing parameters in the BJT model follows. In addition to providing insight into how these parameters impact performance of the BJT, this discussion should provide a mechanism for obtaining SPICE parameters from measured device data.

Although it may appear that all dependence of I_C and I_B on V_{BE} and V_{BC} is exponential, it can be seen from (4.4-3) that Q_B is a complicated function of V_{BC} and V_{BE} . If I_{KF} and I_{KR} are neglected (i.e., $I_{KF} = I_{KR} = \infty$), then Q_B reduces to

$$Q_B = \left(1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AR}} \right)^{-1} \quad (4.4-4)$$

so that the $\frac{1}{Q_B}$ term in (4.4-1) becomes

$$Q_B^{-1} = 1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AR}} = 1 + \frac{V_{CE}}{V_{AF}} - V_{BE} \left(\frac{1}{V_{AF}} + \frac{1}{V_{AR}} \right) \quad (4.4-5)$$

which is approximately equal to the multiplying factor used to model Early Voltage effects in the extended Ebers-Moll model of Chapter 3. Even if I_{KF} and I_{KR} effects are included, Q_B can be approximated by (4.4-4) until V_{BE} or V_{BC} becomes quite large, since I_{KF} is typically about ten orders of magnitude larger than I_S . For large V_{BE} or V_{BC} , however, I_C varies essentially linearly with $e^{V_{BE}/2NF \cdot V_T}$ or $e^{V_{BC}/2NR \cdot V_T}$.

Considerable insight into how the parameters affect device performance can be obtained by plotting I_C and I_B versus one device branch voltage, V_{BE} or V_{BC} , with the other branch voltage set to zero. For brevity, only the $V_{BC} = 0$ case will be considered here. The analysis for the $V_{BE} = 0$ case is essentially a mirror image of the $V_{BC} = 0$ analysis.

Under the assumption that $V_{BC} = 0$, (4.4-1), (4.4-2) and (4.4-3) simplify to

$$I_C = \frac{I_S A_n}{Q_B} \left(e^{V_{BE}/(NF \cdot V_T)} - 1 \right) \quad (4.4-6)$$

$$I_B = \frac{I_S A_n}{BF} (e^{V_{BE}/(NF \cdot V_T)} - 1) + I_{SE} A_n (e^{V_{BE}/(NE \cdot V_T)} - 1) \tag{4.4-7}$$

$$Q_B = \left[\frac{1}{1 - (V_{BE}/V_{AR})} \right] \left[\frac{1 + \sqrt{1 + 4(I_S/I_{KF})(e^{V_{BE}/(NF \cdot V_T)} - 1)}}{2} \right] \tag{4.4-8}$$

A plot of I_C and I_B versus V_{BE} for $V_{BE} < 0$ is shown in Fig. 4.4-2. The parameter A_n , which denotes the relative emitter area, is obtained from geometrical information. The projection of the linear portion of the I_C curve intercepts the I axis at $-I_S A_n$. The slope of the linear portion of the I_C curve can subsequently be used to determine V_{AR} . The vertical axis intercept of the projection of the linear portion of the I_B curve can be used to determine I_{SE} since I_{SE} is typically about four orders of magnitude larger than I_S/BF . Although the $V_{BE} < 0$ curves can be used to determine I_S , I_{SE} and V_{AR} , they are most useful for the V_{AR} determination. The parameters I_S and I_{SE} are typically determined from the $V_{BE} > 0$ plots.

A plot of I_C and I_B versus V_{BE} for $V_{BE} > 0$ is shown in Fig. 4.4-3 on a graph with a logarithmic scale for the vertical axis. Also shown are four straight lines which essentially represent asymptotic behavior of the BJT over a fairly wide range of V_{BE} values. The equations of these asymptotic lines are easily derived from (4.4-6)–(4.4-8). Several of the dc parameters that characterize the BJT can be readily determined from the curves shown in Fig. 4.4-3. A sequence of calculations follows for determining some of the dc parameters after V_{AR} has been determined from Fig. 4.4-2.

First, I_S and I_{SE} can be determined from the y-intercepts of Line 3 and Line 2, respectively. With I_S known, BF can be determined from the y-intercept of Line 4. I_{KF} can be determined from either the vertical axis intercept of Line 1 or the y-coordinate of the intersection of Lines 1 and 3. NF can be obtained

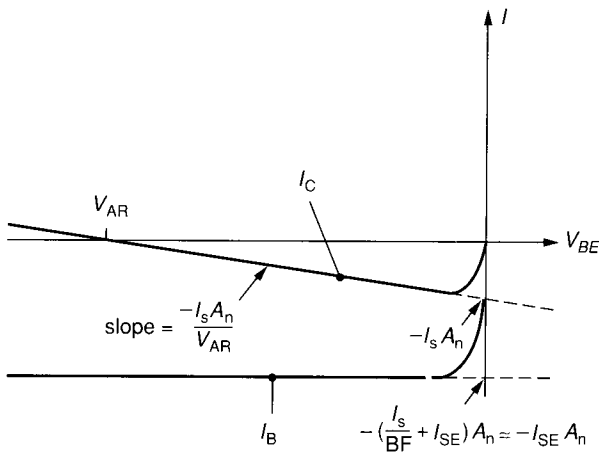
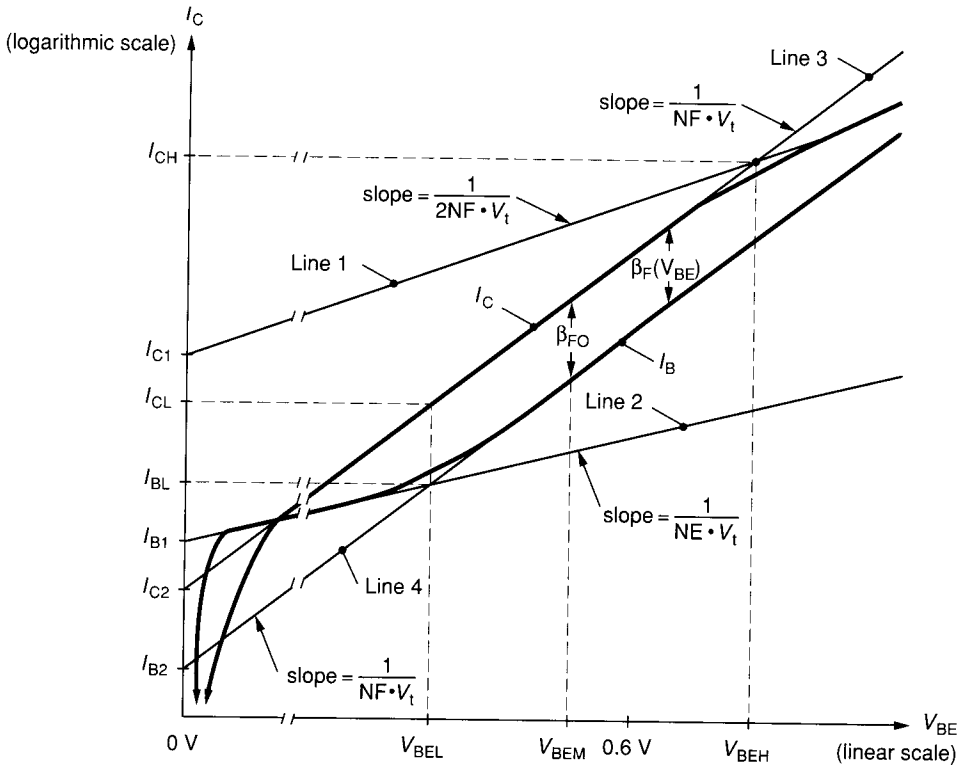


FIGURE 4.4-2
Plot of collector and base current vs. V_{BE} for $V_{BC} = 0$, $V_{BE} < 0$.



$$V_{BE_L} = \frac{V_t \cdot NE \cdot NF}{NE - NF} \ln \left(\frac{I_{SE} \cdot BF}{I_S} \right) \quad I_{CH} = I_{KF} A_n \left(1 + \frac{0.6 \text{ V}}{V_{AR}} \right)$$

$$V_{BE_H} = V_t \cdot NF \cdot \ln \left(\frac{I_{KF}}{I_S} \right) \quad I_{C1} = A_n \sqrt{I_S I_{KF}} \left(1 + \frac{0.6 \text{ V}}{V_{AR}} \right)$$

$$\text{Line 1: } I = \left(1 + \frac{0.6 \text{ V}}{V_{AR}} \right) A_n \sqrt{I_S I_{KF}} e^{\frac{V_{BE}}{2NF \cdot V_t}} \quad I_{CL} = I_{SE} A_n \left(\frac{I_{SE} \cdot BF}{I_S} \right)^{\frac{NF}{NE - NF}}$$

$$\text{Line 2: } I = I_{SE} A_n e^{\frac{V_{BE}}{NE \cdot V_t}} \quad I_{BL} = A_n I_{SE}^{\frac{NE}{NE - NF}} \left(\frac{I_S}{BF} \right)^{\frac{NF}{NE - NE}}$$

$$\text{Line 3: } I = \left(1 + \frac{0.6 \text{ V}}{V_{AR}} \right) I_S A_n e^{\frac{V_{BE}}{NF \cdot V_t}} \quad I_{B1} = I_{SE} A_n$$

$$\text{Line 4: } I = \frac{I_S A_n}{BF} e^{\frac{V_{BE}}{NF \cdot V_t}} \quad I_{C2} = I_S A_n \left(1 + \frac{0.6 \text{ V}}{V_{AR}} \right)$$

$$I_{B2} = \frac{I_S A_n}{BF}$$

FIGURE 4.4-3 Plot of collector current and base current vs. V_{BE} for $V_{BC} = 0, V_{BE} > 0$ (logarithmic scale on vertical axis).

from the slope of Lines 1, 3, or 4, while NE can be determined from the slope of Line 2. At this point, it is easy to verify that *all* parameters in the dc model of (4.4-1)–(4.4-3) can be determined from the plots in Fig. 4.4-2 and Fig. 4.4-3 and the corresponding plots for $V_{BE} = 0$, $V_{BC} > 0$.

The current gain of the BJT is often of interest. Defining the forward current gain (a similar procedure can be used for the reverse current gain) by the expression

$$\beta_F = \left. \frac{I_C}{I_B} \right|_{V_{BC}=0} \quad (4.4-9)$$

it follows from the curves in Fig. 4.4-3 that β_F is V_{BE} dependent. For a rather large range of V_{BE} , however, it is essentially constant and (neglecting V_{AR} effects) approximately equal to

$$\beta_F = \beta_F \approx \beta_{FO} \quad (4.4-10)$$

where β_{FO} represents the maximum value of β_F for $V_{BEL} < V_{BE} < V_{BEH}$ and where V_{BEL} and V_{BEH} are as defined in Fig. 4.4-3. V_{BEM} denotes value of V_{BE} where β_F is maximum. At lower V_{BE} , β_F decreases due to changes in the characteristics of I_B ; for higher V_{BE} , β_F decreases due to changes in the characteristics of I_C . A plot of β_F versus V_{BE} as defined by Eq. 4.4-9 appears in Fig. 4.4-4. It can be seen from Figs. 4.4-3 and 4.4-4 that the parameter I_{KF} is approximately equal to the value of collector current where high-current roll-off in β_F occurs, which explains the name for I_{KF} , “corner for forward current gain roll-off.” The corresponding low-frequency roll-off, which occurs at $V_{BE} = V_{BEL}$, is not characterized by a single parameter but is strongly dependent upon the B–E leakage saturation current, I_{SE} .

This section concludes with a discussion of how the SPICE model parameters can be specified to do simulations based upon the simplified Ebers–Moll model of Chapter 3, characterized by Eqs. 3.3-1 and 3.3-2.

It follows from Eqs. 4.4-1–4.4-3 that if $I_{SE} = I_{SC} = 0$, $I_{KF} = I_{KR} = \infty$, $V_{AF} = V_{AR} = \infty$ and $NF = NR = 1$, the model will agree with this Ebers–Moll model. Since these variable assignments are the default values, the user only needs to specify IS, BF, and BR to use the simplified dc Ebers–Moll model.

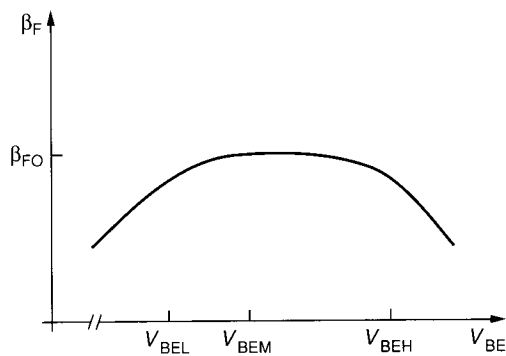


FIGURE 4.4-4
Forward current gain of BJT vs. V_{BE} ($V_{BC} = 0$).

4.4.2 High-Frequency BJT Model

The high-frequency model of the BJT used in SPICE is obtained by adding three parasitic capacitors to the transistor T2 in Fig. 4.4-1 and one capacitor, CBX, between the base of T1 (node B_A) and the collector of T2 (node C). The parasitic capacitors are, in general, voltage dependent. The capacitor values used in SPICE are defined by the derivative

$$C = \frac{dQ}{dV} \quad (4.4-11)$$

where Q is the charge on the capacitor and V is the corresponding port voltage. Seventeen parameters are used to characterize the four parasitic capacitors in SPICE.

The parasitic capacitors are, in general, modeled by the parallel combination (sum) of a depletion region capacitor and a capacitor which occurs due to charge accumulation in the depletion region. The depletion region capacitor is voltage dependent and is modeled by Eqs. 3.2-8 and 3.2-9 of Chapter 3. The capacitor attributed to the charge accumulation is current dependent. Finally, under forward bias the model for the parasitic capacitors has a different parametric form, than under reverse bias. The voltage where transition must be made from the reverse bias parametric capacitance model to the forward bias parametric model is termed the transition voltage. A summary of the parasitic capacitors used in SPICE 2G.6 is shown in Table 4.4-1.

The depletion region reverse-biased junction capacitors are defined by the expressions

$$C_{BEDR} = A_n C_{JE} \left(1 - \frac{V_{BE}}{\phi_B} \right)^{-M_{JE}} \quad (4.4-12)$$

$$C_{BCDR} = \theta A_n C_{JC} \left(1 - \frac{V_{BC}}{\phi_C} \right)^{-M_{JC}} \quad (4.4-13)$$

$$C_{CSDR} = A_n C_{JS} \left(1 - \frac{V_{CS}}{\phi_S} \right)^{-M_{JS}} \quad (4.4-14)$$

$$C_{XSDR} = (1 - \theta) A_n C_{JC} \left(1 - \frac{V_{B^cC}}{\phi_C} \right)^{-M_{JC}} \quad (4.4-15)$$

where M_{JE} , M_{JS} , M_{JC} , C_{JE} , C_{JS} and C_{JC} are input parameters. ϕ_B , ϕ_S , ϕ_C , and θ are also SPICE input parameters, denoted by PB, PS, PC and XCJC, respectively. The parameter θ represents the percentage of the B-C capacitance which is to be associated with the internal base node (base of T2 in Fig. 4.4-1). V_{B^cC} is the voltage from the base of T1 to the collector of T2 in Fig. 4.4-1.

The transition voltages V_{BET} , V_{BCT} , V_{CST} and V_{XST} are $FC \cdot \phi_B$, $FC \cdot \phi_C$, 0 V, and $FC \cdot \phi_C$ respectively where FC is a SPICE input parameter used to characterize the transition.

The forward biased depletion junction capacitors C_{BEDF} , C_{BCDF} , C_{CSDF} , and C_{XSDF} are the continuous and differentiable linear extensions of Eqs. 4.4-12–