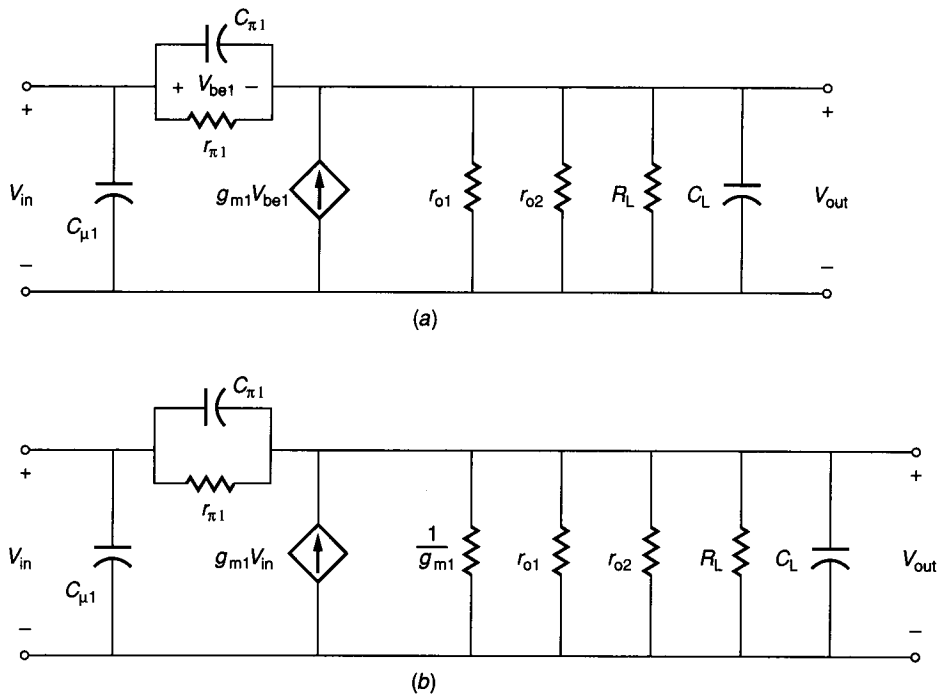


FIGURE 6.4-11
(*a*) Small signal model of Fig. 6.4-9*b*, (*b*) Simplified equivalent of (*a*).

Assuming that Fig. 6.4-12 is voltage-driven allows us to find the transfer function as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_m + G_2 + sC_2}{G_2 + G_3 + s(C_L + C_2)} \tag{6.4-22}$$

From Eq. 6A-20 and 6.4-21, the midband gain is

$$\frac{V_{out}}{V_{in}} = A_{v0} = \frac{g_m + G_2}{G_2 + G_3} \approx \frac{g_{m1}}{g_{m1} + G_L} \tag{6.4-23}$$

The zero of Eq. 6.4-22 is

$$z_1 = -\frac{g_m + G_2}{C_2} \approx -\frac{g_{m1}}{C_2} \tag{6.4-24}$$

and the pole is

$$p_1 = -\frac{G_2 + G_3}{C_2 + C_L} \approx -\frac{g_{m1} + G_L}{C_L} \tag{6.4-25}$$

Typically, $|p_1| < |z_1|$. If the pole and zero are close together, they will tend to cancel each other.

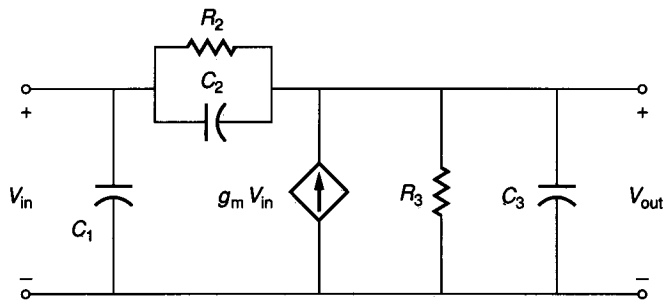


FIGURE 6.4-12
Generic small signal follower model.

The output resistance of the follower not including R_L is found from Fig. 6.4-12 as

$$r'_{out} = (G_2 + G_3)^{-1} = (G_2 + g_{m1})^{-1} \approx \frac{1}{g_{m1}} \tag{6.4-26}$$

For the MOS follower, this resistance is expressed as

$$r'_{out} \simeq \left(\frac{L_1}{2K'_N W_1 I_{D1}}\right)^{1/2} \tag{6.4-27}$$

and for the BJT follower, the output resistance is

$$r'_{out} \simeq \frac{V_t}{I_{C1}} \tag{6.4-28}$$

If the bias current in both followers of Fig. 6.4-9 is 100 μA, and if $W_1 = 10L_1$ and $K'_N = 25\ \mu A/V^2$, then the output resistance of the MOS follower is 4.47 kΩ and that of the BJT follower is 250 Ω.

The performance of the BJT follower is ideally independent of the emitter areas. Considerations of power dissipation and matching suggest large emitter areas whereas capacitive loading and high frequency response suggest small emitter areas.

The Class A shunt feedback follower configuration has the further disadvantage of an asymmetric current sinking and sourcing capability. For the followers of Fig. 6.4-9, the maximum current sourcing capability is limited primarily by the driver. For the MOS follower, the gate voltage of M1 must be sufficiently larger than the output voltage in order for M1 to source the required current. For the BJT follower, the current sourcing is directly related to the amount of base current the driver can provide. The sinking capability is equal to the bias current. As a consequence, the sourcing and sinking capabilities are usually different. The maximum efficiency of either follower configuration of Fig. 6.4-9 is 25%.

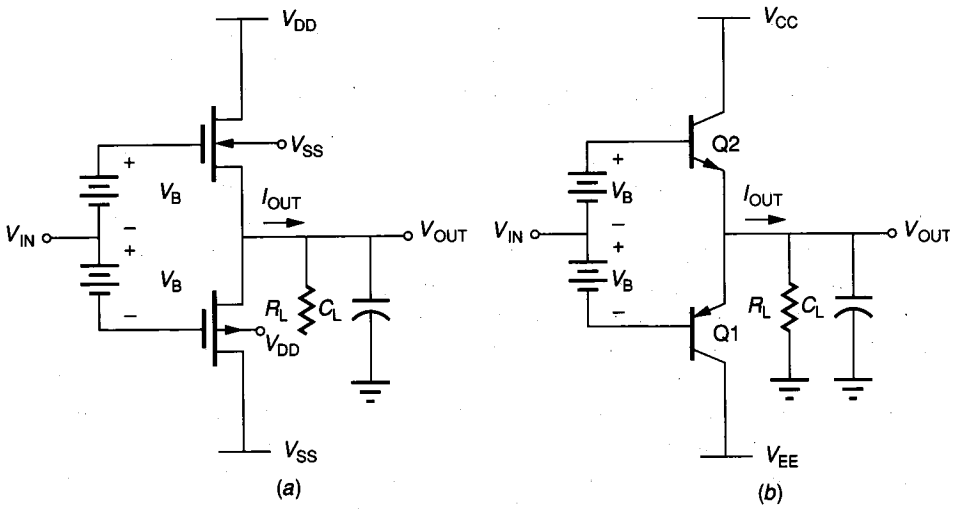


FIGURE 6.4-13
(*a*) Class B source follower, (*b*) Class B emitter follower.

In summary, the Class A follower has very low output resistance, poor signal swing, and low efficiency. The efficiency of the Class A follower can be improved by the Class B followers shown in Fig. 6.4-13. This configuration is also called the Class B push-pull amplifier. The maximum possible efficiency is 78.5%. Also, the maximum sourcing and sinking capabilities are likely to be of the same magnitude, although this depends on the driver. The signal swings at both the positive and negative limits will suffer from the increasing V_T for the MOS Class B follower and from the inability to provide sufficient base currents for the BJT Class B follower.

Figure 6.4-14 shows how the floating batteries, V_B, can be implemented for the Class B followers. In this case, the input is applied at the gate of M3 (base of Q3) instead of to the sources of M4 and M5 (bases of Q4 and Q5) and will require some form of level shifting. The bias current in M4 and M5 (Q4 and Q5) determines whether the circuit is Class B or Class AB. It is generally preferable to bias the output devices in Class AB in order to minimize the crossover distortion that occurs in the push-pull, follower type amplifier when the output current switches from one device to the other. Unfortunately, it is never possible to eliminate this distortion, and it is usually necessary to use external negative feedback to reduce the nonlinear distortion to an acceptable level. Figure 6.4-14 illustrates some of the problems in obtaining a large output signal swing for the Class B follower circuit. For example, the maximum output voltage of the circuit of Fig. 6.4-14*a* is approximately $V_{GG6} - V_{TO6} - V_{T2}$. This limit will usually be several volts below V_{DD}. The negative swing is a little better since M3 can take the gate of M1 to V_{SS}. Thus, the negative signal swing is approximately $V_{SS} + V_{T1}$. Unfortunately, V_{T1} will be larger than V_{TO1} because of the body effect.

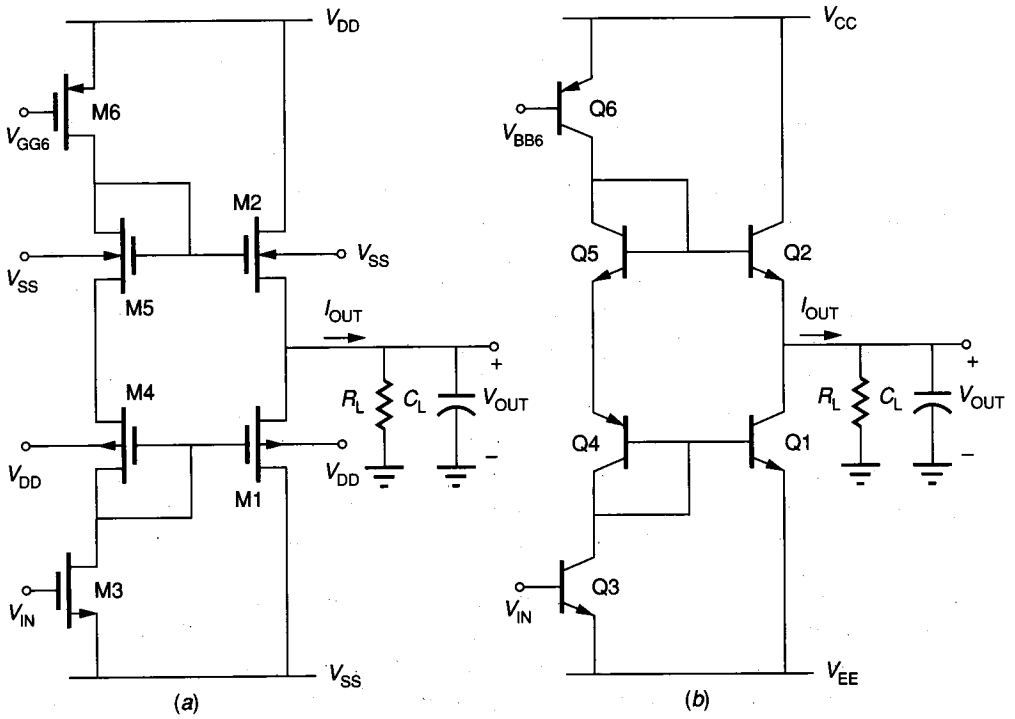


FIGURE 6.4-14
Implementation of: (*a*) Fig. 6.4-13*a*, and (*b*) Fig. 6.4-13*b*, including the implementation of V_B.

At this point we have a situation that often occurs in analog circuit design. The right principles have been identified, but the implementation is still not practical. None of the preceding output amplifiers have contained all of the desirable features of (1) large output signal swings, (2) low output resistance, (3) high efficiency, and (4) low nonlinear distortion. In addition, high frequency performance is also desirable. A practical solution to our problem is shown in Fig. 6.4-15, where we have taken the best candidate and concentrated on improving its negative characteristics. The Class B/Class AB common source (emitter) amplifiers in Fig. 6.4-4 offer good swing characteristics, high efficiency, and low nonlinear distortion. Their primary disadvantage is a high output impedance. Combining the shunt feedback principle with the common-source or common-emitter Class B or Class AB amplifier results in an output stage that meets all specifications even though it has been complicated by additional circuitry.

The output resistance of Fig. 6.4-4 will be reduced approximately by the value of loop gain as given in Eq. 6.4-19. The loop gain of the circuit of Fig. 6.4-15 will be that of the inverter plus the error amplifier. We note that the error amplifier could be implemented by the differential amplifiers of the preceding section. The error amplifiers are designed to turn on M1 or M2 (Q1 or Q2) in a manner that minimizes crossover distortion but maximizes efficiency.

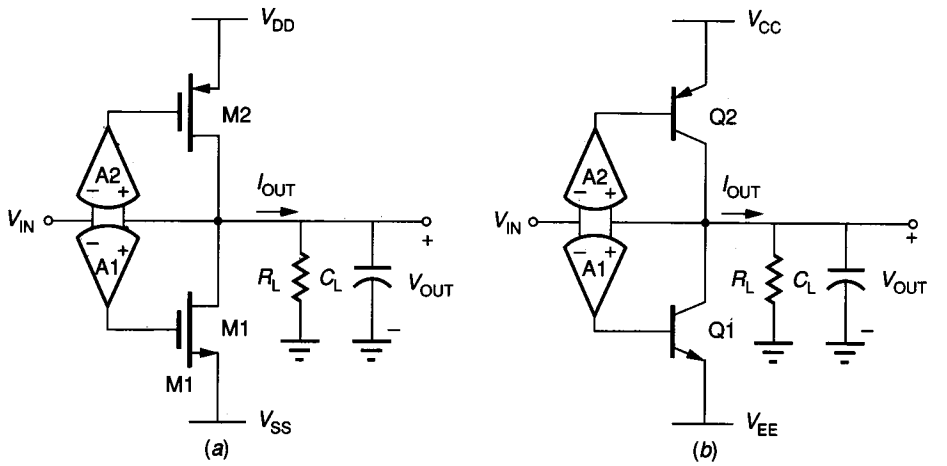


FIGURE 6.4-15
Use of negative feedback with error amplifiers A1 and A2 to obtain an improved output amplifier: (*a*) MOS, (*b*) BJT.

Figure 6.4-16 shows an interesting implementation of the circuit of Fig. 6.4-15. Since the inverter can have reasonable gain, it is possible to use resistive feedback to replace the more complex error amplifier. The resistance R_2 should be twice R_1 so that the input signal does not have to be capable of maintaining the output signal swing. The resistors do not have to be carefully matched and could be polysilicon, diffusion, n- or p-well, or even transistors in the case of the MOS version. Assuming that $R_2 = 2R_1$, the loop gain would be

$$\text{LG} \simeq \frac{g_m R_L}{3} \tag{6.4-29}$$

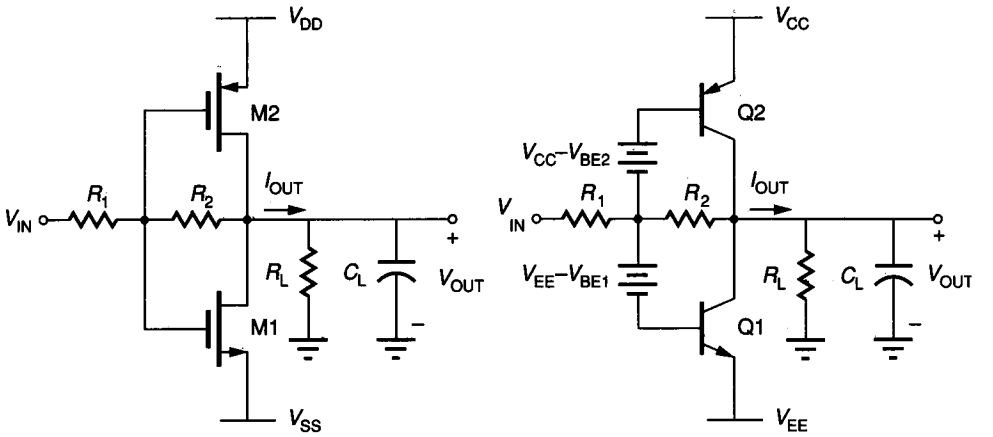


FIGURE 6.4-16
A possible implementation of Fig. 6.4-15.

where g_m is the transconductance of M1 or M2 (Q1 or Q2). Thus, the output resistance of the circuit of Fig. 6.4-16 is expressed as

$$r'_{out} \simeq \frac{r_{out}}{1 + (g_m R_L/3)} \tag{6.4-30}$$

where r_{out} is the resistance of the output amplifier with the loop open.

The frequency response of output amplifiers should be large in order not to cause stability problems in the circuit driving the output amplifier. In general, the frequency response of the output amplifier is determined by its input resistance and capacitance. This implies that the input devices of the output amplifier should be as small as possible for high frequency response.

The design of an output amplifier capable of serving as a buffer between an integrated circuit amplifier and a load consisting of a small resistance and/or large capacitance has been considered in this section. Although not all approaches have been examined, the material discussed gives the principles and allows the reader to appreciate the problems involved. The performance of the various output amplifiers presented in this section is compared in Table 6.4-1. The comparison is made on a qualitative basis because of the complexity involved in the analysis of output amplifiers. In many cases, the performance of the output amplifier determines the performance of the overall circuit and will require much more attention than has been allocated in this section. All of the circuits presented have been used in actual integrated circuits and will be used in various circuits in the next section.

6.5 OPERATIONAL AMPLIFIERS

One of the most important circuits in analog circuit design is the operational amplifier (op amp). Its primary use is to provide sufficient gain to define and implement analog signal processing functions through the use of negative feedback. Such analog signal processing functions include amplification, integration, and summation. In this section we will consider the characteristics and architectures of general op amps. This will be followed by a "first-cut" design of two-stage BJT and CMOS op amps. Architectures capable of driving large load capacitance and small load resistance are presented and discussed. Finally, a brief consideration of simulation and testing of op amps will be given.

6.5.1 Characterization of Op Amps

An op amp has a differential input capability and is represented by the symbol shown in Fig. 6.5-1. The differential input voltages are V_1 and V_2, and the single-ended output voltage is V_O. The op amp ideally has infinite differential input resistance, R_{id}, infinite differential-mode voltage gain, A_v, and a zero output resistance, R_{out}. Although we have assumed the op amp is a voltage-controlled voltage-source, it can be implemented by any of the four types of controlled sources.

TABLE 6.4-1
Performance comparison of output amplifiers

Output amplifier	Figure	I_{OUT}^{+}	I_{OUT}^{-}	r_{OUT}	Efficiency	Linearity	Maximum voltage swing
Class A MOS inverter	6.4-1*a*	I_{BIAS}	$>> I_{BIAS}$	High	<25%	Good	Fair
Class A BJT inverter	6.4-1*b*	I_{BIAS}	$>> I_{BIAS}$	Medium	<25%	Good	Good
Class AB MOS inverter	6.4-4*a*	High for large W/L	High for large W/L	High	<50%	Fair	Fair
Class AB BJT inverter	6.4-4*b*	High if base current is large	High if base current is large	Medium	<50%	Fair	Good
Class B MOS inverter	6.4-4*a*	High for large W/L	High for large W/L	High	<75%	Poor	Fair
Class B BJT inverter	6.4-4*b*	High if base current is large	High if base current is large	Medium	<75%	Poor	Good
Class A MOS source follower	6.4-9*a*	High for large W/L	I_{BIAS}	Low	<25%	Poor	Poor (+) Good (−)
Class A BJT emitter follower	6.4-9*b*	High if base current is large	I_{BIAS}	Low	<25%	Poor	Poor (+) Good (−)
Class B MOS source follower	6.4-13*a*	High for large W/L	High for large W/L	Low	<75%	Poor	Poor
Class B BJT emitter follower	6.4-13*b*	High if base current is large	High if base current is large	Low	<75%	Poor	Poor
Class AB inverter with negative feedback	6.4-15	High if base current or W/L is large	High if base current or W/L is large	Low	<75%	Good	Good

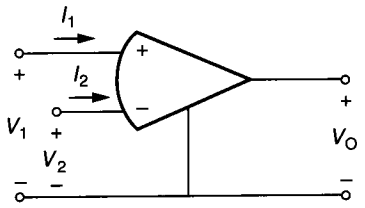


FIGURE 6.5-1
Symbol for the op amp.

In most cases, we can assume that the differential voltage gain, A_v, approaches infinity. If this assumption is valid, then the input terminals of the op amp realize a null port if the output, V_O, is connected back to the input (often through resistors or one or more op amp circuits) to achieve negative feedback. A *null port* is a two-terminal network whose voltage and current are simultaneously equal to zero. Thus, in Fig. 6.5-1, a null port is characterized by

$$| V_1 - V_2 | = 0 \tag{6.5-1}$$

and

$$| I_1 | = | I_2 | = 0 \tag{6.5-2}$$

These two relationships make it very easy to analyze the most common of op amp circuits when the differential gain is assumed to approach infinity and the output of an op amp is returned to the minus input to achieve negative feedback.

Unfortunately, the op amp only approaches the ideal op amp just described. Some of the nonideal op amp characteristics are illustrated in Fig. 6.5-2. This model will be used to define the various characteristics of the op amp. The finite differential input impedance is modeled by R_{id} and C_{id}. The output resistance

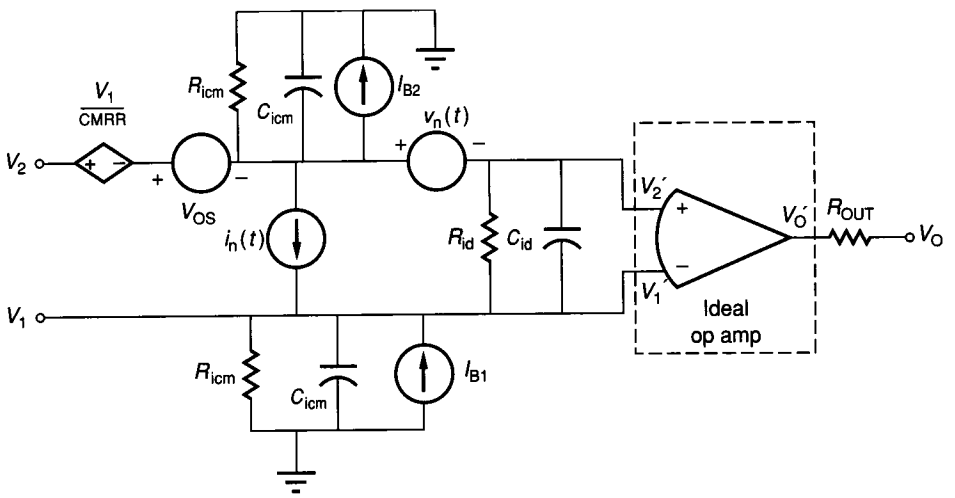


FIGURE 6.5-2
A model for a nonideal op amp showing some of the nonideal characteristics.

is modeled by R_{out}. The common-mode input resistances and capacitances are given by the resistances R_{icm} and capacitances C_{icm} connected from each of the inputs to ground. V_{OS} is the input offset voltage necessary to make the output voltage zero if both inputs of the op amp are grounded. I_{OS} (not shown) is defined as the magnitude of the difference between the two input bias currents, I_{B1} and I_{B2} necessary to make the output voltage of the op amp zero. The common-mode rejection ratio (CMRR) is approximately modeled by the voltage-controlled voltage source indicated as V_1/CMRR. The two sources designated as $\overline{V}_n$ and $\overline{I}_n$ are used to model the op amp noise and are called the noise voltage and noise current, in units of mean square volts and mean square amperes, respectively. Although these noise sources are weakly correlated, they are normally assumed to be uncorrelated.

Not all of the nonideal characteristics of the op amp are illustrated in Fig. 6.5-2. The output voltage of the op amp of Fig. 6.5-1 can be expressed as

$$V_o(s) = A_d(s)[V_1(s) - V_2(s)] + A_c(s)\left[\frac{V_1(s) + V_2(s)}{2}\right] \qquad (6.5\text{-}3)$$

where the first term on the right is the differential portion of $V_o(s)$ and the second term is the common-mode portion of $V_o(s)$. The differential frequency response of the op amp is given as $A_d(s)$, and the common-mode frequency response is given as $A_c(s)$. A typical differential frequency response for an op amp is

$$A_d(s) = \frac{A_{od}\omega_1\omega_2\omega_3\ldots}{(s + \omega_1)(s + \omega_2)(s + \omega_3)\cdots} \qquad (6.5\text{-}4)$$

where $\omega_1, \omega_2, \omega_3, \ldots$ are the poles of the operational amplifier. While the operational amplifier may have zeros, they will be ignored for the present. A_{od} (or simply A_o, where the use is understood) is the low-frequency gain of the op amp. Figure 6.5-3 shows the magnitude of a typical frequency response for the differential-mode gain, $A_d(j\omega)$ where $s = j\omega$. In this case, we see that ω_1 is much smaller than the rest of the poles, causing ω_1 to be the dominant influence in the frequency response. The objective of most compensation schemes which will be considered later is to achieve a single dominant pole so that the frequency response consists of just the -6 dB/octave slope until the magnitude of $A_d(j\omega)$ is less than 0 dB. The intersection of $|A_d(j\omega)|$ and the 0 dB axis is designated as the *unity-gain bandwidth* (GB) of the op amp. The *phase margin* is defined as the phase shift of the op amp at $\omega = GB$. A phase margin greater than 45° is desirable for negative resistive feedback around the op amp.

Other nonideal characteristics of the op amp not defined in Fig. 6.5-2 deserve mention. The *power supply rejection ratio* (PSRR) is defined as the ratio of the open loop gain of the op amp to the change in the output voltage of the op amp caused by the change in the power supply. Thus, the PSRR for V_{DD} is

$$\text{PSRR}(V_{DD}) = \frac{A_d}{(\Delta V_O/\Delta V_{DD})} = \frac{\Delta V_{DD} A_d}{\Delta V_O} \qquad (6.5\text{-}5)$$

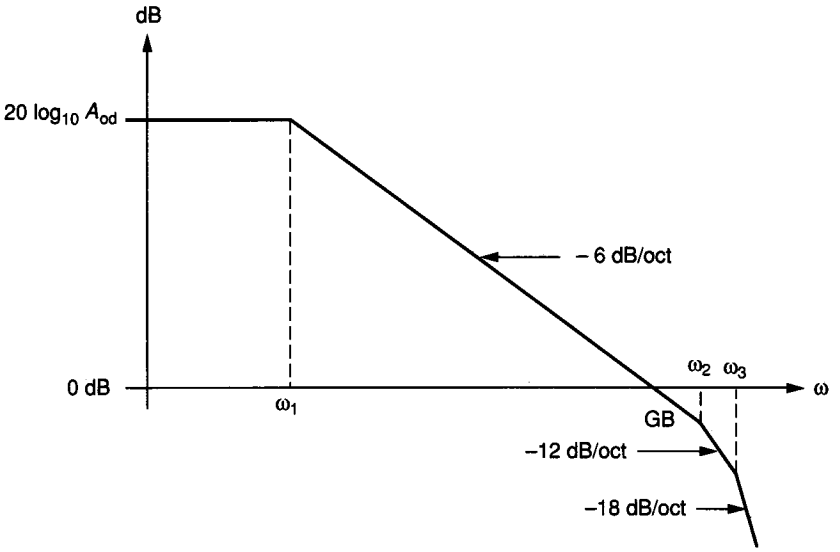


FIGURE 6.5-3
Typical frequency response of the magnitude of $A_d(j\omega)$ for an op amp.

An ideal op amp would have an infinite PSRR. The *common-mode input voltage range* is the voltage range over which the input common-mode signal can vary. Typically, this range is several volts less than the higher power supply voltage and several volts greater than the lower power supply voltage. The op amp has several other characteristics corresponding to those we have already considered for output amplifiers. These include the *maximum output sourcing* or *sinking current*, the *maximum output signal swing*, and the *slew rate*. Another characteristic of importance is the *settling time* defined as the amount of time the op amp requires in a given negative feedback configuration to respond to an input step and to settle to within a given percentage of the final value of the output step response.

The steps in designing an op amp depend on the desired values of these parameters. In this study we shall restrict ourselves to general purpose op amps that are implemented as part of an integrated circuit. Typical target specifications are shown in Table 6.5-1 for BJT and CMOS op amps. From these specifications we may propose several architectures.

The first possible op amp architecture is shown in Fig. 6.5-4*a* for the BJT op amp. This architecture is called the two-stage op amp. We observe that it consists of a differential amplifier similar to that of Fig. 6.3-11 cascaded with an inverter similar to that of Fig. 6.1-18*b*. The source of bias voltage for the differential amplifier current sink is also the source of bias voltage for the inverter's current-sink load. Two stages are often necessary because the differential amplifier generally has a voltage gain less then 60dB. The output resistance of the inverting amplifier is large and will not be capable of driving a low value of R_L. If the output resistance must be lower, then an output amplifier must be used, creating a third stage in the architecture.

TABLE 6.5-1
Typical specifications for integrated circuit BJT and CMOS op amps

Op amp specification	BJT	CMOS	Units
Differential gain, A_d	80	60	Decibels
Unity gain bandwidth, GB	1	1	Megahertz
Output resistance, r_{out}	1 K	100 K	Ohms
Input differential resistance, r_{id}	1 M	10^{12}	Ohms
Input offset voltage, V_{OS}	5	10	Millivolts
Input offset current, I_{OS}	100	-0	Nanoamperes
Power consumption, P_{DD}	10	5	Milliwatts
PSRR	80	80	Decibels
Phase margin (unity gain) (C_L = 20 pF)	60	60	Degrees
CMRR	100	100	Decibels
Slew rate (C_L = 20 pF)	± 1	± 1	Volts/microsecond
Settling time (C_L = 20 pF)	1	1	Microseconds

The two-stage architecture has the disadvantage of having two high-impedance nodes, which are indicated by A and B in Fig. 6.5-4*a*. This implies that two poles will be dominant, which will deteriorate the phase margin of the op amp. In order to resolve this situation, a Miller capacitance (C_c) is introduced between points A and B. The feedback path through C_c around the inverter causes these poles to split; it makes the pole at A dominant and for an appropriate value of C_c drives the pole at B out to or beyond GB. While this creates a single dominant pole, any large load capacitor will drive the pole at B back toward the origin, causing a poor phase margin.

The susceptibility of the Miller compensation scheme to capacitive loading has influenced the development of a second op amp architecture shown in Fig. 6.5-4*b*. This type of architecture is called the cascode configuration. A modification of this architecture, called the folded cascode configuration, is shown in Fig. 6.5-4*c*. In each of these cascode configurations, there is only one high-impedance node, which is at the output. The reason is that the input resistance of the cascode stage is very low ($1/g_m$), as was seen in Sec. 6.2. Since the gain of the cascode is approximately equal to that of the inverter, this is a very clever way of eliminating the high-impedance point at A of Fig. 6.5-4*a*. Compensation of the cascode op amp is accomplished by a capacitor connected from the output to ground. This has the attractive feature that as C_L increases, the compensation increases, keeping the op amp stable for large values of load capacitance.

Figure 6.5-5 shows the equivalent architectures for the CMOS op amp. The need for a second stage for the CMOS op amp is more obvious since the gain of a CMOS stage is typically less than that of an equivalent BJT stage. Although many other architectures for op amps exist, these represent the basic structures. They will aid in the designer's understanding of new or different architectures.

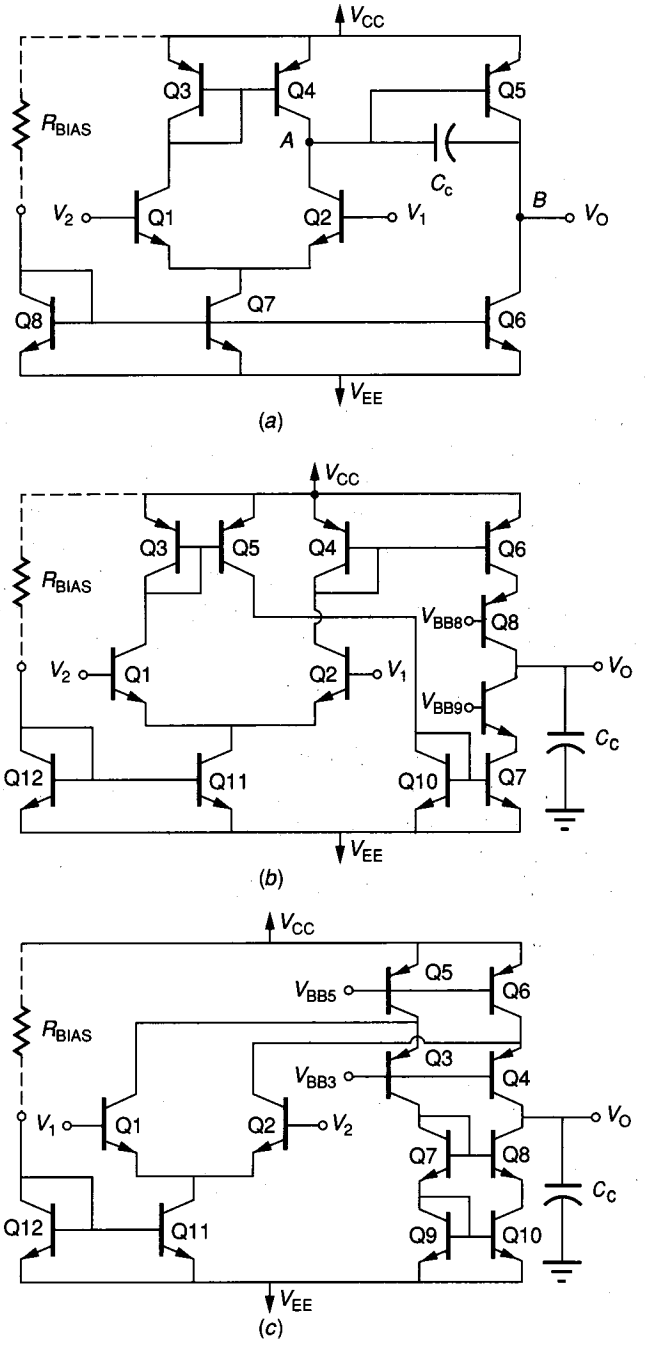
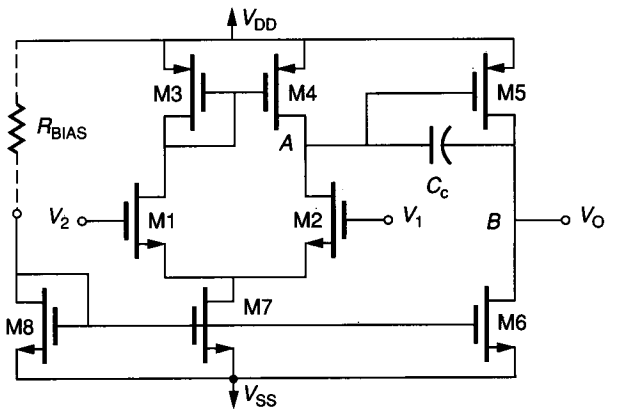
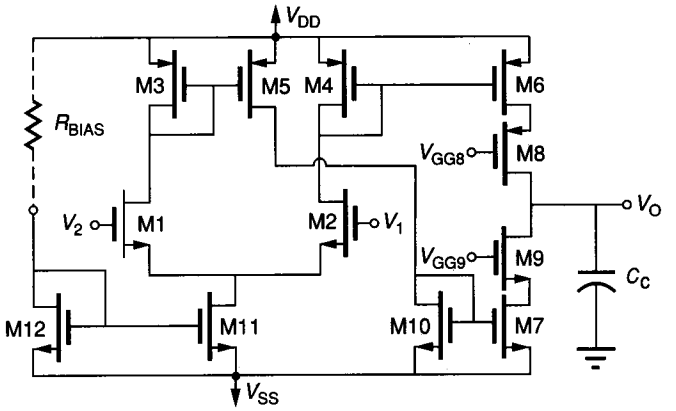


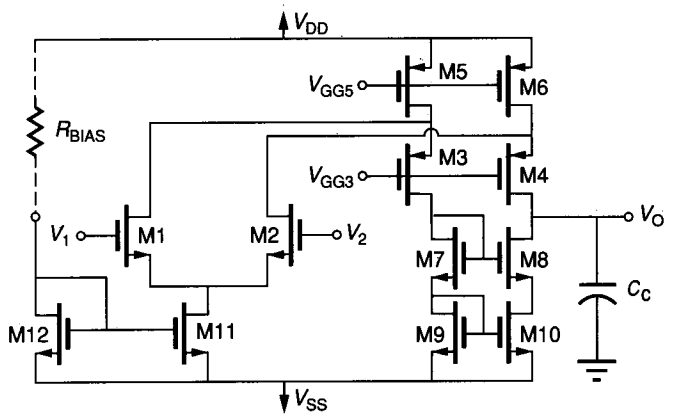
FIGURE 6.5-4
(*a*) Two-stage BJT op amp, (*b*) Cascode BJT op amp, (*c*) Folded cascode BJT op amp.



(a)



(b)



(c)

FIGURE 6.5-5
(*a*) CMOS two-stage op amp, (*b*) CMOS cascode BJT op amp, (*c*) CMOS folded cascode op amp.

6.5.2 The BJT Two-Stage Op Amp

The design of the two-stage BJT op amp will be considered first because it is the simplest.[1] Because the performance of the op amp is based on the small signal model, Fig. 6.5-6*a* shows the small signal model of the op amp of Fig. 6.5-4*a*. The first-stage model was developed in Fig. 6.3-15, where definitions of R_1, R_2, C_1, and C_2 are still valid, with the exception that $r_{\pi 5}$ is added in parallel to R_2, causing that resistance to be significantly decreased. The second stage in this model is simply that of an inverter. R_3 and C_3 are given as

$$R_3 = r_{o5} \parallel r_{o6} \tag{6.5-6}$$

and

$$C_3 = C_{\mu 5} + C_{\mu 6} + C_{CS5} + C_{CS6} + C_L \tag{6.5-7}$$

In order to simplify our considerations, assume that ω_1 and ω_1' of Eq. 6.3-84 approximately cancel and that $g_{m3} \simeq g_{m4}$. The resulting small signal, differential-input model for the two-stage BJT op amp is shown in Fig. 6.5-6*b* where $v_{id} = v_i - v_2$. The parameters of this model are defined as

$$g_{mI} = g_{m1} = g_{m2} \tag{6.5-8}$$

$$R_I = R_2 = r_{o2} \parallel r_{o4} \parallel r_{\pi 5} \tag{6.5-9}$$

$$C_I = C_2 = C_{\mu 2} + C_{\mu 4} + C_{\pi 5} + C_{CS2} + C_{CS4} \tag{6.5-10}$$

$$g_{mII} = g_{m5} \tag{6.5-11}$$

$$R_{II} = R_3 = r_{o5} \parallel r_{o6} \tag{6.5-12}$$

and

$$C_{II} = C_3 = C_{\mu 5} + C_{\mu 6} + C_{CS5} + C_{CS6} + C_L \tag{6.5-13}$$

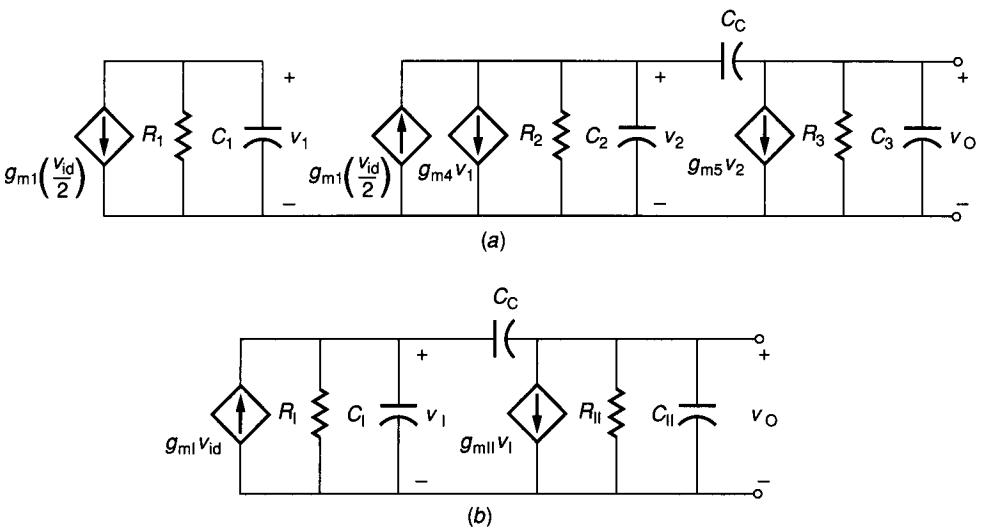


FIGURE 6.5-6
(*a*) Small signal model of Fig. 6.5-4*a* or Fig. 6.5-5*a*, (*b*) Simplified model of (*a*).

C_c is the compensation capacitance and is not included in C_I or C_{II}.

Analysis of the circuit of Fig. 6.5-6*b* illustrates how the Miller capacitor, C_c, splits the poles and accomplishes the dominant pole compensation. If C_c is zero, then the transfer function $V_O(s)/V_{ID}(s)$ is given as

$$\frac{V_O(s)}{V_{ID}(s)} = \frac{g_{mI}R_I g_{mII}R_{II}\omega_I'\omega_{II}'}{(s + \omega_I')(s + \omega_{II}')} = \frac{A_o\omega_I'\omega_{II}'}{(s + \omega_I')(s + \omega_{II}')} \tag{6.5-14}$$

where

$$\omega_I' = -p_I' = \frac{1}{R_I C_I} \tag{6.5-15}$$

and

$$\omega_{II}' = -p_{II}' = \frac{1}{R_{II}C_{II}} \tag{6.5-16}$$

p_I' and p_{II}' are the pole locations of Fig. 6.5-4*a* when C_c is zero.

When C_c is not zero, then the transfer function of Eq. 6.5-14 becomes

$$V_O(s)/V_{ID}(s) = A_o\left[1 - (sC_c/g_{mII})\right] \Big/ \Big\{ 1 + s\left[R_I(C_I + C_{II}) + R_{II}(C_{II} + C_c) + g_{mII}R_I R_{II}C_c\right] + s^2 R_I R_{II}\left[C_I C_{II} + C_c(C_I + C_{II})\right] \Big\} \tag{6.5-17}$$

Applying Eq. 6.1-26 to Eq. 6.5-17 gives

$$p_I \simeq \frac{-1}{g_{mII}R_I R_{II}C_c} \tag{6.5-18}$$

and

$$p_{II} \simeq \frac{-g_{mII}C_c}{C_I C_{II} + C_{II}C_c + C_I C_c} \tag{6.5-19}$$

Also, the zero introduced by C_c is located at

$$z = \frac{g_{mII}}{C_c} \tag{6.5-20}$$

Figure 6.5-7 summarizes these results. Figure 6.5-7*a* shows how the poles at $-p_I'$ and $-p_{II}'$ have been split into the poles at $-p_I$ and $-p_{II}$. C_c also creates a zero in the right-half plane (RHP). The effects of the RHP zero can be ignored for the BJT two-stage op amp. Figure 6.5-7*b* shows a possible form of the magnitude of the frequency response if GB $< p_{II} < z$. It is important to note that the BJT op amp will have $|p_{II}'|$ less than $|p_I'|$ if the input resistance to Q5 is not increased. Often a Darlington is used in place of Q5 for this purpose.

The preceding analysis of the BJT two-stage op amp can be summarized as follows. The low-frequency open-loop gain is given as

$$A_o = g_{mI}g_{mII}R_I R_{II} \tag{6.5-21}$$

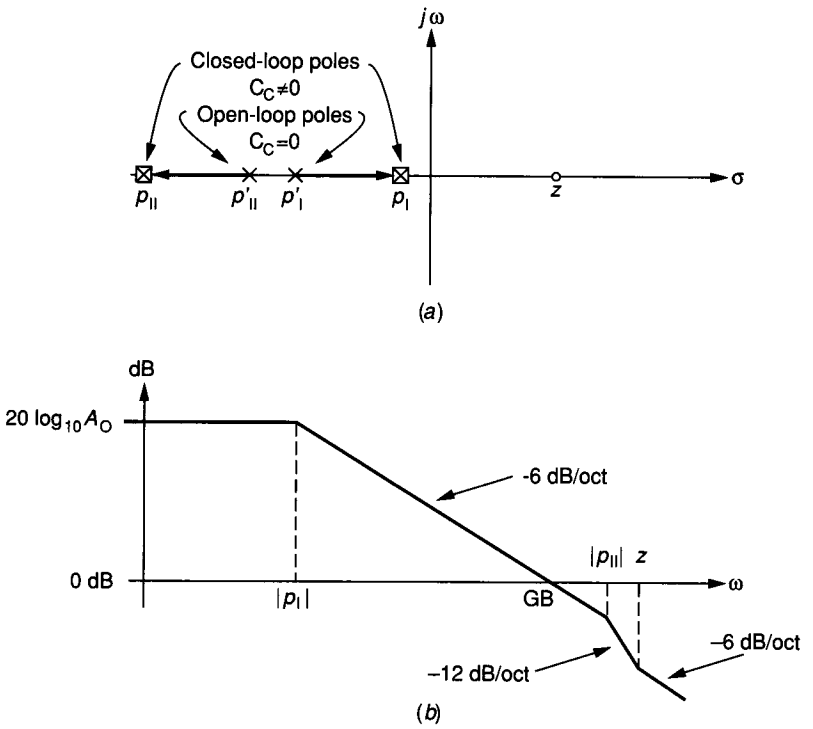


FIGURE 6.5-7
(*a*) Open- and closed-loop roots of Fig. 6.5-6*b*, (*b*) Closed-loop magnitude response of Fig. 6.5-6*b*.

The dominant pole is given by

$$| p_I | \simeq \frac{1}{g_{mII} R_I R_{II} C_c} \tag{6.5-22}$$

The unity-gain bandwidth, GB, is found by the product of Eqs. 6.5-21 and 6.5-22 and is

$$\text{GB} = \frac{g_{mI}}{C_c} \tag{6.5-23}$$

These three relationships form the basis of the two-stage op amp design along with two other constraints, which are developed below. For good phase margin, it is desirable to have $z > | p_{II} |$ and $| p_{II} | > \text{GB}$. From these two constraints, we get

$$g_{mII} > g_{mI} \tag{6.5-24}$$

and

$$C_{II} < \frac{g_{mII}}{g_{mI}} C_c \tag{6.5-25}$$

The design approach for the BJT two-stage op amp will be to establish the bias currents in the first and second stages of Fig. 6.5-4*a* to meet the specification for A_o and maintain the constraints of Eqs. 6.5-24 and 6.5-25. C_c will be chosen to meet the specification for GB. Replacing the small signal model parameters in terms of dc currents and device characteristics results in the following key equations which give a reasonable phase margin.

$$A_o \simeq \frac{g_{mI} g_{mII} r_{\pi 5}}{g_{o5} + g_{o6}} = \frac{\beta_{F5}/V_t}{1/V_{AN} + 1/V_{AP}} \left(\frac{I_{C1}}{I_{C5}} \right) \tag{6.5-26}$$

$$GB = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{I_{C1}}{V_t C_c} \tag{6.5-27}$$

$$\frac{g_{mII}}{g_{mI}} = \frac{g_{m5}}{g_{m1}} = \frac{I_{C5}}{I_{C1}} \tag{6.5-28}$$

To illustrate the design of a BJT two-stage op amp, we will assume that the desired specifications are $A_o \geq 10,000$ and GB $\simeq$ 1 MHz. Obviously, there are many other specifications of the op amp, as illustrated in Table 6.5-1, but we will start with these two. Assuming that $\beta_{FN} \simeq 200$, $\beta_{FP} \simeq 50$, $V_{AFN} \simeq 100$ V, and $V_{AFP} \simeq 50$, Eq. 6.5-26 becomes

$$A_o = 66,700 \left(\frac{I_{C1}}{I_{C5}} \right) \tag{6.5-29}$$

Choosing $I_{C5} = 5I_{C1}$ gives $A_o = 13,340$. Picking $C_c = 30$ pF gives $I_{C1} \simeq 5$ μA from Eq. 6.5-27. Thus, $I_{C5} \simeq 25$ μA. From these currents we can calculate the differential input resistance as $r_{id} \simeq 2r_{\pi 1} = 2$ MΩ and the output resistance as $r_{out} = 1.334$ MΩ. The slew rate is determined by how fast C_c can be charged and discharged. This is given by the expression

$$\text{Slew rate} = \text{SR} = \frac{I}{C_c} \tag{6.5-30}$$

where I is the smaller of $2I_{C1}$ or I_{C5}. In this example, the slew rate of the op amp is $2I_{C1}/C_c = 0.33$ V/μs. It is seen that the design of the BJT two-stage op amp is simple but constrained in its ability to simultaneously satisfy many op amp specifications. The performance is satisfactory for most applications, with the possible exception of the high output resistance. The choices that were made in this design example can be varied to achieve different values of specifications.

Up to this point, the design of the BJT two-stage op amp has not depended on the geometries of the individual devices. In other words, while Q1 and Q2 should be matched and Q3, Q4, and Q5 should be matched, there is no geometric relationship between them. The sizes of Q6, Q7, and Q8 determine the currents. Generally, a resistor is connected from the collector of Q8 to V_{CC} to establish I_{C8}. This current will be dependent on power supply variations, leading to a poor PSRR. To improve the PSRR, the current for I_{C8} must be provided by one of the current sources of Sec. 5.3. When I_{C8} is defined, the ratio of the emitter areas of Q6, Q7, and Q8 can be used to define I_{C7} ($=I_{C1}/2$) and I_{C6} ($=I_{C5}$). It is

important to keep each BJT operating in the forward active region for the best performance and largest signal swings. The sizing of the emitter areas depends on the application. Devices in the input (Q1 and Q2) and in all current mirrors should be as large as possible for matching without degrading the frequency response. The remaining device areas should be as small as possible if power dissipation is not a concern.

After an initial design has been obtained by the method illustrated, the next step is to use a simulator such as SPICE that permits the designer to consider second-order effects and examine the influence of parameter and process variation. This step is important since it gives the designer a good understanding of the performance of the op amp and of how to make tradeoffs using the computer to achieve the final design specifications.

6.5.3 The CMOS Two-Stage Op Amp

Let us consider next the design of the two-stage CMOS op amp shown in Fig. 6.5-5*a*. Since the small signal model of Fig. 6.5-6 holds for the CMOS case, Eqs. 6.5-21 through 6.5-25 are also valid. The values of R_I, R_{II}, C_I, and C_{II} for the CMOS case are given as

$$R_I = r_{ds2} \parallel r_{ds4} \tag{6.5-31}$$

$$R_{II} = r_{ds5} \parallel r_{ds6} \tag{6.5-32}$$

$$C_I = C_{gd2} + C_{gd4} + C_{gs5} + C_{db2} + C_{db4} \tag{6.5-33}$$

and

$$C_{II} = C_{gd6} + C_{db5} + C_{db6} + C_L \tag{6.5-34}$$

The key equations pertaining to the CMOS two-stage op amp design are given as

$$\begin{aligned} A_o &= g_{mI} g_{mII} R_I R_{II} = \frac{g_{m1} g_{m5}}{(g_{ds2} + g_{ds4})(g_{ds5} + g_{ds6})} \\ &= \left[\left(\frac{1}{\lambda_2 + \lambda_4}\right)\left(\frac{2K'_N W_1}{I_{D1} L_1}\right)^{1/2}\right]\left[\left(\frac{1}{\lambda_5 + \lambda_6}\right)\left(\frac{2K'_P W_5}{I_{D5} L_5}\right)^{1/2}\right] \\ &\simeq \frac{1}{2\lambda^2}\left(\frac{K'_N K'_P W_1 W_5}{I_{D1} I_{D5} L_1 L_5}\right)^{1/2} \end{aligned} \tag{6.5-35}$$

$$\text{GB} = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{1}{C_c}\left(\frac{2K'_N W_1 I_{D1}}{L_1}\right)^{1/2} \tag{6.5-36}$$

and

$$\frac{g_{mII}}{g_{mI}} = \frac{g_{m5}}{g_{m1}} = \left[\frac{K'_N I_{D1}(W_1/L_1)}{K'_P I_{D5}(W_5/L_5)}\right] \tag{6.5-37}$$

Comparing Eqs. 6.5-35 through 6.5-37 with Eqs. 6.5-26 through 6.5-28 reveals a very important difference between BJT and CMOS integrated circuits. This difference is that the performance of the CMOS op amp is dependent on the geometry of the devices, whereas the BJT op amp is independent of the geometry of its transistors. While this creates additional complexity in the expressions, the designer has much more freedom to meet the specifications of the design.

The additional degrees of freedom allow the designer to impose constraints that will ensure that all MOS devices operate in saturation over wide process variations. In Sec. 5.4, we showed how the ratio of the W/L values of two MOS devices connected gate-to-gate and source-to-source could control the ratio of the drain currents. This principle is employed in the circuit of Fig. 6.5-5*a* to ensure that M4 operates in saturation. All other devices either operate in saturation by their connection or by external potentials applied to the inputs or outputs. For matching and symmetry, we must choose $W_1/L_1 = W_2/L_2$ and $W_3/L_3 = W_4/L_4$. If we force V_{GS3} to be equal to V_{GS5} by the following relationship

$$\frac{W_3}{L_3} = \frac{W_5}{L_5}\left(\frac{I_3}{I_5}\right) \tag{6.5-38}$$

then since $I_5 = I_6$, $I_3 = I_4$, and $W_3/L_3 = W_4/L_4$, we may express Eq. 6.5-38 as

$$\frac{W_4}{L_4} = \frac{W_5}{L_5}\left(\frac{I_4}{I_6}\right) \tag{6.5-39}$$

However, because $I_4 = 0.5I_7$ and $I_7/I_8 = (W_7/L_7)/(W_8/L_8)$, the condition for M4 to remain in saturation becomes

$$\frac{W_4}{L_4} = \frac{(W_5/L_5)}{2}\left(\frac{W_7/L_7}{W_6/L_6}\right) = \frac{(W_5/L_5)}{2}\left(\frac{I_7}{I_6}\right) \tag{6.5-40}$$

To illustrate the design of a two-stage CMOS op amp such as that given in Fig. 6.5-5*a*, assume that the desired specifications are $A_o \geq 50{,}000$, GB $= 1$ MHz, and the slew rate is 2 V/μs. Assume that the device parameters are $K'_N = 2K'_P = 25\ \mu\text{A/V}^2$, $\lambda = 0.01\ \text{V}^{-1}$ and $C_c = 5$ pF. From the slew rate specification and C_c, we see that $I_{D1} = 5\ \mu$A. We will pick I_{D5} equal to 50 μA to make the zero due to Miller compensation larger than the second pole. Solving for W_1/L_1 in Eq. 6.5-36 gives $W_1/L_1 \simeq 4.0$. Since M1 and M2 are matched, W_2/L_2 is also 4.0. In Eq. 6.5-35 we may solve for W_5/L_5 to get 4.5. Since the ratio of current in M6 and M7 is I_{D5} to $2I_{D1}$, we may solve for W_4/L_4 from Eq. 6.5-40 as being 10 times less than W_5/L_5, or 0.45. Finally, one can solve for the value of W_8/L_8 necessary to establish a reasonable current in M8 and solve for W_6/L_6 and W_7/L_7 using the current ratios. The small signal input resistance, R_{id}, of the CMOS op amp is infinity because of the infinite gate resistance. The output resistance is equal to the parallel combination of r_{ds5} and r_{ds6} and is 1 MΩ for this example.

At this point, the circuit designer typically sets the smaller value of W or L equal to perhaps twice the smallest allowable value and solves for the remaining dimension. For a minimum L or W of 5 μ, Table 6.5-2 gives a set of possible

TABLE 6.5-2
A set of first-cut W and L values for the design of a CMOS two-stage op amp such as that shown in Fig. 6.6-5*a*

	M1	M2	M3	M4	M5	M6	M7	M8
W (μ)	40	40	10	10	45	10	10	10
L (μ)	10	10	22	22	10	10	50	10

W and L values for the op amp of Fig. 6.5-5*a* if the current in M8 is 50 μA when $W_8/L_8 = 1$. At this point, the designer would turn to a simulator to refine and optimize the design.

Unfortunately, the transconductance of the MOS device is not as large as for the BJT, which causes a problem due to the zero of Eq. 6.5-20. Using the values of the preceding example, we find that the zero is located at 2.39 MHz (the RHP zero for the BJT two-stage op amp was at 10.6 MHz). This RHP zero will destroy the phase margin of the CMOS two-stage amplifier. Figure 6.5-8 shows a clever way to eliminate this zero and to make the two-stage CMOS op amp of Fig. 6.5-5*a* practical. It can be shown that the new zero location is given by

$$z' = \frac{1}{C_c[(1/g_{mII}) - R_z]} \tag{6.5-41}$$

With the nulling resistor, the designer can conceptually move the RHP zero to infinity; in fact, the zero can be moved into the left-hand plane and used for lead compensation. R_z is typically implemented by an n-channel and p-channel transistor in parallel with the gates taken to the appropriate power supply. For our example of the two-stage CMOS op amp, g_{m5} was 75 μS; therefore, a value of $R_z = 13.33$ kΩ would move the RHP zero to infinity and retrieve the good stability properties. The same nulling resistor technique can be applied to the two-stage BJT op amp if necessary.

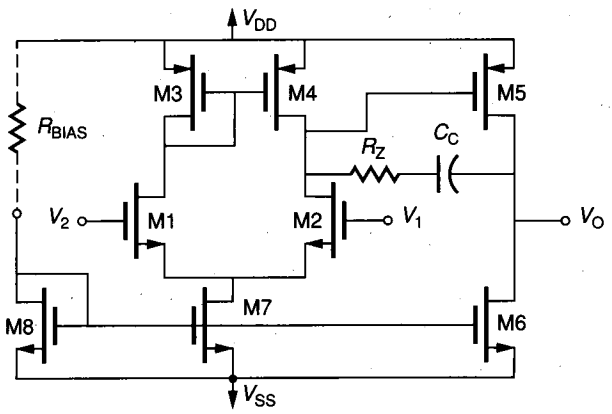


FIGURE 6.5-8
Nulling method to remove the effects of the RHP zero due to low device transconductance.

6.5.4 Cascode Op Amps

If the load to an op amp is primarily capacitive, it is not necessary to use a low resistance output stage to achieve satisfactory performance because large output currents are only required under dynamic conditions. The difficulty with a capacitive load for the two-stage op amp is that it destroys the Miller compensation and eventually causes the op amp to become unstable if C_L is too large or the closed-loop gain of the op amp approaches unity. In this case, the cascode architectures shown in Fig. 6.5-4 and Fig. 6.5-5 are very useful. Consider the BJT cascode op amp of Fig. 6.5-4*b*. The current from the collector of Q1 is mirrored into the collector current of Q7 while the collector current of Q2 is mirrored into the collector current of Q6. These currents are applied to the common-base configuration of Q8 and Q9. Q6 and Q8 and Q7 and Q9 are cascode amplifiers, as will be recognized from Sec. 6.2. The differential currents are combined at the collectors of Q8 and Q9, resulting in a single-ended output voltage, V_O. The important feature of the circuit of Fig. 6.5-4*b* is that the high-impedance point at A in Fig. 6.5-4*a* is no longer present. Since the output resistance is very high, the compensation can be accomplished by a capacitor connected from the output to ground. This means that a large load capacitance, C_L, will simply provide more compensation, keeping the op amp circuit stable. The low-frequency gain of the BJT cascode op amp is similar to that of the two-stage BJT op amp because the gain of the cascode stage is approximately equal to the gain of the inverter stage.

The BJT folded cascode op amp of Fig. 6.5-4*c* uses the same principle as the BJT cascode op amp to eliminate the high-impedance point at A, thus achieving a configuration with the high-impedance point at the output of the op amp. In this architecture, Q1-Q3 and Q2-Q4 form the cascode pairs. It is necessary to use a cascode current mirror (Q7 through Q10) to maintain the high output resistance of this configuration. The folded cascode is useful in acheiving a wide common-mode input voltage range.

In many cases, the two-stage BJT op amp is satisfactory for driving moderate values of C_L because of the higher values of g_m for a BJT. The higher value of g_m pushes the RHP zero away from the origin and keeps C_L from having a strong influence on the stability of the op amp. However, the CMOS cascode configurations of Fig. 6.5-5*b* and *c* are often used because of the low g_m of the MOS devices compared with that of the BJT devices. Another reason for using the cascode architecture is due to PSRR performance. It can be shown that variations in the upper power supply for the two-stage architecture couple through the base-emitter of Q5 (gate-source of M5) and C_c to the output, resulting in poor PSRR performance. The cascode configurations do not have this problem, which was another motivation for their development.

To understand the performance of the cascode op amp configuration in more detail, consider the folded cascode CMOS op amp of Fig. 6.5-5*c*. Figure 6.5-9*a* shows a small signal model for this op amp. The bulk effects of all devices whose source is not on ground have been ignored. r'_{in}, r'_{out} and the current-controlled current source, i, represent the cascode mirror consisting of M7 through M10 (see Sec. 5.4). Figure 6.5-9*b* is a simplified version of Fig. 6.5-9*a* using the technique

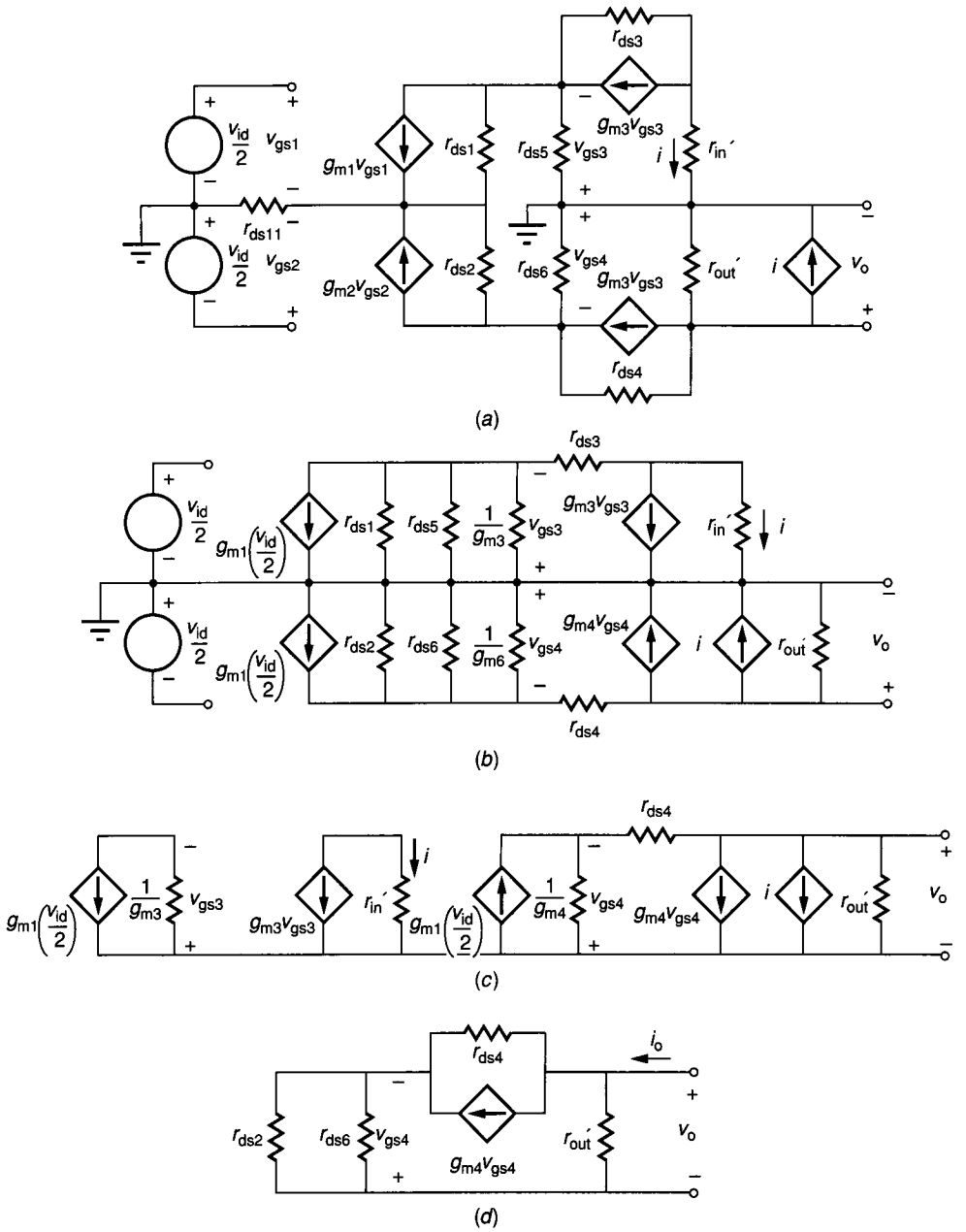


FIGURE 6.5-9
(*a*) Small signal model of the CMOS folded cascode op amp, (*b*) Simplification of (*a*), (*c*) Approximate model of (*b*), (*d*) Model for calculating the output resistance.

illustrated in Sec. 6.3 for the differential amplifier of Fig. 6.3-4*c*. Neglecting r_{ds} as compared to $1/g_m$ results in the approximate small signal model of the circuit of Fig. 6.5-5*c* shown in Fig. 6.5-9*c*. Analysis of this circuit shows that the low-frequency voltage gain is

$$\frac{v_o}{v_{id}} = A_o \simeq g_{m1} r'_{out} \simeq g_{m1} g_{m8} r_{ds8} r_{ds10} \tag{6.5-42}$$

where r'_{out} was given by simplication of Eq. 5.3-10. Assuming that all *W/L* ratios are unity, $K'_N = 2K'_P = 25\ \mu A/V^2$, $\lambda_N = \lambda_P = 0.01\ V^{-1}$, and $I_{D1} = I_{D2} = 5\ \mu A$, the dc current in M5 through M9 (M6 through M10) is 50 μA and the low-frequency gain, A_o, is 22,361. The output resistance of the circuit of Fig. 6.5-5*c* can be found with the assistance of the circuit of Fig. 6.5-9*d*. r_{out} is found as

$$\begin{aligned} r_{out} &= r'_{out} \,||\, r_{ds4}\left[1 + (1 + g_{m4} r_{ds4}) \frac{r_{ds2} r_{ds4}}{r_{ds2} + r_{ds4}}\right] \\ &\simeq (g_{m8} r_{ds8} r_{ds10}) \,||\, [(g_{m4} r_{ds4})(r_{ds2} \,||\, r_{ds4})] \end{aligned} \tag{6.5-43}$$

Using these values for the folded cascode CMOS op amp, we find that r_{out} is equal to 78.3 MΩ.

The frequency performance of the folded cascode CMOS op amp is simply given as

$$\frac{V_O(s)}{V_{ID}(s)} \simeq \frac{A_o \omega_I}{s + \omega_I} = \frac{GB}{s + \omega_I} \tag{6.5-44}$$

where ω_I is given as

$$\omega_I = \frac{1}{R_{out} C_L} \tag{6.5-45}$$

C_L is the total capacitance attached to the output of the folded cascode CMOS op amp. The slew rate is found as

$$SR = \frac{I}{C_L} \tag{6.5-46}$$

where I is I_{D11} of Fig. 6.5-5*b* or *c*. The performance of this op amp can be evaluated with the assistance of Eqs. 6.5-42 through 6.5-46. Continuing with the preceding assumptions, we find that for GB = 5 MHz, the value of C_L is 9.1 pF. This gives a slew rate of about 1.1 V/μs. Of course, the *W/L* values can be used to modify the design to achieve different specifications.

One of the disadvantages of this architecture is that the output signal swing is limited by the cascode configuration. This swing limitation can be alleviated using the technique described for cascode current mirrors (see Fig. 5.4-10). A practical implementation of the folded cascode CMOS op amp is shown in Fig. 6.5-10.[2] With ±5 V power supplies, the op amp has an output swing of ±4.1 V. It has a low-frequency gain of 5000, a GB of approximately 5 MHz, and a PSRR in the range of 60–70 dB. The input offset voltage, V_{OS}, is ±6 mV. In the basic

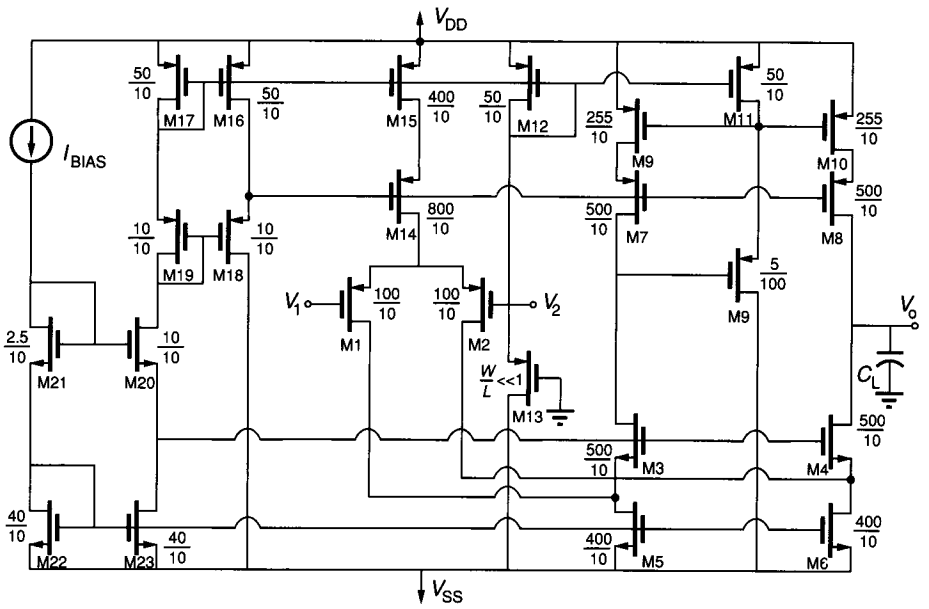


FIGURE 6.5-10
Folded cascode CMOS op amp design. *W/L* values are in microns.

folded cascode architecture of Fig. 6.5-5*c*, the operating region of all devices can be defined by external voltages so that ratio constraints are not necessary. In choosing the *W/L* values, one of the primary considerations is to increase the signal swings. The *W/L* values of the circuit of Fig. 6.5-10 correspond to $K'_N = 23.6\ \mu A/V^2$, $K'_P = 5.84\ \mu A/V^2$, $V_{TN} = 0.79$ V, $V_{TP} = -0.52$ V, $\gamma_N = 0.526\ V^{1/2}$, $\gamma_P = 0.67\ V^{1/2}$, $\lambda_N = 0.0207\ V^{-1}$, and $\lambda_P = 0.0121\ V^{-1}$.

6.5.5 Op Amps with an Output Stage

None of the op amps considered so far are capable of driving low values of load resistance. If the application requires a low output resistance, then the two-stage op amp can be followed with an output amplifier by use of the concepts of Sec. 6.4. Figure 6.5-11 shows the combination of the BJT two-stage op amp of Fig. 6.5-4*a* with the output stage of Fig. 6.4-14*b* to obtain an op amp with the ability to drive a low value of R_L. Q6 and Q7 are used to determine the operating current in the push-pull output transistors, Q8 and Q9. One of the difficulties in adding an output stage is to decide whether or not to include the output stage within the Miller compensation. The two choices are indicated in Fig. 6.5-11 by C_{c1} and C_{c2}. C_{c2} is less desirable because the pole due to the output stage will be large and close to GB, resulting in three poles inside the compensation loop. The Miller compensation method does not work well in this situation because complex conjugate poles can be created. The ability of the output stage to drive

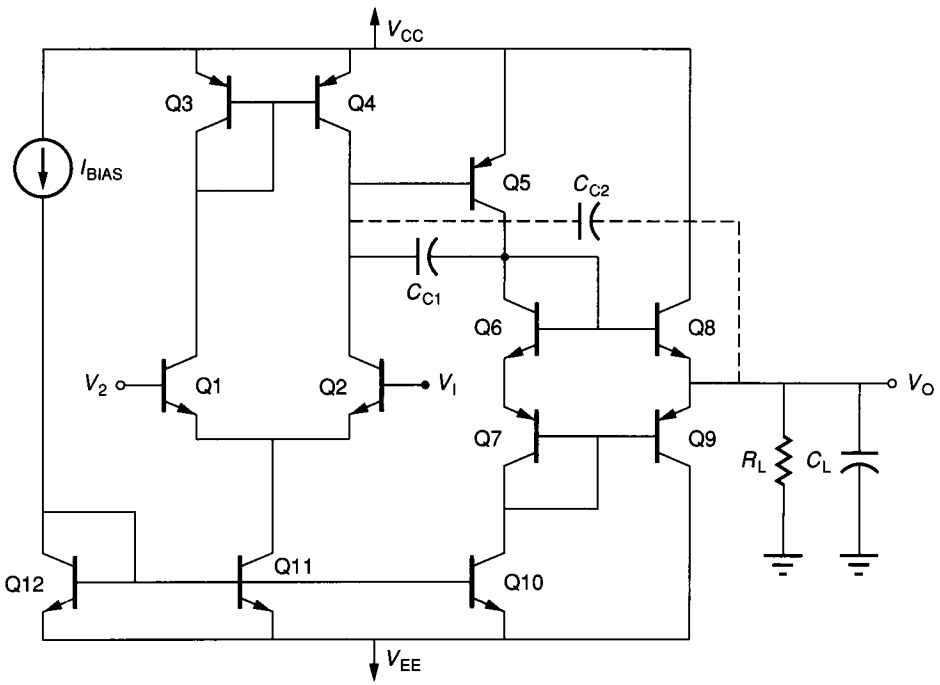


FIGURE 6.5-11
BJT two-stage op amp with a push-pull output stage.

a load resistance has been discussed in the preceding section. Further information can be found in the references.[3–7]

Figure 6.5-12*a* shows a two-stage CMOS op amp with an output stage similar to that of Fig. 6.4-14*a*. The compensation capacitor does not include the output stage and uses a nulling resistor, R_z, to achieve good stability properties. The ability to sink or source current is determined by the second stage of the op amp (M5). The bias current in the output devices (M8 and M9) should be chosen to reduce the crossover distortion and keep the quiescent dissipation low. Also, the bias current in the output devices will determine the small signal value of output resistance. The output swing of this op amp will be limited due to the body effects, causing V_T to increase as the positive or negative rail is approached by the output voltage.

Figure 6.5-12*b* shows use of the substrate BJT to create an output stage. This technique will provide low small signal output resistance because of the large value of g_m for the BJT. Unfortunately, the BJT suffers from the inability to source current for large positive output swings. Because the output devices are of a different type and in a different configuration (emitter follower and common source), the sourcing and sinking currents will be difficult to match. In addition, this configuration will create appreciable distortion.

A better solution to the output stage problem for the CMOS op amp is to couple the circuits of Fig. 6.4-15*a* and Fig. 6.5-10 resulting in the

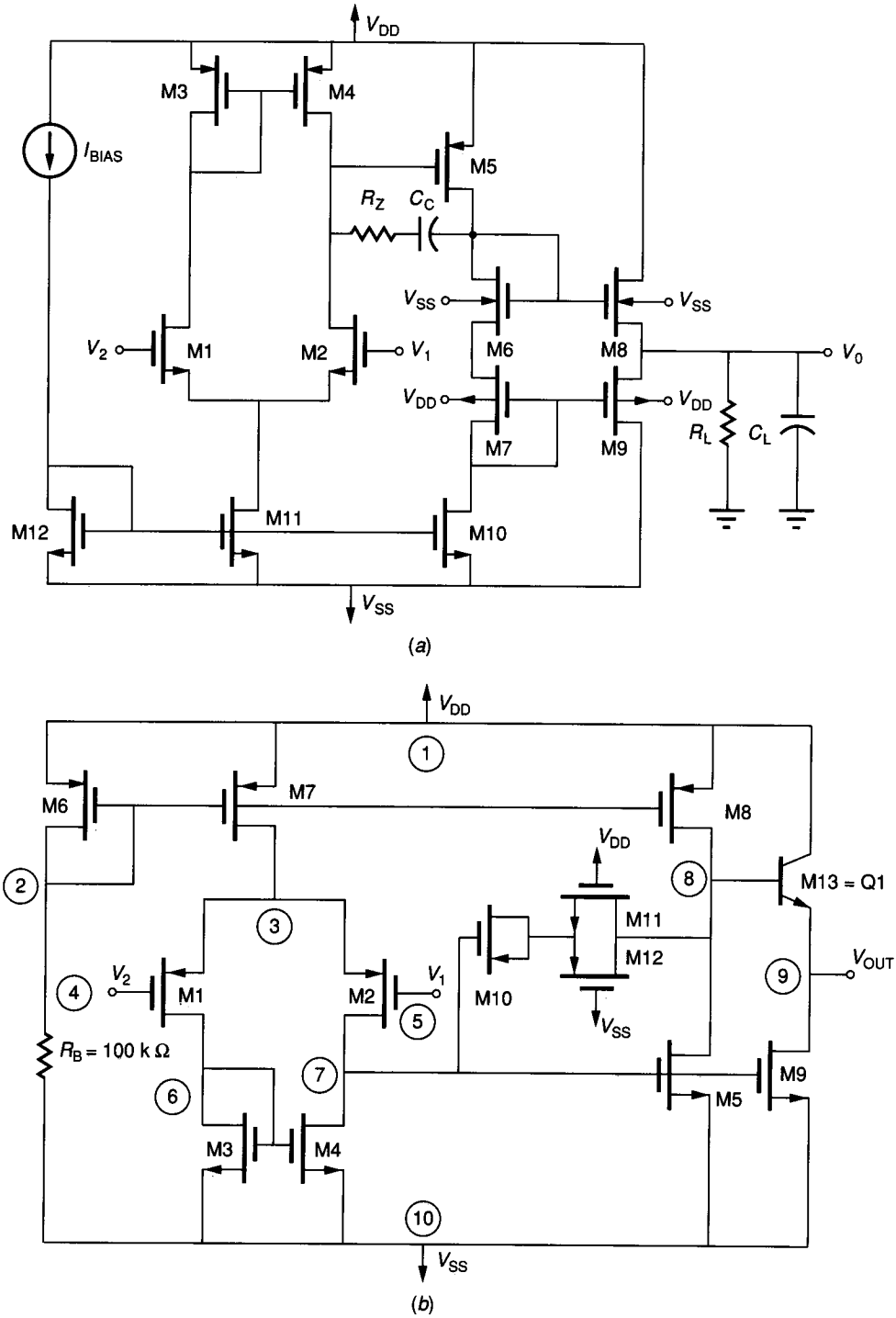


FIGURE 6.5-12
(*a*) CMOS two-stage op amp with a push-pull output stage, (*b*) CMOS two-stage op amp with a substrate BJT used in the output stage.

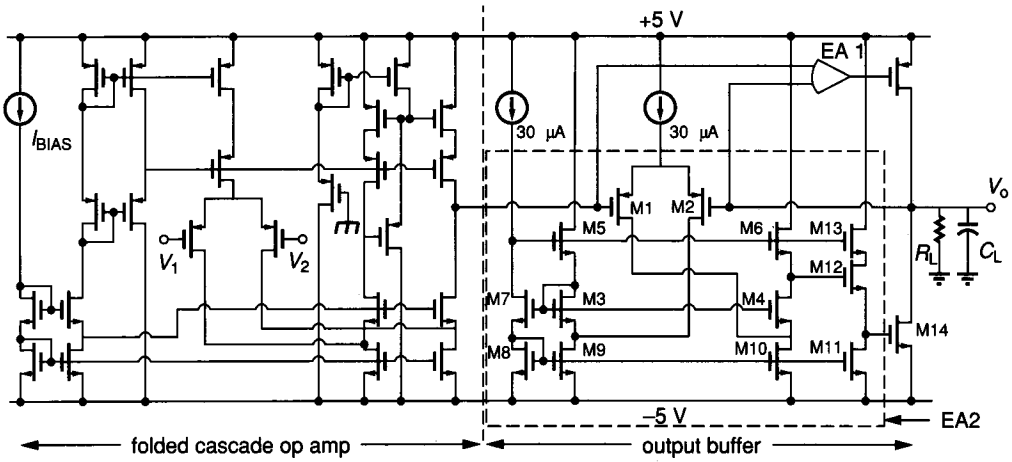


FIGURE 6.5-13
Folded cascode CMOS op amp with output buffer.

arrangement of Fig. 6.5-13. Only one of the error amplifiers is shown in this figure. The resulting CMOS op amp has an output resistance of 300 Ω and achieves an output signal swing of approximately −4.3 V to +3.5 V for ±5 V power supplies and a load of 2000 Ω and 100 pF. Total power dissipation of the op amp and buffer stage is 5 mW for ±5 V supplies.

6.5.6 Simulation and Measurement of Op Amps

It has been mentioned that the next step after developing a first-cut design of an op amp is simulation. This is a key step in the successful design of an op amp. Another important step is the actual measurement of the op amp when it is fabricated. Because the considerations necessary for the simulation and testing are so closely related, they will be considered simultaneously. One of the more important characterizations of op amp performance is operation in the open-loop mode. However, as it is difficult to measure an op amp in its open-loop mode, it is also difficult to simulate an op amp in the open-loop mode. The reason for this difficulty is the high differential gain of the op amp. Figure 6.5-14 shows how this step might be performed. V_{off} is an external voltage whose value is

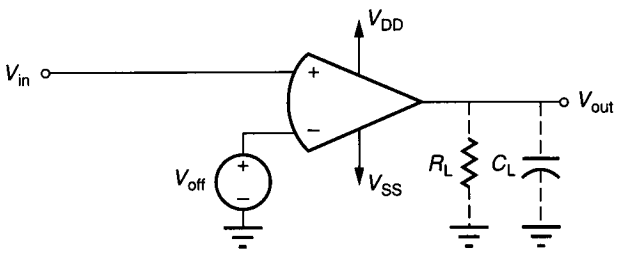


FIGURE 6.5-14
Open-loop mode with offset compensation.

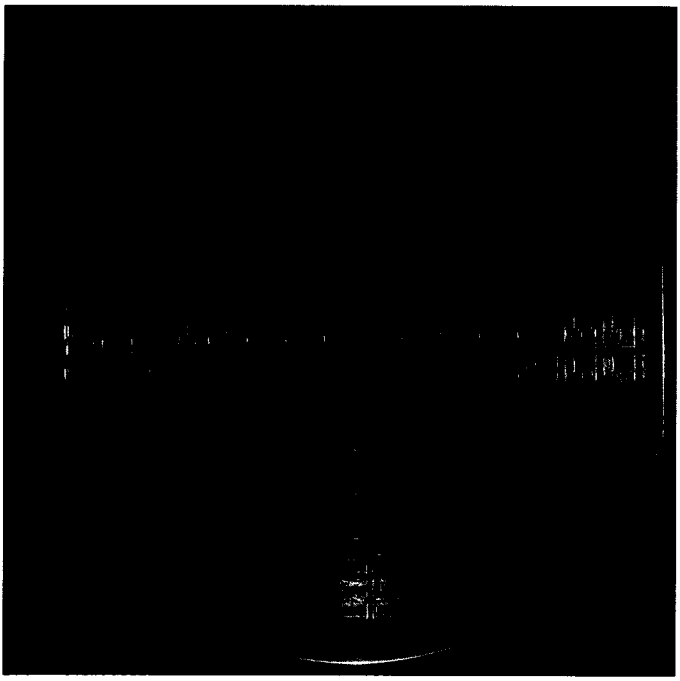


PLATE ONE Wafer photo — Motorola 68000 Family Microprocessor
(Photo courtesy of Motorola, Inc.)

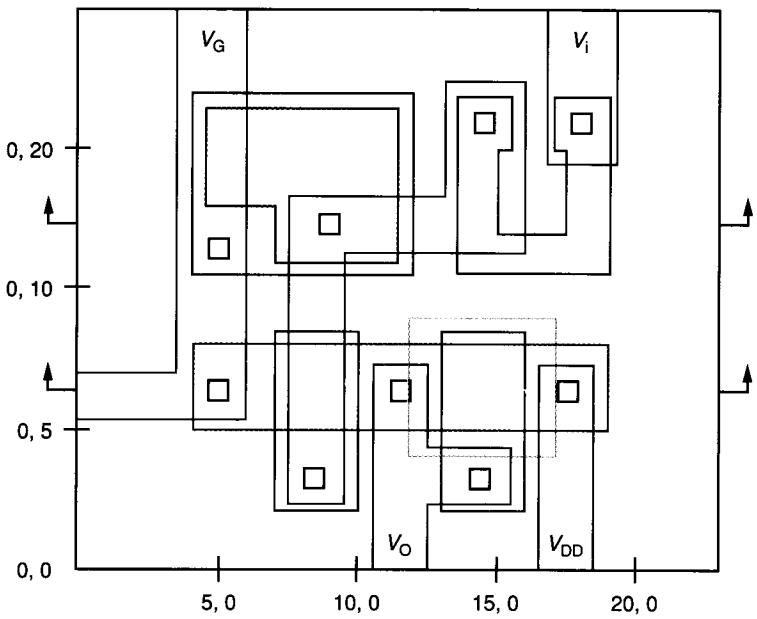
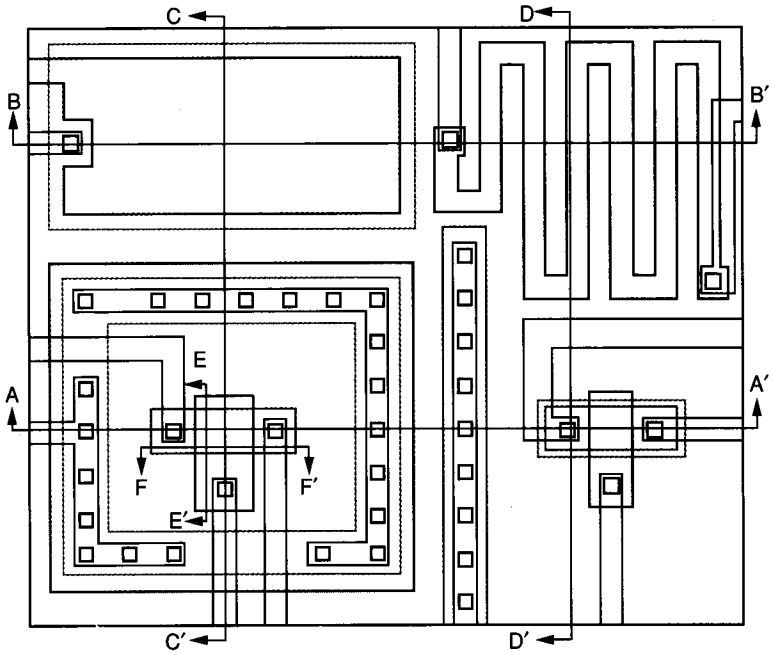
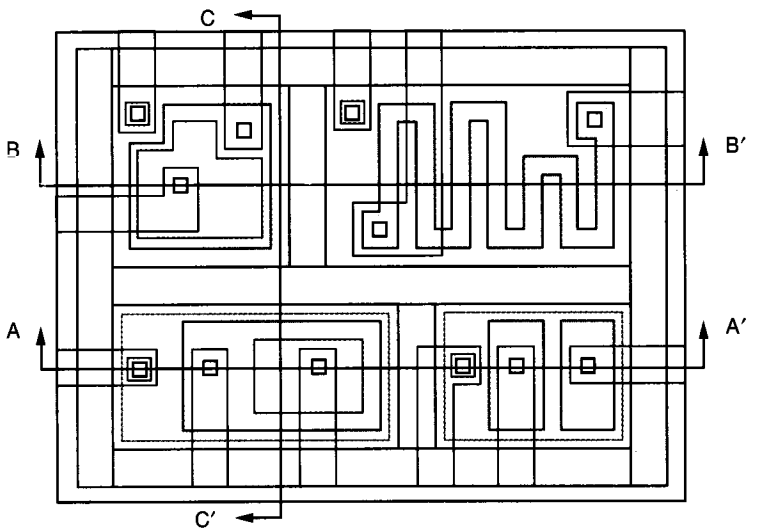


PLATE TWO Layout for NMOS process



Top view (a) Fig. 2b.1a

PLATE THREE Layout for CMOS process



Top view of Bipolar Die (Fig. 2c.1a)

PLATE FOUR Layout for Bipolar process

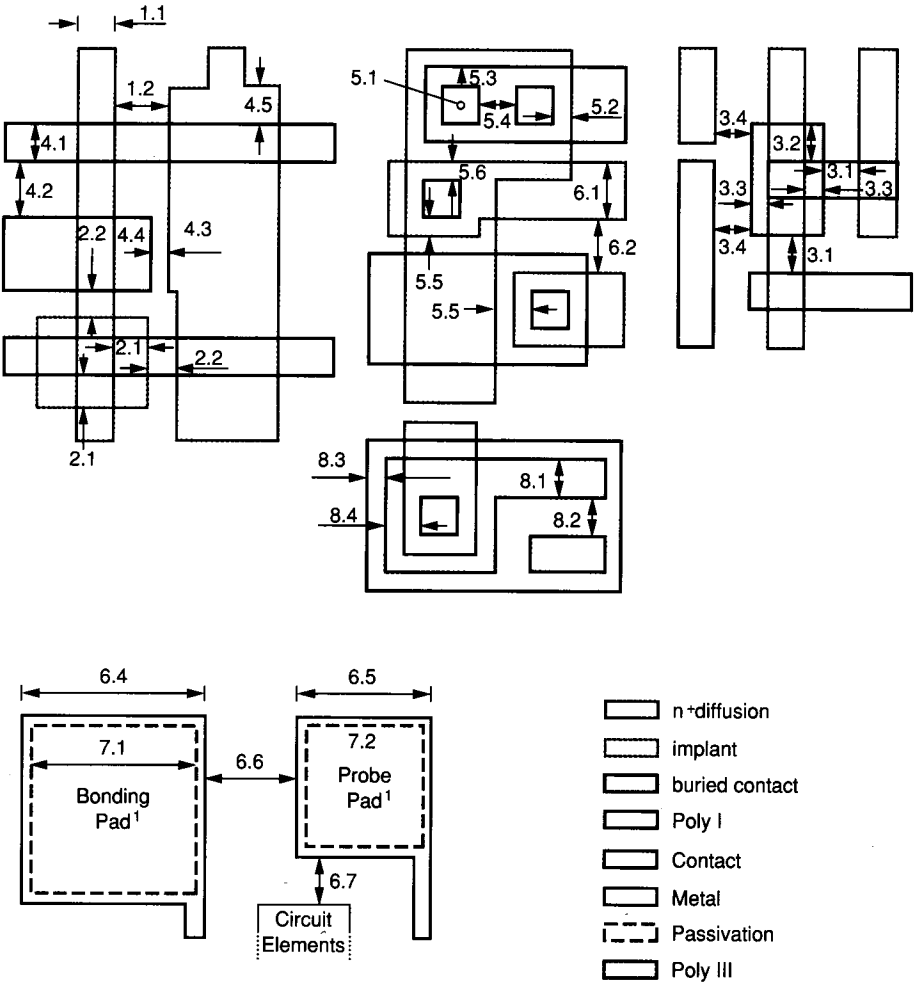


PLATE FIVE Table 2A.3 Graphical interpretation of NMOS design rules of Table 2A.2

[1]Scale for pads is much smaller than scale for other features depicted in this figure.

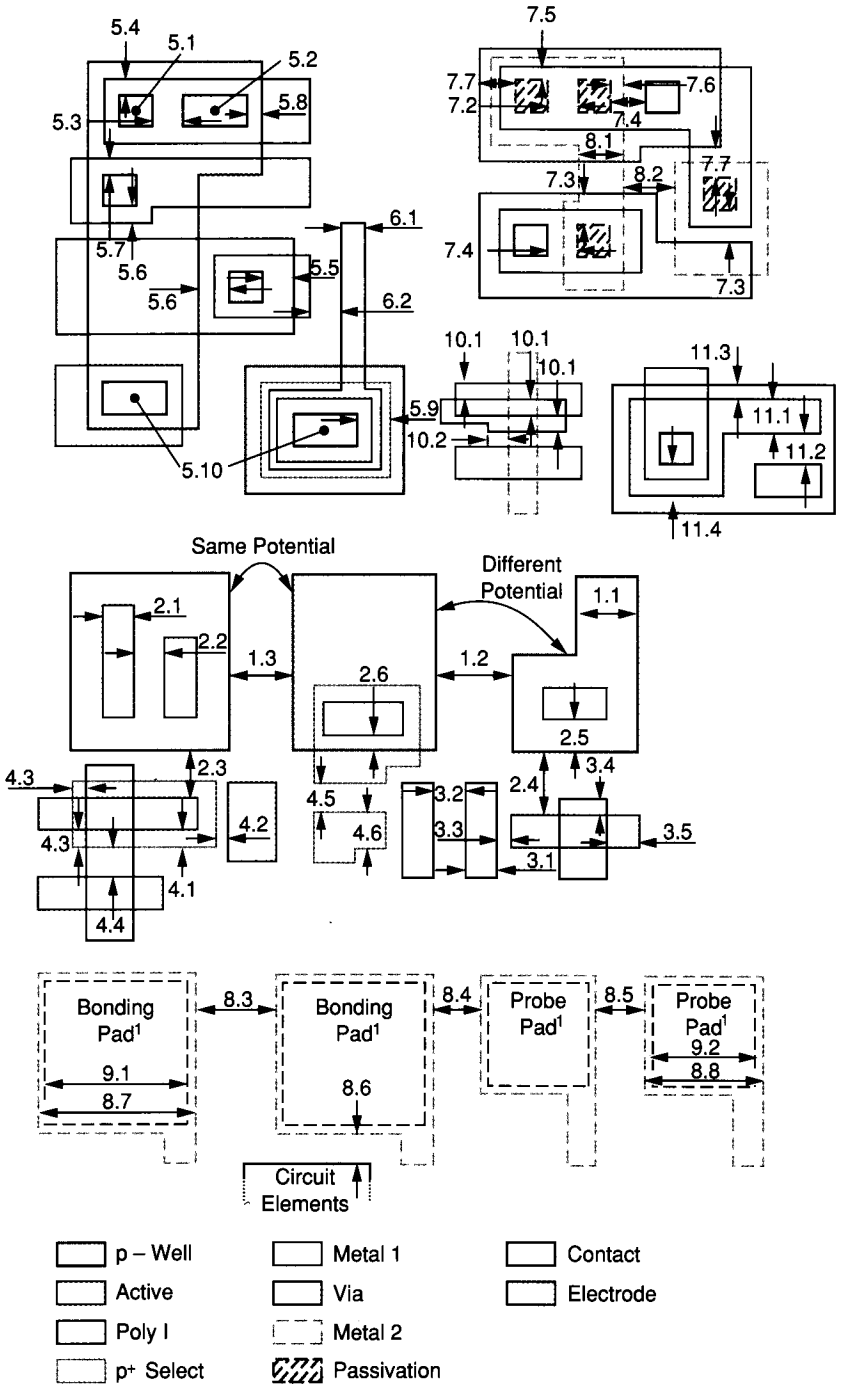


PLATE SIX Table 2B.3 Graphical interpretation of CMOS design rules of Table 2B.2

[1] Scale for pads is much smaller than scale for other features depicted in this figure.

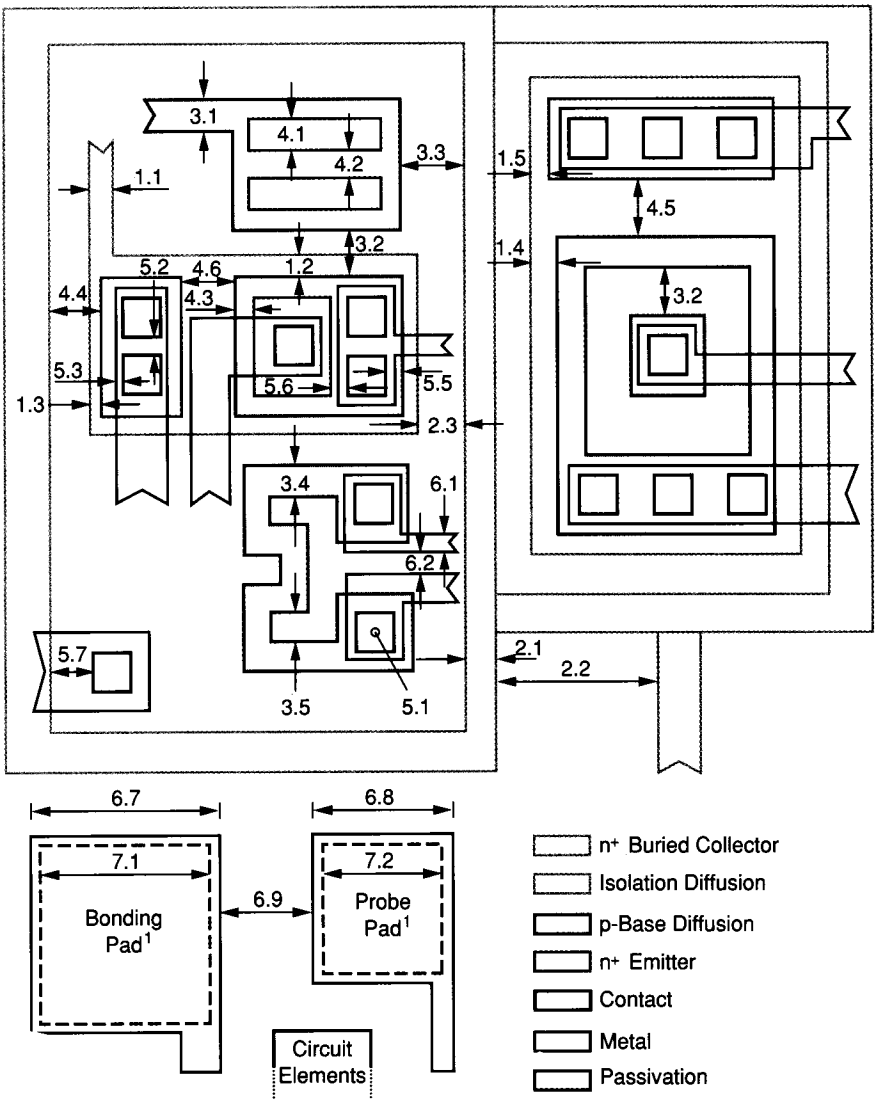


PLATE SEVEN Table 2C.3 graphical interpretation of Bipolar design rules of Table 2C.2

[1] Scale for pads is much smaller than scale for other features depicted in this figure.

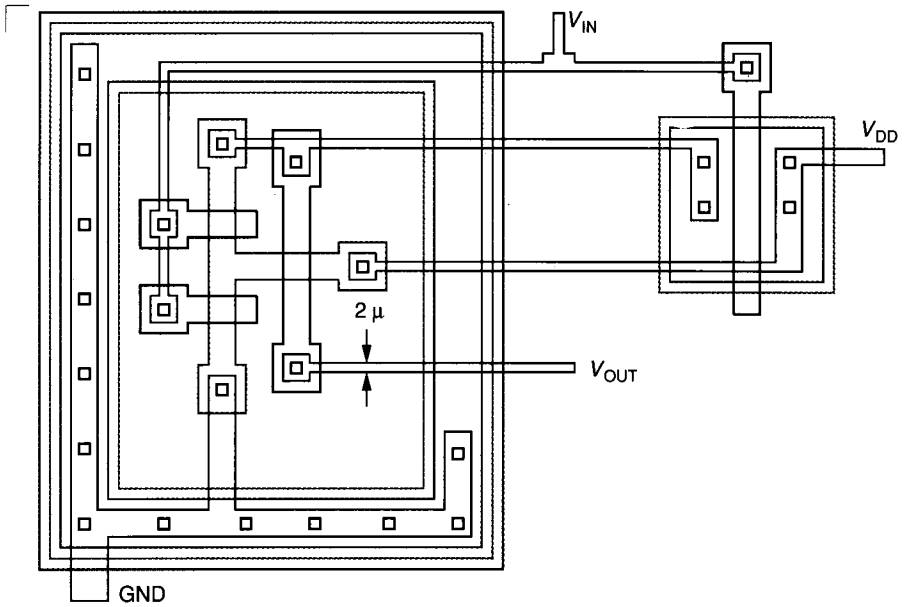


PLATE EIGHT Layout of Schmitt Trigger circuit (see Problem 2.20)

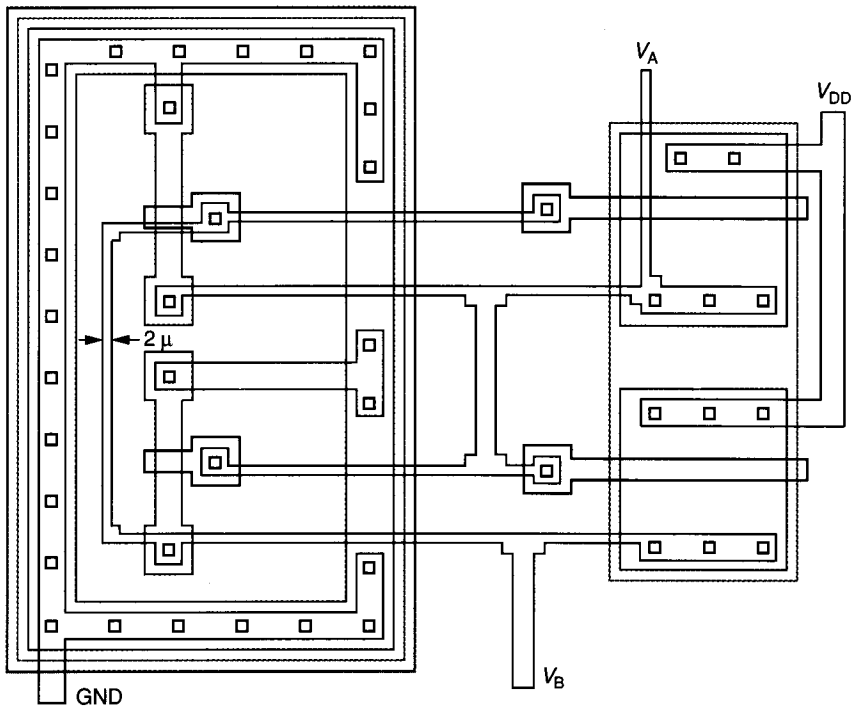


PLATE NINE Layout of latch circuit (see Problem 2.23)

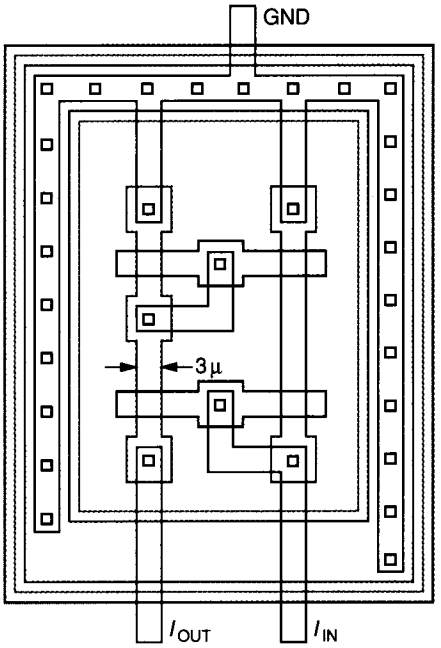


PLATE TEN Layout of common source amplifer (see Problem 2.22)

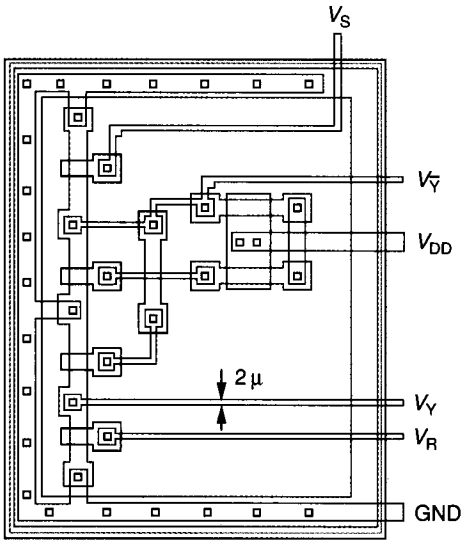


PLATE ELEVEN Layout of flip flop (see Problem 2.23)

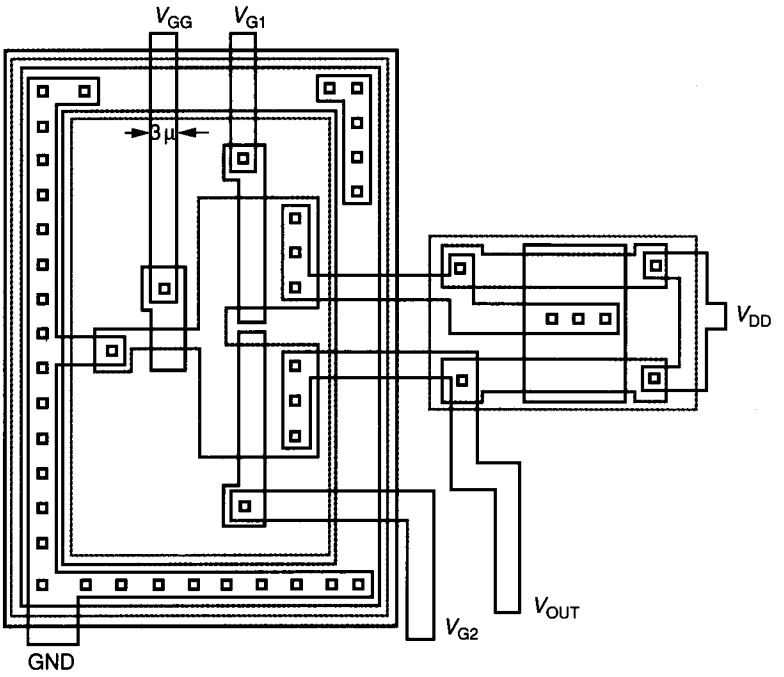


PLATE TWELVE Layout of differential amplifier with error (see Problem 2.31)

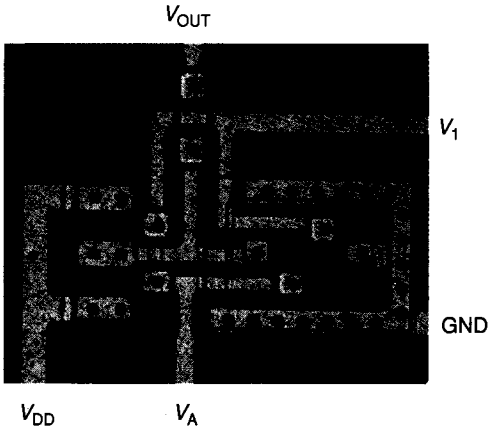


PLATE THIRTEEN Die photo of logic circuit (see Problem 2.26)

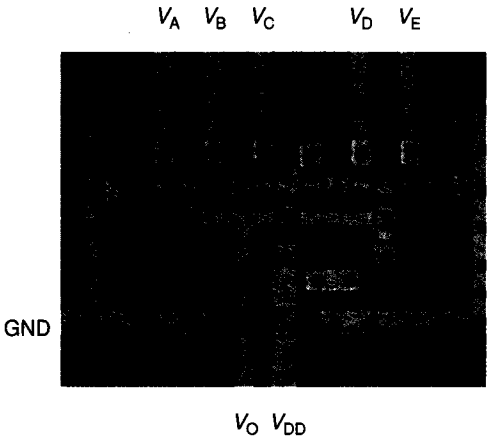


PLATE FOURTEEN Die photo of logic circuit (see Problem 2.26)

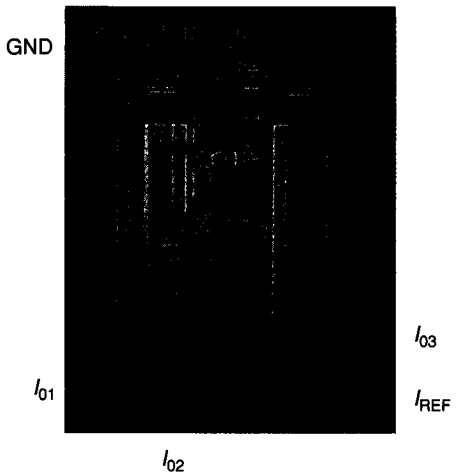


PLATE FIFTEEN Die photo of current source (see Problem 2.27)

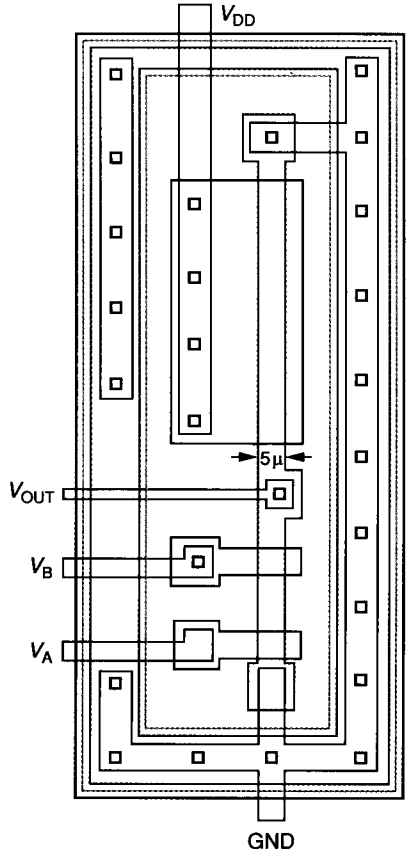


PLATE SIXTEEN Layout of NAND circuit with error (see Problem 2.29)

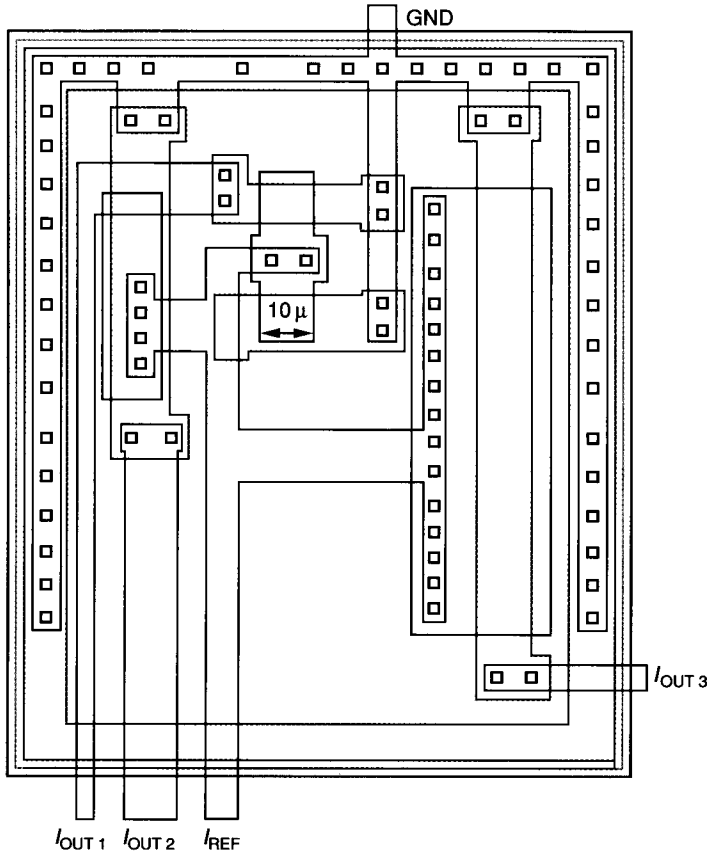


PLATE SEVENTEEN Layout of current source with error (see Problem 2.30)

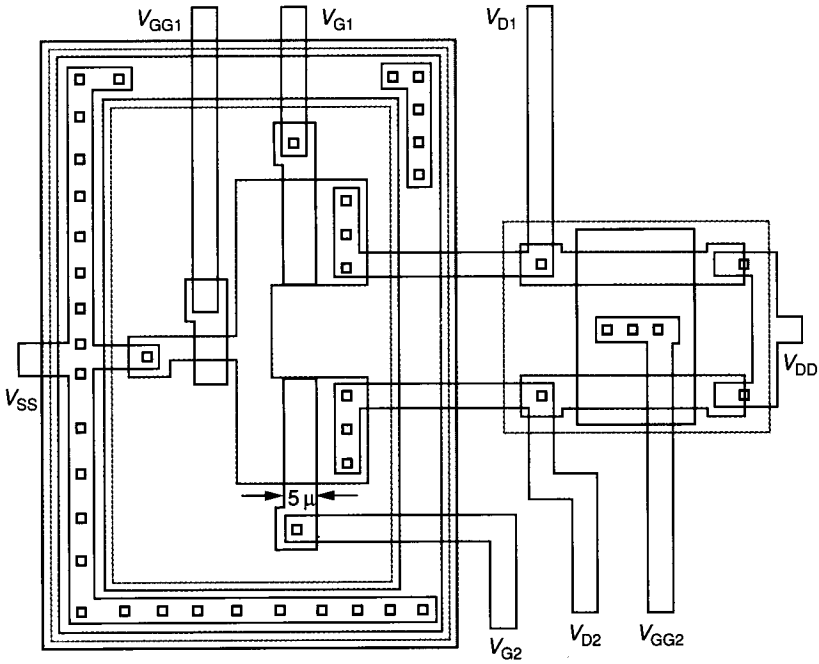


PLATE EIGHTEEN Layout of differential amplifier with error (see Problem 2.31)

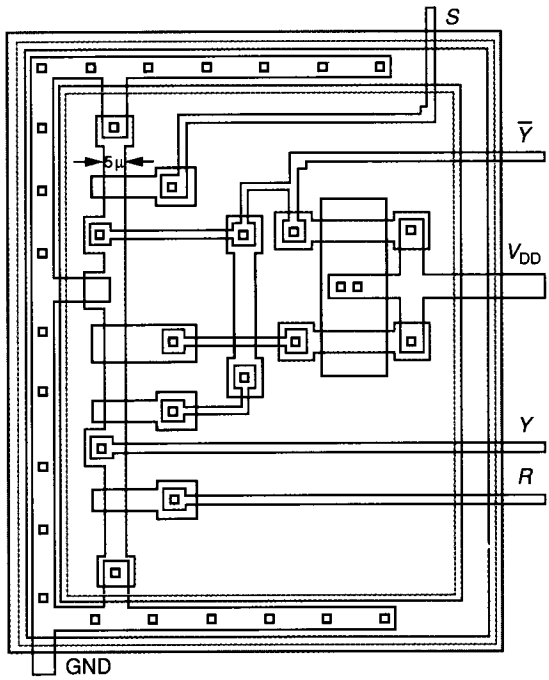


PLATE NINETEEN Layout of flip-flop with error (see Problem 2.32)

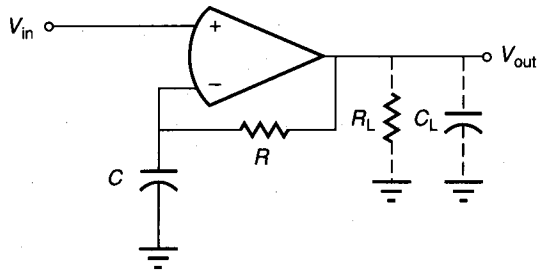


FIGURE 6.5-15
A method of measuring open-loop characteristics with dc bias stability.

adjusted to keep the dc value of V_{OUT} between the power supply limits. Without V_{off}, the op amp output will be at the positive or negative power supply for either the measurement or simulation case. The resolution necessary to find the correct value of V_{off} usually escapes the novice designer. It is necessary to find V_{off} to the accuracy of the magnitude of the power supply voltage divided by the low-frequency differential gain (typically in the range of millivolts).

The approach proposed in Fig. 6.5-14 to measure the open-loop gain is only practical for simulation. A better method of measuring the open-loop gain is shown in the circuit of Fig. 6.5-15. In this configuration, it is necessary to select the reciprocal *RC* time constant to be about 10 to 100 times less than the anticipated dominant pole of the op amp. Under these conditions, the op amp has total dc feedback, which stabilizes the bias. The dc value of V_{OUT} will be exactly the dc value of V_{IN}. The true open-loop frequency response characteristics will not be observed until the frequency is approximately 10 times $1/RC$. Above this frequency, the ratio of V_{OUT} to V_{IN} is essentially the open-loop gain of the op amp. This method works well for both simulation and measurement.

Simulation or measurement of the open-loop configuration of the op amp will characterize the open-loop transfer curve, the open-loop output swing limits, the phase margin, the dominant pole, the unity-gain bandwidth, and other open-loop characteristics. The designer should connect the anticipated loading at the output in order to get meaningful results. In some cases where the open-loop gain is not too large, it can be measured by applying v_{in} in Fig. 6.5-16 and measuring v_{out} and v_i. In this configuration, one must be careful that R is large enough not to cause a dc current load on the output of the op amp.

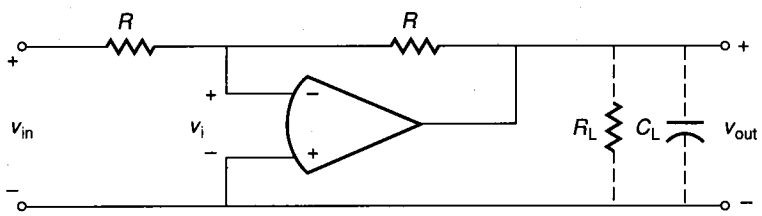


FIGURE 6.5-16
Configuration for simulating the open-loop frequency response for moderate-gain op amps.

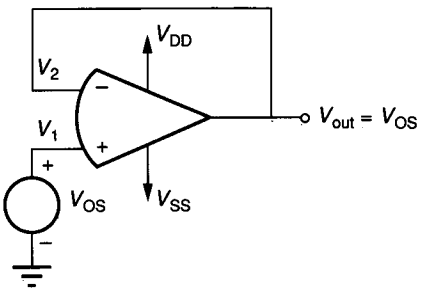


FIGURE 6.5-17
Configuration for measuring the input offset voltage.

The dc input offset voltage, V_{OS}, can be measured using the circuit of Fig. 6.5-17. If the dc input offset voltage is too small, it can be amplified by the use of a resistor divider in the negative feedback path. Figure 6.5-17 is also a good configuration for measuring or simulating the input common-mode range. Figure 6.5-18 shows the anticipated unity-gain transfer characteristic of the op amp in Fig. 6.5-17, illustrating the input common-mode range.

The common-mode gain is most easily simulated using the circuit of Fig. 6.5-19. It is seen that if V_{off} fails to keep the op amp in the linear region, this measuring configuration will fail. An alternate method of measuring the common-mode gain is given in Fig. 6.5-20. This circuit can be used to measure the CMRR, which will also give the common-mode gain. The method involves a sequence of two steps. The first step is to set V_{HH} to V_{HH} + 1 V, V_{LL} to V_{LL} + 1 V, and V_{out} to 1 V by applying -1 V to the input designated as $-V_{out}$. This is equivalent to applying a common-mode input signal of 1 V to the amplifier with the nominal supply values. The value at V_{OFF} is measured and designated as V_{OFF1}. Next, V_{HH} is set to $V_{HH} - 1$ V, V_{LL} to $V_{LL} - 1$ V, and V_{out} to -1 V

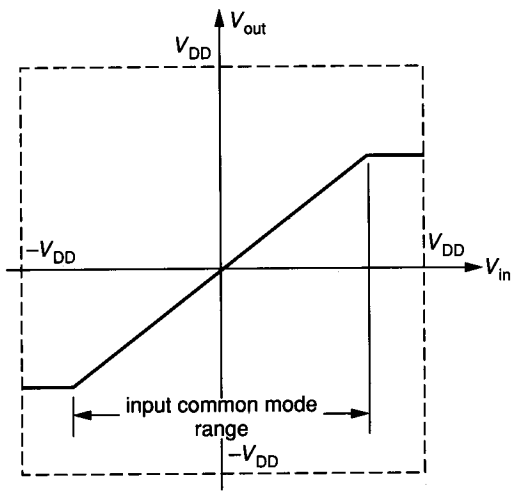


FIGURE 6.5-18
Unity-gain transfer function of the op amp.

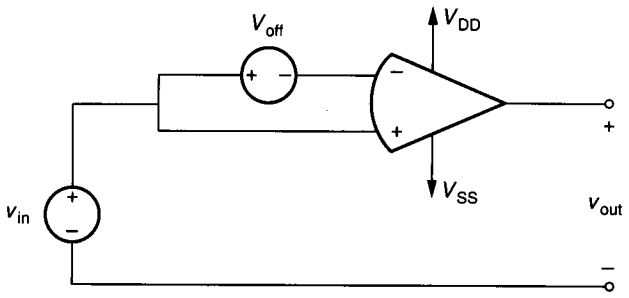


FIGURE 6.5-19
Configuration for simulating the common-mode gain.

by applying +1 V to the input designated as $-V_{out}$. V_{OFF} is measured and designated as V_{OFF2}. The CMRR can be found by

$$\text{CMRR} = \frac{2000}{|\, V_{OFF1} - V_{OFF2} \,|} \tag{6.5-47}$$

This measurement is a spot measurement and must be modified to obtain the frequency response of the CMRR. The modification involves placing small sinusoidal signals of the proper phase in series with the power supplies.

The configuration of Figure 6.5-20 can also be used to measure the PSRR. First, set V_{HH} to V_{HH} + 1 V and V_{out} to 0 V by grounding $-V_{out}$. In this case, V_i is the input offset voltage for V_{HH} + 1 V. Measure V_{OFF} under these conditions, and designate it as V_{OFF3}. Next, set V_{HH} to V_{HH} − 1 V and V_{out} to 0 V, and measure V_{OFF}, designated as V_{OFF4}. The PSRR of the V_{HH} supply is given as

$$\text{PSRR of } V_{HH} = \frac{2000}{|\, V_{OFF3} - V_{OFF4} \,|} \tag{6.5-48}$$

For the PSRR of V_{LL}, change V_{LL} and keep V_{HH} constant while V_{out} is at 0 V.

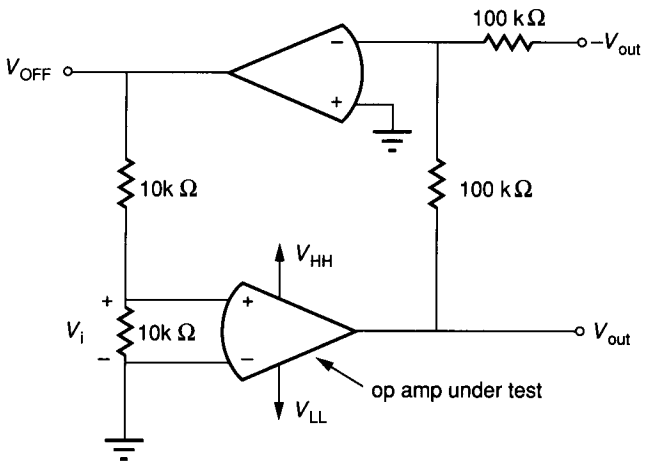


FIGURE 6.5-20
Circuit used to measure CMRR and PSRR.