The circuit of figure 6.5-17 can also be used to measure the PSRR of the positive or negative power supply. Assume that the output voltage can be expressed as

$$V_{out} = A_{vd}(V_1 - V_2) + A_{dd}V_{dd} \tag{6.5-49}$$

where A_{dd} is the small signal voltage gain from V_{dd} to V_{out}. It can be shown that

$$V_{out} = \frac{A_{dd}V_{dd}}{1 + A_{vd}} \simeq \frac{A_{dd}}{A_{vd}}V_{dd} = \frac{V_{dd}}{\text{PSRR}} \tag{6.5-50}$$

if $A_{vd} > 1$. Therefore, applying an ac signal V_{dd} in series with V_{DD} of Fig. 6.5-17 and measuring (or simulating) V_{out} will give the value of 1/PSSR.

The last configuration we will consider is for the large signal transient response. Figure 6.5-21*a* shows a configuration suitable for measuring the transient response of the op amp. Figure 6.5-21*b* shows a typical transient response. Both the positive and negative slew rates and the positive and negative settling times can be obtained from this configuration.

Other configurations not considered here include tests for noise, tolerances, process parameter variations, temperature, etc. The primary objective of any configuration is to keep the op amp in the desired region of operation and to maximize the accuracy of the measurement/simulation data.

The design of BJT and CMOS op amps has been introduced in this section. The basic two-stage architectures were introduced. The first-cut design of BJT and CMOS two-stage op amps was illustrated. This step should be followed by an extensive simulation of the design and the optimization of its performance. The CMOS two-stage op amp is unable to drive large capacitive loads, which led to the introduction of the cascode architectures. An example of a first-cut design for a CMOS folded cascode op amp was presented. This was followed by the addition of an output stage to permit the op amp to drive low resistive loads. Finally, the configuration and techniques useful in simulating and measuring the performance of op amps has been discussed.

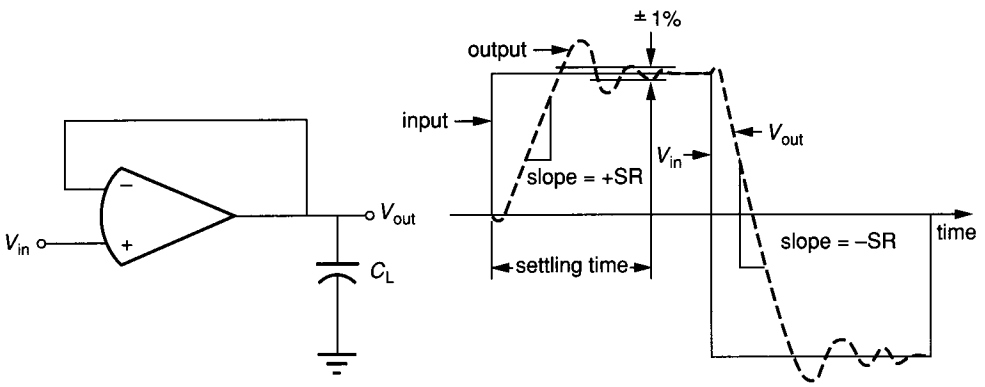


FIGURE 6.5-21
Measurement/simulation of slew rate and settling time.

The reader should be cautioned that the material presented was selected to give an appreciation for, and an introduction to, the subject of integrated circuit op amp design. The design of an actual op amp may deviate from the simplified examples considered in this section. If the reader is faced with the task of designing an op amp for a sophisticated application, this material is a good starting place. It should be followed by a careful reading of the technical literature—in particular, pertinent articles in the *IEEE Journal of Solid State Circuits* and some of the references cited in this section.

6.6 COMPARATORS

In many signal processing applications, the ability to compare two signals and identify which is larger is very important. A *comparator* is a circuit that compares one analog signal with another. The output of the comparator depends on which input signal is larger. Figure 6.6-1 shows the symbol for a comparator. We note that it has two inputs and one output.

6.6.1 Characterization of Comparators

The ideal operation of the comparator is illustrated by Fig. 6.6-2. In Fig. 6.6-2*a*, a noninverting comparator is shown. This characteristic can be described as

$$V_{OUT} = \begin{cases} V_{OH} & V_P \geq V_N \\ V_{OL} & V_P < V_N \end{cases} \tag{6.6-1}$$

where V_{OH} is the upper limit and V_{OL} is the lower limit of the output voltage of the comparator. The comparator of Fig. 6.6-2*a* is called *noninverting* because the output goes from the low state to the high state when the voltage V_P becomes larger than V_N. Figure 6.6-2*b* shows an inverting comparator. This type of comparator can be described as

$$V_{OUT} = \begin{cases} V_{OL} & V_P \geq V_N \\ V_{OH} & V_P < V_N \end{cases} \tag{6.6-2}$$

where the output goes from the high state to the low state when the voltage V_P becomes larger than V_N.

The comparator characteristics of Fig. 6.6-2 are ideal in the sense that they require the comparator to have infinite gain during the output transition. Figure

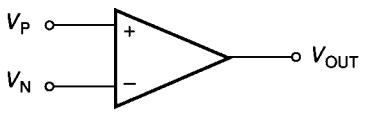


FIGURE 6.6-1
Circuit symbol for a comparator.

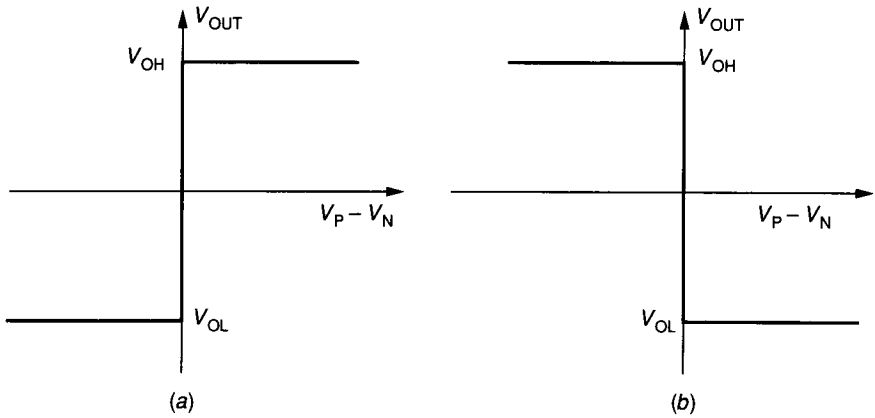


FIGURE 6.6-2
Ideal voltage transfer characteristics of: (*a*) A noninverting comparator, (*b*) An inverting comparator.

6.6-3 shows the transfer characteristics for comparators that do not have infinite gain. The noninverting comparator is described by

$$V_{OUT} = \begin{cases} V_{OH} & (V_P - V_N) > V_{IH} \\ A_v(V_P - V_N) & V_{IL} \leq (V_P - V_N) \leq V_{IH} \\ V_{OL} & (V_P - V_N) < V_{IL} \end{cases} \tag{6.6-3}$$

where V_{IL} and V_{IH} represent the values of $(V_P - V_N)$ at which the output is at V_{OL} and V_{OH}, respectively, as $| V_P - V_N |$ is increased from zero. The inverting comparator is shown in Fig. 6.6-3*b* and is described as

$$V_{OUT} = \begin{cases} V_{OL} & (V_P - V_N) > V_{IH} \\ -A_v(V_P - V_N) & V_{IL} \leq (V_P - V_N) \leq V_{IH} \\ V_{OH} & (V_P - V_N) < V_{IL} \end{cases} \tag{6.6-4}$$

The performance of a comparator can be characterized by its (1) resolving capability or threshold sensing, (2) input offset voltage, (3) speed or propagation delay time, and (4) input common-mode range. The *resolving capability* of a comparator is defined in terms of Fig. 6.6-3 as $V_{IH} - V_{IL}$. It is easy to see that the resolving capability of a comparator is related to its gain. Assuming that V_{OH} and V_{OL} are fixed by power supply limits, the resolving capability, ΔV , can be expressed as

$$\Delta V = \frac{V_{OH} - V_{OL}}{A_v} \tag{6.6-5}$$

As A_v becomes large, the resolving capability approaches the ideal of Fig. 6.6-2. The input offset voltage, V_{OS}, is the value of voltage applied between the inputs

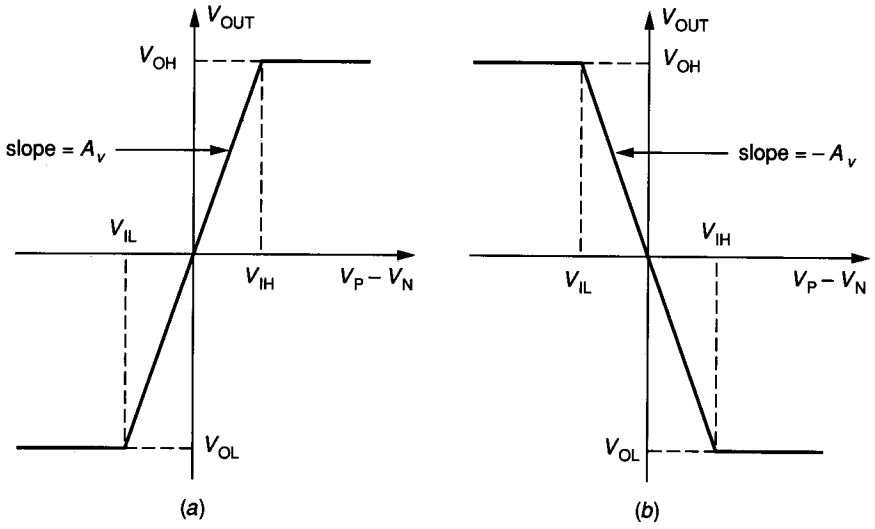


FIGURE 6.6-3
Practical voltage transfer characteristics of: (*a*) A noninverting comparator, (*b*) An inverting comparator.

to make V_{OUT} equal to zero when V_P and V_N are connected together (i.e., the comparator V_{OS} is the same as the op amp V_{OS}). Figure 6.6-4 shows the effect of V_{OS} on the transfer characteristics of the noninverting comparator of Fig. 6.6-3*a*.

The *propagation time* of the comparator is a measure of how quickly the output changes states after the input threshold has been reached. Figure 6.6-5 shows the time domain response of a noninverting comparator. The propagation

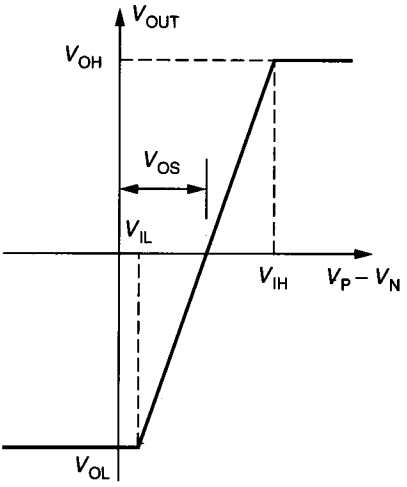


FIGURE 6.6-4
Practical noninverting voltage transfer characteristic with input offset voltage illustrated.

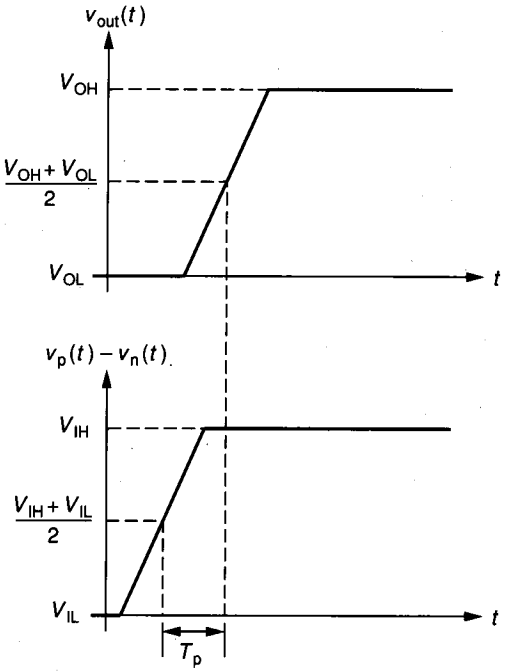


FIGURE 6.6-5
Time response for the practical noninverting comparator.

time, T_p, is the time between when $(V_P - V_N)$ is equal to zero, typically $0.5(V_{IH} + V_{IL})$, and when V_{OUT} is equal to $0.5(V_{OH} + V_{OL})$. This parameter is very important since it determines how many comparisons the comparator can make per unit of time. The propagation delay generally varies as a function of the slope, the amplitude of the input, and its common mode value. A larger input or a steeper slope will generally result in a smaller delay time.

The input common-mode range of the comparator is the range of voltages over which the inputs continue to sense the difference between applied input voltages. The resolving capability and input offset voltage are a function of the common-mode input voltage.

6.6.2 High-Gain Comparators

A comparator can be implemented by three methods: use of a high-gain differential amplifier, use of positive feedback, and charge balancing. The charge balancing comparator uses switches and a clock and functions as a comparator only at discrete periods of time. We will discuss only the first method and show how positive feedback can be used to enhance its performance. Charge balancing comparators are discussed elsewhere.[8,9] A good candidate for a comparator is the differential amplifier presented in Sec. 6.3. The key attribute

of the differential amplifier is its ability to amplify the difference between the inverting and noninverting inputs over a wide common-mode range. As a result, the threshold point, or trip point, can be made independent of process and supply variations to a first order. The transfer curve describing the differential amplifier has been presented in Sec. 6.3. For the CMOS differential amplifier of Fig. 6.3-4*c*, the input common-mode range is given by Eqs. 6.3-40 and 6.3-44. The gain of this differential amplifier is given by Eq. 6.3-36 and was calculated as 103 if $K'_N = 24\ \mu A/V^2$, $W_1/L_1 = 1$, $\lambda_N = \lambda_P = 0.01$, and $I_{SS} = 10\ \mu A$. If it is assumed that the difference between V_{OH} and V_{OL} is 5 V, then the resolving capability is about 32 mV. If W_1/L_1 is increased to 10, the resolving capability is 10 mV. The BJT differential amplifier of Fig. 6.3-11 is a good implementation of a comparator. Because of the larger gain, the resolving capability is better than that of the CMOS differential amplifier of Fig. 6.3-4*c*. Assuming $V_{AN} = 100$ V, $V_{AP} = 50$ V, and $V_{OH} - V_{OL} = 5$ V, then the BJT differential amplifier has a gain of 1333 which gives a resolving capability of 3.75 mV.

The input offset voltage of the differential amplifier is due to the mismatches in the devices. Mismatches of this type are unavoidable and result from imperfections in the process. Offsets can be minimized by using a common-centroid geometry layout. Figure 6.6-6 illustrates a common-centroid geometry for a CMOS differential amplifier. It is also desirable to keep the number of bends and corners in the layout to a minimum for the two devices that must match. Typical offsets in the differential amplifier range from 5 to 15 mV for CMOS and from 3 to 10 mV for bipolar. The input offset voltage can be reduced by using large areas for the devices and by keeping the gate-source voltages small.

The propagation time of the differential amplifier used as a comparator is due to the pole at the output. Using Fig. 6.3-15*b* and ignoring the doublet gives a step response of

$$v_o(t) = V_o\left[1 - \exp\left(\frac{-t}{\tau_2}\right)\right] \tag{6.6-6}$$

where τ_2 is equal to R_2C_2 of Fig. 6.3-15*b* and V_o is the final value of the output. The time at which $v_o(t)$ is 50% of V_o is equal to $0.69\tau_2$. Assuming that the rise time of the input step is zero gives the propagation delay of the differential amplifier comparator as

$$T_p \simeq 0.69\tau_2 = 0.69R_2C_2 \tag{6.6-7}$$

Using the values $R_2 = 1\ M\Omega$ and $C_2 = 0.7$ pF for the CMOS differential amplifier comparator gives a propagation delay of 0.43 μs. Using values of $R_2 = 0.67\ M\Omega$ and $C_2 = 7$ pF for the BJT differential amplifier comparator gives a propagation delay time of 3.23 μs. The load capacitance seen by the differential amplifier comparator will greatly influence the propagation delay time. It will be seen that the propagation delay time may be determined by the large signal response (slew rate) rather than the linear step response.

The gain of most CMOS differential amplifier comparators is too small to give satisfactory resolving capability. In order to increase the gain, we turn to the

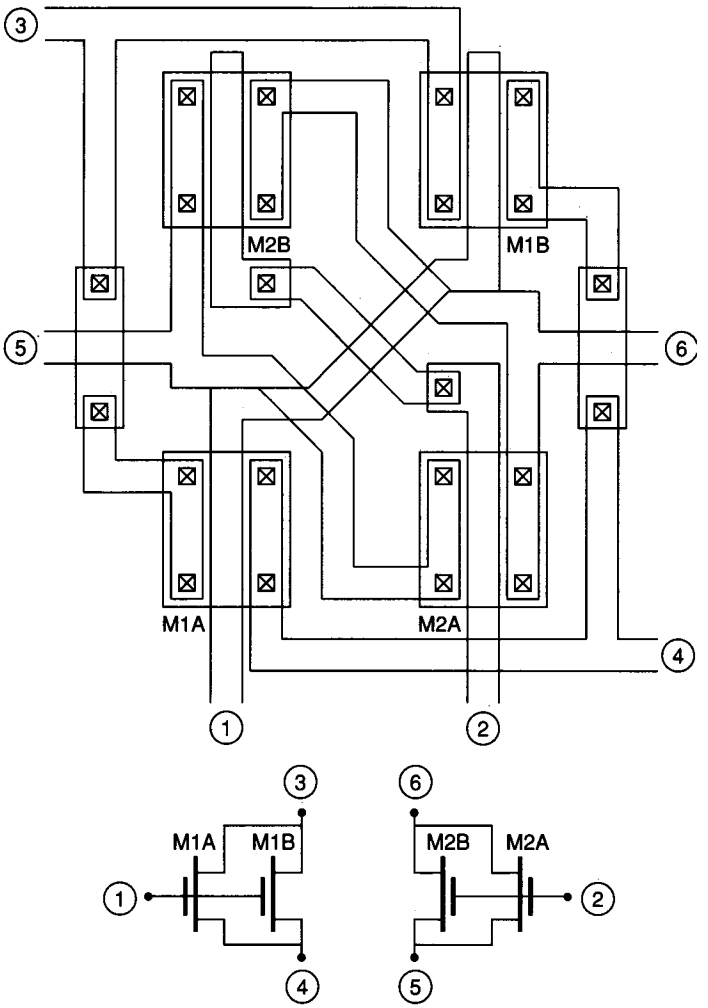


FIGURE 6.6-6
Cross-coupled transistor pair having a common-centroid geometry.

two-stage op amp as a possible architecture for a CMOS comparator. Consider the two-stage CMOS comparator shown in Fig. 6.6-7. It will be assumed that the bulk-source voltages of M1 and M2 are zero (i.e., M1 and M2 are in a floating p-well). This circuit should be designed so that all devices are in saturation. This can be achieved if M1 and M2 are matched and if M3 and M4 are matched and if $V_{SG3} = V_{SG4} = V_{SG5}$. Using these guidelines, we can establish design rules for transistor sizes in this circuit. In order to keep the circuit balanced, M1 and M2, and M3 and M4 must be matched. If the input is balanced, then when V_P and V_N are equal, the current flowing in M7 is split equally through M1 and M2. As a result, we have the following relationships.

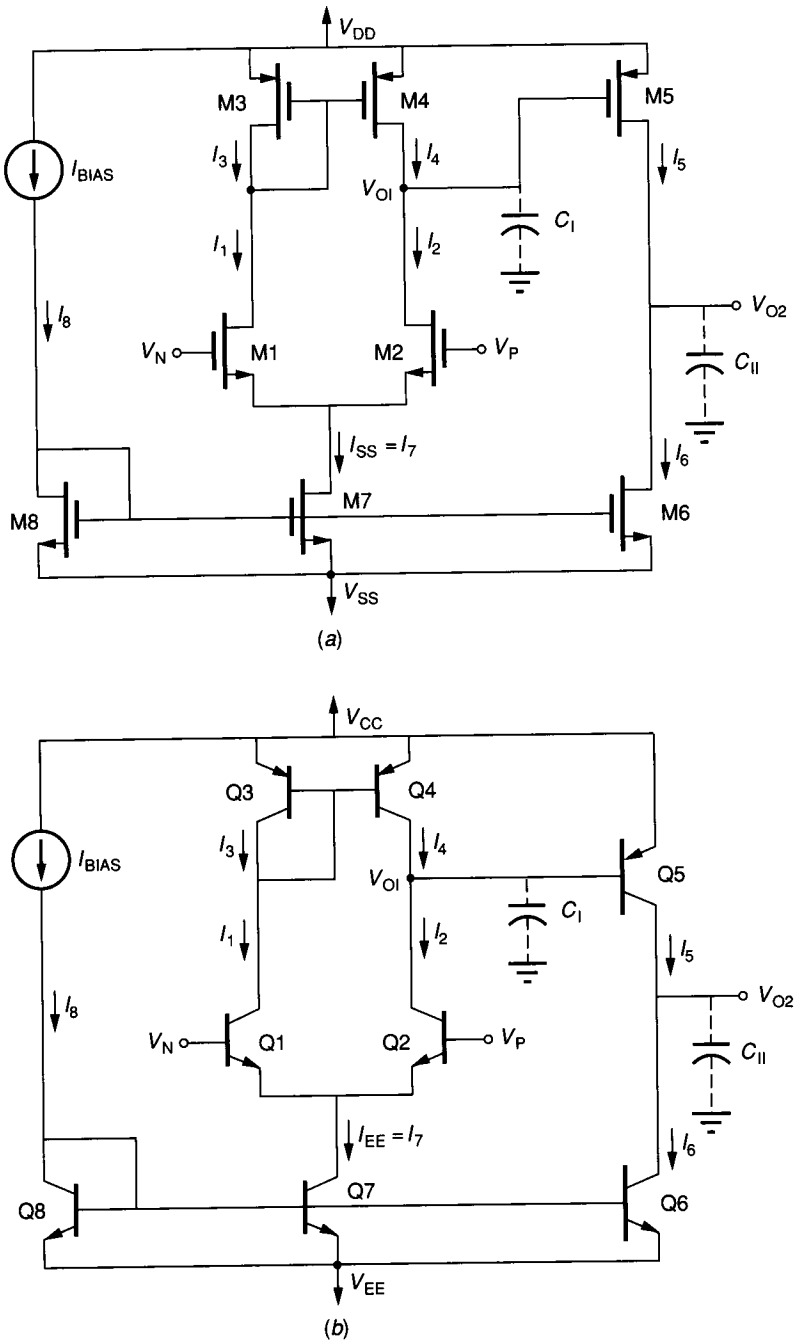


FIGURE 6.6-7
Two-stage comparators. (*a*) CMOS, (*b*) BJT.

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} \tag{6.6-8}$$

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} \tag{6.6-9}$$

and

$$I_1 = I_2 = 0.5I_7 = I_{SS} \tag{6.6-10}$$

These relationships together with Eq. 6.5-40 completely describe the constraints necessary to achieve the desired balance conditions. Unfortunately, there will always be current mismatches in the current mirrors, which will lead to systematic offset (as opposed to a statistical device mismatch offset). This systematic offset is investigated in the following example.

Example 6.6-1. Calculation of systematic offset. The two-stage comparator of Fig. 6.6-7*a* with the following device sizes has been designed using Eqs. 6.6-8–6.6-10 and Eq. 6.5-40: $W_1/L_1 = W_2/L_2 = 20\ \mu/10\ \mu$, $W_3/L_3 = W_4/L_4 = 20\ \mu/10\ \mu$, $W_5/L_5 = 40\ \mu/10\ \mu$, $W_6/L_6 = 10\ \mu/10\ \mu$, $W_7/L_7 = 10\ \mu/10\ \mu$. Assume that $V_{DD} = 10$ V, $V_{SS} = 0$ V, $V_{DS7} = 3$ V, and $V_{DS3} = V_{DS4} = 2$ V. The pertinent process parameters are $K_N' = 24.75\ \mu A/V^2$, $K_P' = 10.13\ \mu A/V^2$, $|V_{TO}| = 1$ V, $\gamma_N = \gamma_P = 0.5\ V^{1/2}$, $\lambda_N = 0.015\ V^{-1}$, and $\lambda_P = 0.02\ V^{-1}$. Find the systematic offset voltage at the input of the comparator.

Solution. Assuming the bias current in M7 is 20 μA gives the following current ratios (see Sec. 5.4).

$$\frac{I_6}{I_7} = \left(\frac{1 + \lambda_N V_{DS6}}{1 + \lambda_N V_{DS4}}\right)\left(\frac{W_6/L_6}{W_7/L_7}\right) = \left[\frac{1 + (0.015)(5)}{1 + (0.015)(2)}\right](1) = 1.029$$

$$\frac{I_5}{I_4} = \left(\frac{1 + \lambda_P V_{DS5}}{1 + \lambda_P V_{DS4}}\right)\left(\frac{W_5/L_5}{W_4/L_4}\right) = \left[\frac{1 + (0.020)(5)}{1 + (0.020)(2)}\right](2) = 2.115$$

and

$$I_7 = 2I_4$$

Thus, the currents I_6 and I_5 can be expressed as

$$I_6 = (1.029)(2)I_4 = 2.058I_4$$

and

$$I_5 = 2.115I_4$$

Since I_5 is greater than I_6, then the current in M5 must be reduced. Next we determine by how much V_{GS5} must be reduced in order to make I_5 equal I_6. The method for accomplishing this is expressed by the following relationship.

$$\Delta V_{GS6} = \left[\frac{2L_5}{K_5 W_5}\right]^{1/2}\left[(I_6)^{1/2} - (I_5)^{1/2}\right] = -14.1\ \text{mV}$$

It can be shown that the voltage gain of the differential amplifier is 81.32. Dividing this value into ΔV_{GS6} gives the systematic offset at the input of the comparator as $|V_{OS}| = 0.174$ mV.

The two-stage BJT op amp is also suitable for use as a comparator. In many cases, the higher gain of the BJT differential amplifier comparator makes it unnecessary to turn to the two-stage architecture. We can note that if the two-stage comparator only switches from V_{OH} to V_{OL} or from V_{OL} to V_{OH}, that compensation is not necessary.

The performance of the input common-mode range of the two-stage BJT and CMOS comparators is identical to that of the BJT and CMOS differential amplifiers of Sec. 6.3. For the CMOS two-stage comparator, a procedure for designing the input stage for a specific common-mode input range is to size M3 to meet the maximum input requirement and design the sizes of M1 and M2 to meet the minimum input requirement. The input common-mode range limits for the CMOS differential amplifier were given in Eqs. 6.3-40 and 6.3-42. These limits, according to the device numbering in Fig. 6.6-7, are

$$V_{G1}(\max) = V_{DD} - \left[\frac{I_7}{\beta_3}\right]^{1/2} - |V_{TO3}| - V_{T1} \tag{6.6-11}$$

where $\beta_3 - K'_P(W_3/L_3)$ and

$$V_{G1}(\min) \simeq V_{TO7} + V_{TO1} + V_{G7} \tag{6.6-12}$$

However, since V_{G7} is not known, it is more convenient to express Eq. 6.6-12 as

$$V_{G1}(\min) \simeq V_{SS} + V_{DS7} + \left[\frac{I_7}{\beta_1}\right]^{1/2} + V_{T1} \tag{6.6-13}$$

where $\beta_1 = K'_N(W_1/L_1)$. An example will be given to illustrate the design of the input stage for a specified input common-mode range.

Example 6.6-2. Designing for a specified input common-mode range. Using the circuit of Fig. 6.6-7*a*, size the transistors M1 through M4 for an input common-mode range of 1.5 to 9 V with $V_{DD} = 10$ V and $V_{SS} = 0$ V.

Solution. Assume the same device parameters as used in Example 6.6-1, except that the magnitude of the p-channel and n-channel threshold voltages vary from 0.4 to 1.0 V, $I_7 = 20$ μA, and $V_{DS}(\text{sat}) = 0.1$ V. Using Eq. 6.6-13 with $V_{G1}(\min) = 1.5$ V, $V_{DS7} = 0.1$ V and $V_{T1} = 1$ V (worst case), we get $\beta_1 = 125$ μA/V^2, which gives $W_1/L_1 = W_2/L_2 = 5.05$. Using Eq. 6.6-11 with $V_{G1}(\max) = 9$ V and worst-case threshold voltages gives $\beta_3 = 125$ μA/V^2, which gives $W_3/L_3 = W_4/L_4 = 12.34$.

6.6.3 Propagation Delay of Two-Stage Comparators

In completing the design of the two-stage CMOS comparator, the gain of the comparator will be achieved by the geometry and dc current of M5. The remaining characteristic to be examined is the propagation delay of the two-stage comparator. Since the comparator is made up of two stages, the total delay is determined by adding the propagation delays of each stage together. Figure 6.6-7 shows the

CMOS and BJT two-stage comparators and the two parasitic capacitors that will be the primary source of the propagation delay. These capacitors are the same ones used in Fig. 6.5-6*b*. C_c was not included in Fig. 6.5-6*a* because the comparators are not usually compensated since they do not normally operate in the linear range. Compensation is only necessary when negative feedback is applied around the comparator. The analysis for the propagation delay of the two-stage comparator is based on the waveforms illustrated in Fig. 6.6-8. The delay for the first stage is the time required for V_{OI} to go from its quiescent state (V_{OHI} or V_{OLI}) to the trip point (V_{TRP2}) of the second stage. The delay for the second stage is the time required for V_{OII} to go from its quiescent state (V_{OHII} or V_{OLII}) to the trip point of the load circuit, which will be assumed to be $0.5(V_{OHII} + V_{OLII})$.

We will consider the propagation delay time for both the BJT and CMOS two-stage comparators simultaneously. It is seen that the propagation delay time for a rising output (T_p^+) will be different from the propagation delay time for a falling output (T_p^-). As a result, we will define the propagation delay time of a comparator (T_p) as the average of T_p^+ and T_p^-. First, let us assume that the output of the comparator is falling and develop an expression for T_p^-. It will be assumed that the difference between V_P and V_N is large enough that M2 (Q2) is off and all of I_7 goes through M1 (Q1). Therefore, the current available to

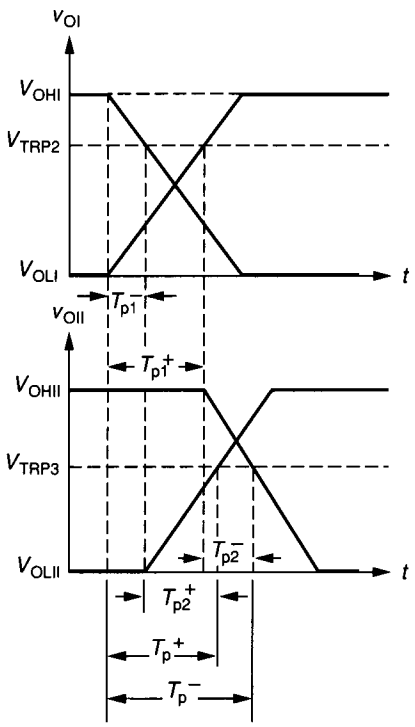


FIGURE 6.6-8
The slewing waveforms at the output of each stage of the two-stage comparator.

charge C_I from V_{OLI} to V_{OHI} is I_7. Thus, the rising propagation delay for the first stage (T_{p1}^+) is

$$T_{p1}^+ = C_I \frac{V_{TRP2} - V_{OLI}}{I_7} \tag{6.6-14}$$

Similarly, the propagation delay time for the falling output of the second stage is

$$T_{p2}^- = C_{II} \frac{V_{OHII} - V_{OLII}}{2I_5} \tag{6.6-15}$$

Adding Eqs. 6.6-14 and 6.6-15 together results in

$$T_p^- = C_I \frac{V_{TRP2} - V_{OLI}}{I_7} + C_{II} \frac{V_{OHII} - V_{OLII}}{2I_5} \tag{6.6-16}$$

The trip point at the input of stage 2 for the BJT is approximately $V_t \ln (I_{BIAS}/I_s)$. I_{BIAS} is the bias current in the second stage, Q6. The trip point for the CMOS output stage is found by equating the currents in M5 and M6, assuming both devices are saturated. The result is

$$\frac{\beta_5}{2}[V_{GS5} - V_{T5}]^2 = I_6 = I_5 \tag{6.6-17}$$

where $\beta_5 = K_P'(W_S/L_S)$ which gives a trip point of

$$V_{TRP2} = V_{DD} - V_{GS5} = V_{DD} - V_{T5} - \left[\frac{2I_5}{\beta_5}\right]^{1/2} \tag{6.6-18}$$

The propagation delay time for a positive-going output is similar, except that the current source charging C_{II} is not limited by the dc value of I_5. The falling propagation delay time for the input stage is given as

$$T_{p1}^- = C_I \frac{V_{OHI} - V_{TRP2}}{I_7} \tag{6.6-19}$$

The rising propagation delay time is given by

$$T_{p2}^+ = C_{II} \frac{V_{OHII} - V_{OLII}}{2I_5(\text{max})} \tag{6.6-20}$$

where $I_5(\text{max})$ is the current M5 or Q5 can source to C_{II} when the gate or base is taken low. In order to find $I_5(\text{max})$, one must know the value of V_{GS5}. Obviously, the value of V_{GS5} will be somewhere between V_{TRP2} and V_{OLI}. Let us approximate V_{GS5} as halfway between V_{OHI} and V_{OLI}. This gives $I_5(\text{max})$ for the CMOS comparator as

$$I_5(\text{max}) \simeq \frac{\beta_5}{2}\left[\frac{V_{OHI} - V_{OLI}}{2} - V_{T5}\right]^2 \tag{6.6-21}$$

For the BJT comparator, $I_5(\text{max})$ is

$$I_5(\text{max}) \simeq \beta_F 5 I_7 \tag{6.6-22}$$

With this interpretation of $I_5(\max)$, the rising propagation delay time of the two-stage comparator is

$$T_p^+ = C_I \frac{V_{OHI} - V_{TRP2}}{I_7} + C_{II} \frac{V_{OHII} - V_{OLII}}{2I_5(\max)} \tag{6.6-23}$$

An example will illustrate the use of these relationships.

Example 6.6-3. Calculation of the propagation delay time for the two-stage comparator. Calculate the propagation time for the CMOS and BJT two-stage comparators of Fig. 6.6-7. Let $V_{DD} = -V_{SS} = 5$ V, $V_{OLI} = -3$ V, $V_{OHI} = 4$ V, $V_{OHII} = 4$ V, and $V_{OLII} = -4$ V. Using the values $C_{gs} = 0.2$ pF, $C_{ds} = 0.1$ pF, and $C_L = 0.5$ pF and assuming the model values of $K_P' = 12.5\ \mu A/V^2$ and $W_5/L_5 = 4.5$. Let $V_{CC} = -V_{EE} = 5$ V, $V_{OHI} = -V_{OLI} = 4.7$ V and $V_{OHII} = -V_{OLII} = 4.5$ V. Furthermore, let us assume that $\beta_{F5} = 100$, $I_{s5} = 0.01$ pA, $C_\mu = 0.2$ pF, $C_\pi = 2$ pF, $C_{CS} = 0.4$ pF, and $C_L = 3$ pF.

Solution. Let us first consider the CMOS two-stage comparator. From Eqs. 6.6-18 and 6.6-21, the values of $V_{TRP2} = 2.67$ V and $I_5(\max) = 112.5\ \mu A$. From Eqs. 6.6-14 and 6.6-15, we obtain the values $T_{p1}^+ = 0.227\ \mu s$ and $T_{p2}^- = 0.056\ \mu s$. Using Eq. 6.6-16 gives the falling propagation delay time as $T_p^- = 0.283\ \mu s$. From Eqs. 6.6-19 and 6.6-20, we get $T_{p1}^- = 0.0132\ \mu s$ and $T_{p2}^+ = 0.0249\ \mu s$. This gives a rising propagation delay time of $0.038\ \mu s$. The average propagation delay time is $T_p = 0.161\ \mu s$. It is seen that the fastest transition of the CMOS comparator is for a rising output.

Next let us consider the BJT two-stage comparator. V_{TRP2} is equal to $V_{CC} - V_t \ln(I_5/I_{s5})$, which is 4.482 V. $I_5(\max)$ is equal to 1 mA from Eq. 6.6-22. From Eqs. 6.5-10 and 6.5-13 we find that $C_I = 3$ pF and $C_{II} = 3.8$ pF. Assuming $I_5 = 200\ \mu A$ and $I_7 = 40\ \mu A$ in Eqs. 6.6-14 through 6.6-16 gives $T_{p1}^+ = 0.69\ \mu s$, $T_{p2}^- = 0.086\ \mu s$, and $T_p^- = 0.775\ \mu s$. Equations 6.6-19, 6.6-20, and 6.6-23 give $T_{p1}^- = 0.0164\ \mu s$, $T_{p2}^+ = 0.0043\ \mu s$, and $T_p^+ = 0.021\ \mu s$. The average propagation delay time of the BJT two-stage comparator is found as $T_p = 0.398\ \mu s$.

We note two things of interest about the two-stage comparator. First, as illustrated in Example 6.6-3, the propagation delay time for a falling output is different from the propagation delay time for a rising output. The reason is due to the value of V_{TRP2}. In both cases, V_{TRP2} is very close to the value of V_{OHI}, which minimizes the delay of the first stage. In addition, the ability to source more output current than sinking current at the output of the second stage reduces the delay time of the second stage. Therefore, two methods that will reduce the propagation delay time of a two-stage comparator are increasing the current sinking/sourcing capability and reducing the signal swings. Of course, smaller values of C_I and C_{II} will reduce the propagation delay times.

Another form of comparator is the *clamped comparator*, shown in Fig. 6.6-9. This comparator architecture attempts to reduce the propagation delay time by keeping the output swing of the first stage clamped. Closer examination of Fig. 6.6-9 shows that only the drains (collectors) of the output devices M5 and M6 (Q5 and Q6) have a large difference between V_{OH} and V_{OL}. Consequently, the propagation delay for the first stage is greatly reduced. While this comparator

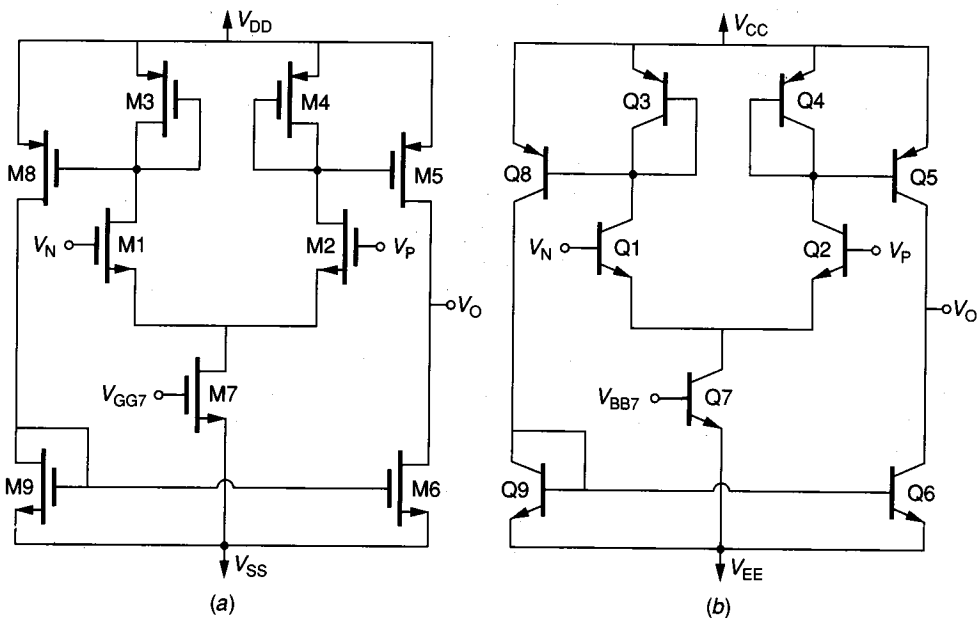


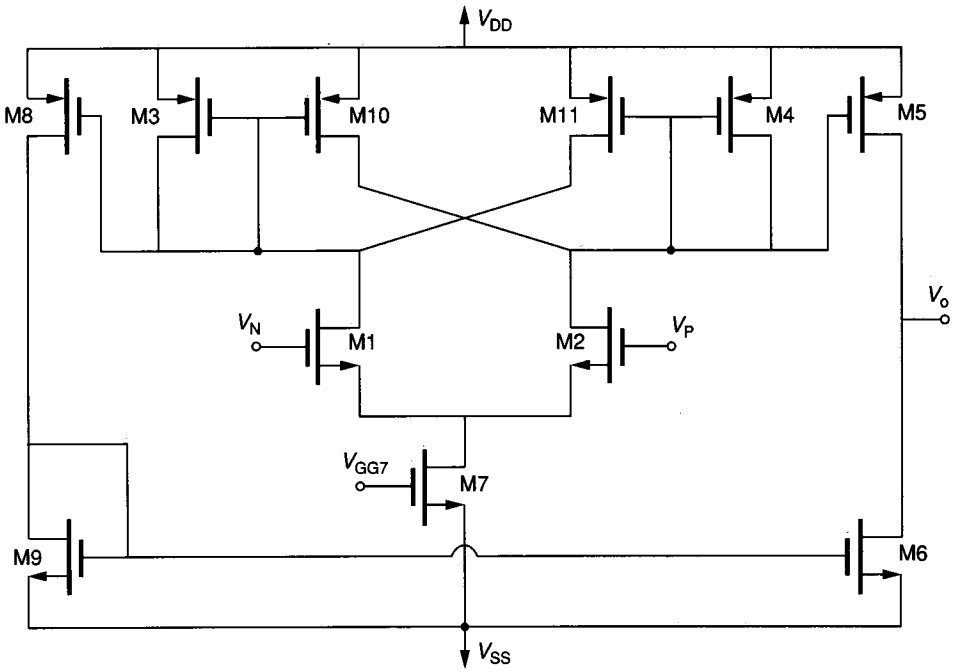
FIGURE 6.6-9
Two-stage clamped comparators: (*a*) CMOS, (*b*) BJT.

architecture reduces the propagation delay time, the overall comparator gain is reduced. Since the effective load devices of the input differential amplifier are smaller, the gain is significantly reduced. In fact, the voltage gain of the first stage will be approximately equal to the ratio of the transconductances of M1 (Q1) and M3 (Q3).

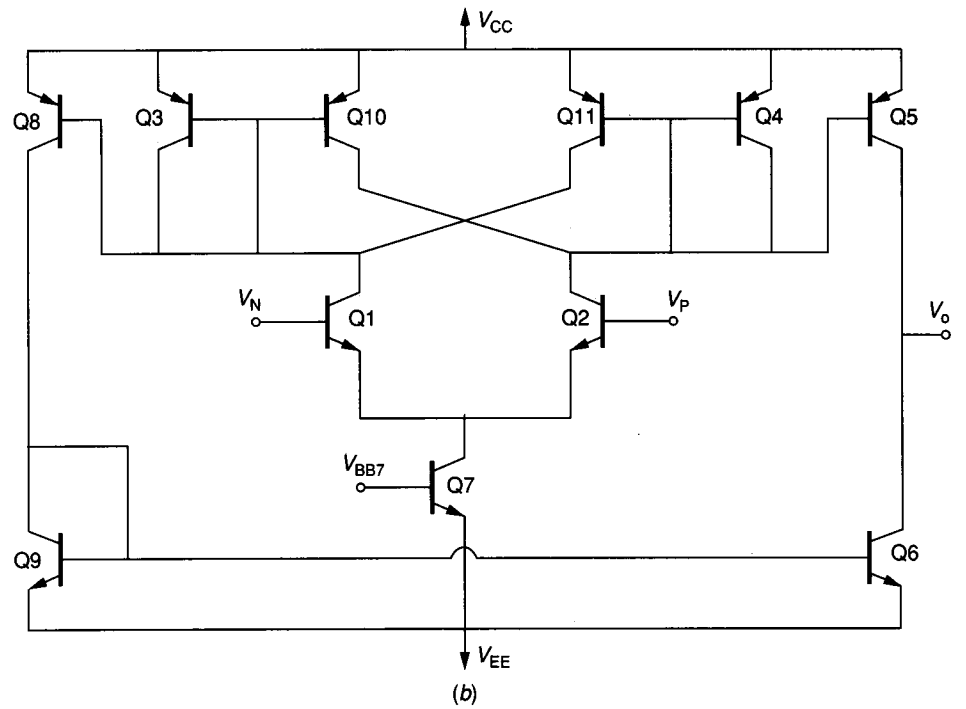
The use of weak positive feedback to overcome the low gain of the clamped comparator can result in satisfactory gain and minimized propagation delay time. One possible implementation is shown in Fig. 6.6-10, where M10 and M11 (Q10 and Q11) have introduced positive feedback paths between the outputs of the differential amplifier. The amount of positive feedback must be less than unity so that the stage still acts like a linear stage as a result of overall negative feedback provided by the source (emitter) connections of the input transistors M1 and M2 (Q1 and Q2).

6.6.4 Comparators Using Positive Feedback

The second approach to implementing comparators uses strong positive feedback or regenerative techniques. This approach is similar to that used in sense amplifiers for memories. Figure 6.6-11 shows a flip-flop with storage capacitors to ground at each output. The circuit works as follows. Assume that the strobe is low, so that M5 (Q5) is off. The flip-flop, consisting of M1 through M4 (Q1 through Q4), is deactivated since no current can flow through any of the devices. This mode



(*a*)



(*b*)

FIGURE 6.6-10
Two-stage, cross-coupled clamped comparator: (*a*) CMOS, (*b*) BJT.

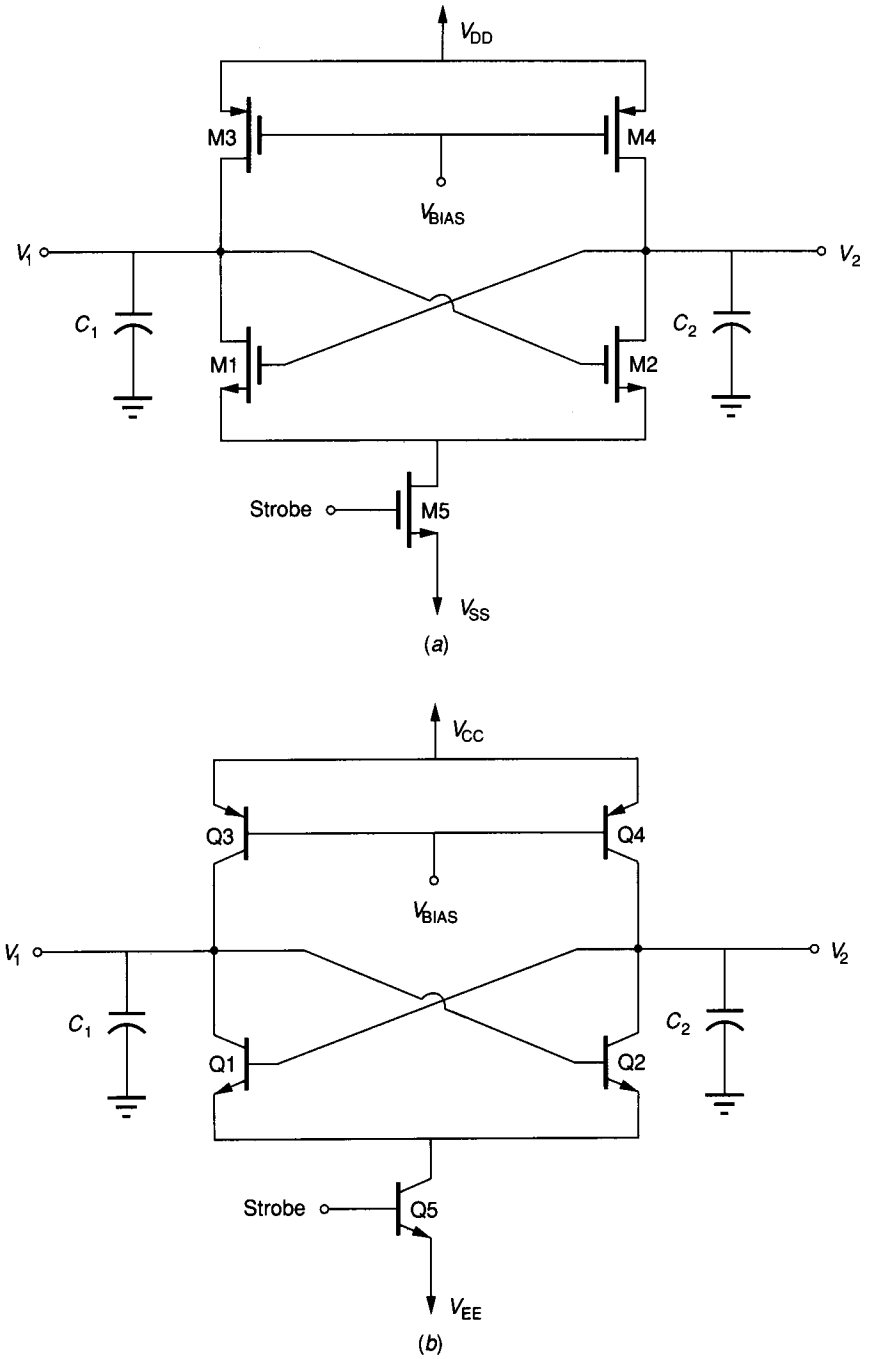


FIGURE 6.6-11
Strobed flip-flop: (*a*) CMOS, (*b*) BJT.

is called the *memory mode,* because the capacitors C_1 and C_2 will "remember" the states of V_1 and V_2. During this time, C_1 and C_2 can also be changed to new values of V_1 and V_2, respectively. When the strobe turns on the flip-flop, then it will go to the state corresponding to the values of V_1 and V_2. For example, if V_1 is greater than V_2, then when the strobe (clock) pulse is applied to M5 (Q5), the voltage at the gate (base) of M2 (Q2) will be higher than the voltage at the gate (base) of M1 (Q1). If the devices are matched, then the flip-flop will regeneratively switch to the state with V_1 high and V_2 low. This circuit can detect differences in V_1 and V_2 within 5 to 10 mV depending on how well the devices in the circuit are matched. A circuit showing how the clocks are applied and how the outputs are buffered is illustrated in Fig. 6.6-12. During the sample mode, ϕ_1 is low and ϕ_2 is high. If V_2 is greater than V_1, then the logic output Q is true. If V_1 is greater than V_2, then the logic output $\overline{Q}$ is true.

6.6.5 Autozeroing

One of the more serious problems of all comparators is the input offset voltage. Clever design techniques and careful layout can reduce but not eliminate the effects of offset. In most applications, the comparator does not operate continuously but rather makes a comparison between two voltages and then is reset. During the reset phase, it is possible to apply a technique called *autozeroing*. This technique works particularly well with CMOS because of the high input resistance of MOS devices. This is rather fortunate, as the offset of CMOS circuits is typically a factor of 2 or more worse than for equivalent BJT circuits.

Figure 6.6-13 illustrates an input offset voltage canceling algorithm. The comparator is shown in terms of an ideal comparator with an external offset voltage in Fig. 6.6-13*a*. A polarity is arbitrarily assigned for purposes of convenience. It is also assumed that the comparator works on a nonoverlapping two-phase clock cycle. During the first cycle, designated ϕ_1, the offset is measured as shown in Fig. 6.6-13*b* and stored in a capacitor, C_{AZ}. During the second cycle, designated ϕ_2, the capacitor is connected in such a manner as to cancel the effects of the offset, as illustrated in Fig. 6.6-13*c*.

A practical implementation of an autozeroed comparator is shown in Fig. 6.6-14. During ϕ_1, the offset is sampled and stored in C_{AZ}. During ϕ_2, the capacitor C_{AZ} is connected in such a manner as to cancel the offset voltage. The comparator can be CMOS or BJT as long as the input resistance is sufficiently large so that C_{AZ} does not discharge during ϕ_2. Figure 6.6-15*a* shows the configuration modified for the case where the comparator is noninverting and V_N is zero. Figure 6.6-15*b* shows the modification of Fig. 6.6-14 for the case where the comparator is inverting and V_P is zero.

Although the autozero technique seems like the perfect solution to the offset problem, it does not completely remove the influence of offset for several reasons. The first is that when the MOS switches open and close, charge is injected or removed by the large clock swings on the gates of the switches. Second, the capacitor C_{AZ} will lose some of its charge during the ϕ_2 phase. Third, if the offset is completely canceled for a given common-mode value of V_P and V_N

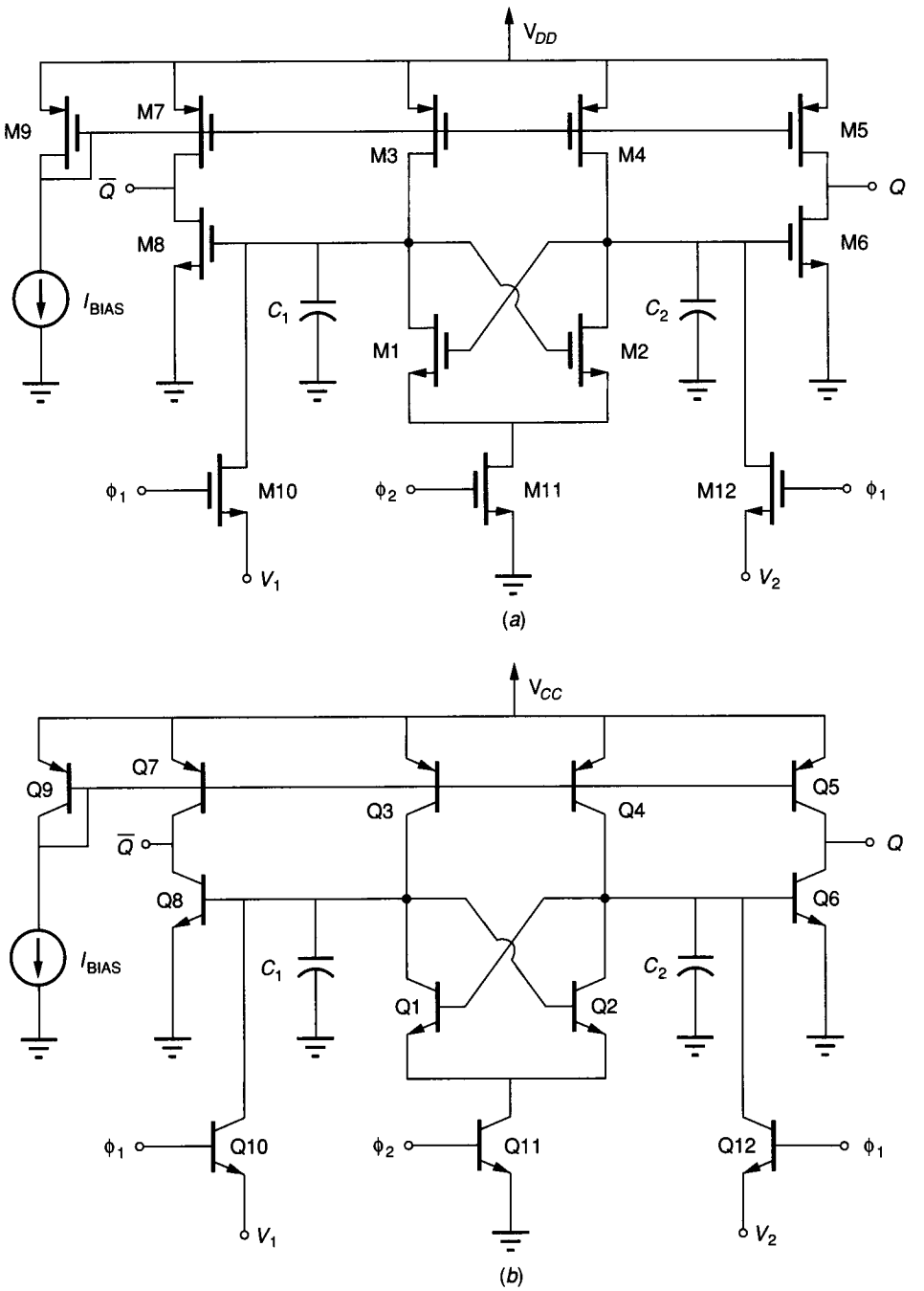


FIGURE 6.6-12
Sense amplifier used as a comparator: (*a*) CMOS, (*b*) BJT.

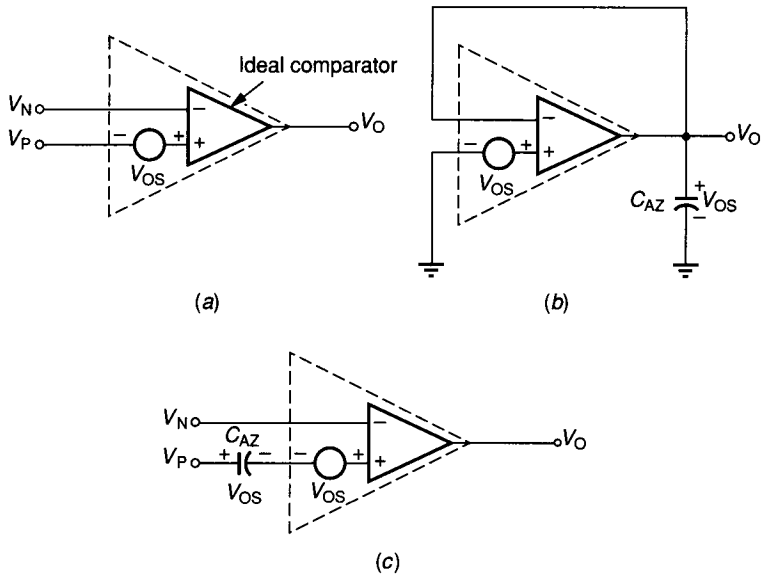


FIGURE 6.6-13
Algorithm to achieve autozeroing of a comparator with offset: (*a*) Model for offset, (*b*) Storing of V_{OS} in C_{AZ}, (*c*) Cancellation of V_{OS}.

during ϕ_1, it may not cancel during ϕ_2 because a different common-mode value of V_P and V_N may have a different value of offset voltage. There is also the problem of stability because the comparator has unity gain, negative feedback applied to it during the sampling mode. It is necessary to compensate the comparator. Finally, a noise kT/C_{AZ} is injected into the circuit each time the switch closes.

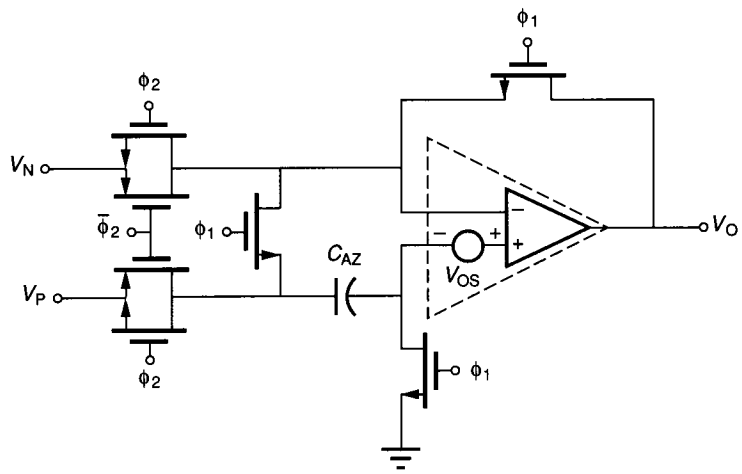


FIGURE 6.6-14
Practical implementation of an autozeroed comparator.

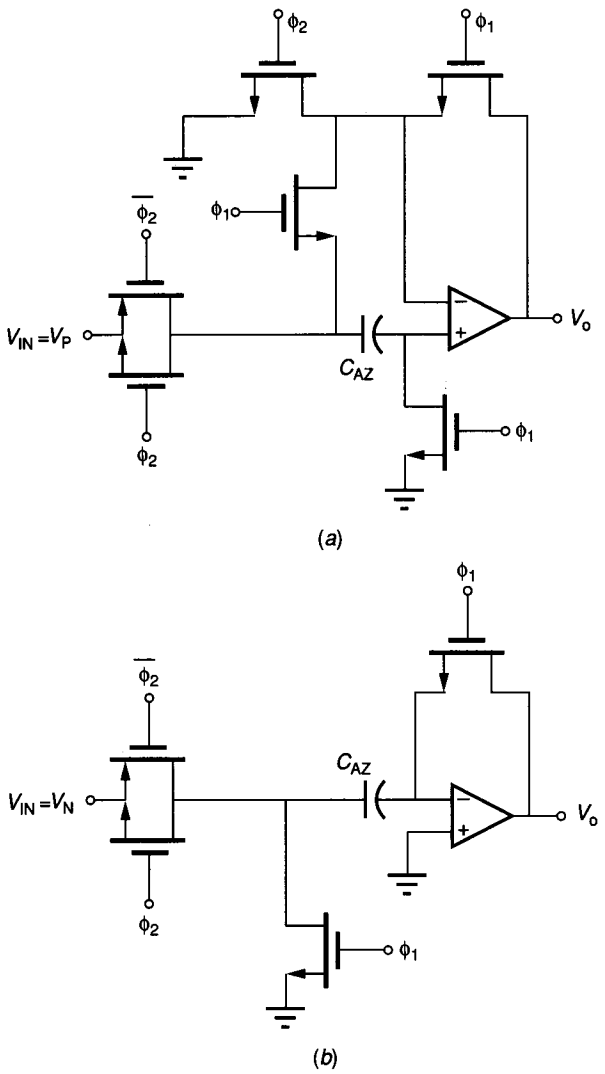


FIGURE 6.6-15
(*a*) Noninverting autozeroed comparator, (*b*) Inverting autozeroed comparator.

The design principles of voltage comparators and various architectures that can be employed have been presented in this section. The important parameters of the comparator are its resolving capability, its input offset voltage, its propagation delay time, and its common-mode input range. The performance of the various circuits was related to these parameters. Except for the considerations of propagation delay time, the comparator requirements were found to be similar to those of the op amp. The comparators in this section represent simple but practical designs. This section represents the starting point in the design of more complex comparators. It should allow the designer the ability to select the design most suitable for the specification. The next step is a thorough simulation of the comparator using a simulator.

6.7 SUMMARY

Basic circuits that form the high-level building blocks of analog integrated circuit design have been presented in this chapter. These circuit blocks include the inverter, the differential amplifier, the output amplifier, the op amp, and the comparator. Design procedures, principles, and examples were given for each type of circuit for both BJT and CMOS technologies. Most of the circuits considered used n-channel or npn devices as the input devices. This choice typically will lead to better performance. The use of p-channel or pnp input devices is straightforward and exactly follows the design concepts presented in this chapter.

It was shown that the design cycle of these blocks starts with the specifications of the circuit performance. Next, an architecture is proposed to implement the circuit. This architecture is always made up from building blocks or circuit blocks with which the designer is familiar. The proposed architecture is then analyzed (typically by hand) and modified by the designer, leading to a first-cut design. This design is then simulated with much more accuracy and detail using a circuit simulator such as SPICE2. The simulation is a very important part of the design cycle and is where the designer can explore process parameter variation and second-order effects.

The circuits presented in this chapter along with the building blocks of Chapter 5 form the blocks or components which the designer uses to achieve a circuit realization. Most of the analog circuits and systems presented in the remainder of this text are simply combinations of these blocks or components. In fact, some of the circuits in this chapter are combinations of previous circuits. For example, the op amp was implemented as a combination of the differential amplifier and the inverter or cascode amplifier.

The material presented in this chapter represents the simplest level of design because of limited space. In many applications, these simple circuits are sufficient. The basic design sequence has been illustrated and has given the reader an appreciation for the design process. This material should be a good starting point in the design of more complex analog integrated circuits.

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PROBLEMS

Section 6.1

6.1 Assume that Eq. 6.1-1, which corresponds to the circuit of Fig. 6.1-3*a*, is given as

$$I_O = V_{IX}^2 + \frac{V_{OX}}{100}$$

and that

$$I_L = \frac{V_P - V_{OUT}}{100}$$

Solve for the small signal voltage gain when $V_{IN} = V_{OUT} = 0$ V.

6.2 Use the relationships given in Prob. 6.1 and develop a linear small signal model similar to that of Fig. 6.1-6. Assuming $V_{IN} = V_{OUT} = 0$ V, find the small signal voltage gain.

6.3 Assume that $r_1 = 1\ \text{M}\Omega, r_2 = 100\ \text{k}\Omega, C_1 = 1$ pF, $C_2 = 1$ pF, and $g_m = 0.001$ S. Find the root (poles and zero) locations if $C_3 = 0$ and $C_3 = 1$ pF for the circuit of Fig. 6.1-8.

6.4 Repeat Example 6.1-1 if $W_1/L_1 = 100\ \mu/10\ \mu$ and $W_2/L_2 = 5\ \mu/10\ \mu$.

6.5 Repeat Example 6.1-2 if $W_1/L_1 = W_2/L_2 = 10\ \mu/10\ \mu$.

6.6 Repeat Example 6.1-2 for the inverter of Fig. P6.6. Assume the active area extends 10 μ beyond the polysilicon.

6.7 Figure P6.7 shows several MOS inverters. Assume that $K_N = 2K_P$, that $\lambda_N = \lambda_P$, and that the dc bias current through each inverter is equal. Qualitatively select, without using extensive calculations, which inverter(s) has (*a*) the largest ac small signal gain, (*b*) the lowest ac small signal gain, (*c*) the highest ac output resistance, and (*d*) the lowest ac output resistance. Assume all devices are in saturation.

6.8 Repeat Example 6.1-4 for $V_{BB2} = 4.3$ V.

6.9 Repeat Example 6.1-4 for the BJT inverter of Fig. 6.1-18*b*.

6.10 Figure 6.1-18 shows two BJT inverters. If $V_{AFN} = 2V_{AFP}$ and $\beta_{FN} = 2\beta_{FP}$, which inverter has (*a*) the highest ac voltage gain, (*b*) the smallest ac voltage gain, (*c*) the

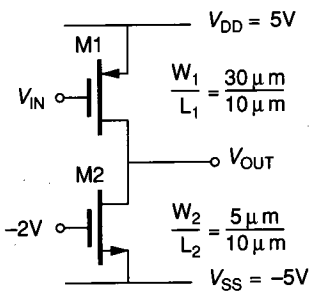

FIGURE P6.6

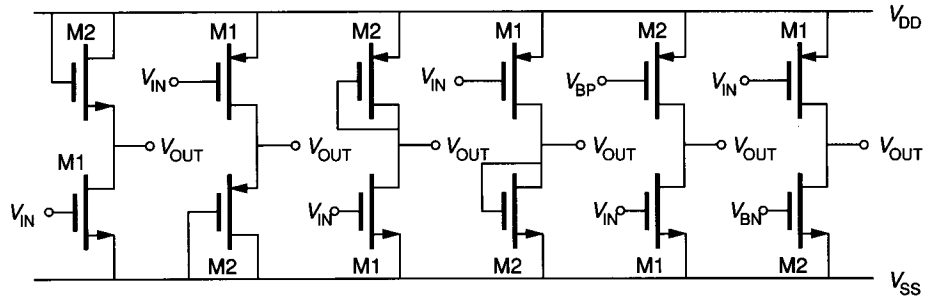

FIGURE P6.7

highest ac output resistance, and (*d*) the lowest ac output resistance. Assume that the bias currents are equal.

Section 6.2

6.11 Find the ac voltage gain and the output resistance for the circuit of Fig. 6.2-2 if the bias current is 100 μA, $W_1/L_1 = 100\ \mu/10\ \mu$, $W_2/L_2 = 100\ \mu/10\ \mu$, and $W_3/L_3 = 10\ \mu/10\ \mu$. Use the model parameters of Table 3.1-2 and assume all devices are saturated.

6.12 Repeat Example 6.2-1 with all W/L values equal to 20 $\mu/20\ \mu$.

6.13 Find the small signal voltage gain and output resistance for the circuit of Fig. 6.2-8 if $I_C = 1$ mA.

6.14 Repeat Prob. 6.13 for the circuit of Fig. 6.2-10.

Section 6.3

6.15 If the active loads of the circuit of Fig. 6.3-1 were replaced by identical drain–gate-connected enhancement n-channel transistors, sketch the large signal voltages, V_{D1} and V_{D2}, as a function of the differential input voltage V_{ID} if K_N' is 20 μA/V^2, $W_1/L_1 = W_2/L_2 = 10\ \mu/10\ \mu$, $W_3/L_3 = W_4/L_4 = 10\ \mu/40\ \mu$ (M3 and M4 are the drain–gate-connected active loads), and $I_{SS} = 50$ μA. Assume $V_{DD} = 10$ V. Ignore the bulk effects of M3 and M4 in this problem.

6.16 Substitute Eq. 6.3-7 into Eq. 6.3-18 and develop an expression for V_{D1} as a function of V_{ID} as a function of $(\beta_1/I_{SS})^{1/2}V_{ID}$. Evaluate the large signal, differential to single-ended voltage gain at $V_{id} = 0$ V of Fig. 6.3-4*a* and compare with Eq. 6.3-20.

6.17 Develop expressions for the maximum and minimum input voltages, V_{G1}(max) and V_{G1}(min), for the differential amplifier of Fig. 6.3-4*a* assuming $V_{G1} = V_{G2}$. Develop expressions for the maximum and minimum output voltages, V_{D2}(max) and V_{D2}(min). Assume that these limits are found by keeping the appropriate devices in the saturation region.

6.18 Verify the small signal voltage gain, A_{vds} (Eqs. 6.3-20 and 6.3-28), and the output resistance, r_{out} (Eqs. 6.3-25 and 6.3-31) for the circuit of Fig. 6.3-4*a* and *b*.

6.19 Interchange the p-channel and n-channel devices in Fig. 6.3-4*c*. Assume that $W_1/L_1 = W_2/L_2$ and $I_5 = 10$ μA. Using the parameters of Table 3.1-2 find the voltage gain, A_{vdd}, and output resistance, r_{out}.

6.20 Replace the current sink of Fig. 6.3-12*b* with the current mirror of Fig. 5.4-12*a*. I_{IN} is to be generated by connecting an arbitrary resistor to V_{DD}, and I_{OUT} is to be used as I_5. Develop an expression for the CMRR and compare with Eq. 6.3-49.

6.21 Assume that two equal resistors designated as R_E are placed between the emitters of Q1 and Q2 at point A in Fig. 6.3-9. Construct a plot similar to that of Fig. 6.3-10 of the normalized value of I_{C1} as a function of V_{ID}. Express the differential-in, single-ended-out transconductance for this case, g'_m, in terms of the transconductance, g_m, given by Eq. 6.3-55.

6.22 Find the small signal, differential-in, differential-out voltage gain, input differential resistance, and output resistance for the circuit of Fig. 6.3-11 if Q1 and Q2 are matched, Q3 and Q4 are matched, $I_{EE} = 100\ \mu A$, $\beta_F = 100$, $V_{AFN} = 100$ V, and $V_{AFP} = 50$ V. Assume room temperature. Repeat for $I_{SS} = 10\ \mu A$.

6.23 Verify the small signal expressions for A_{vds}, and A_{vc} and derive an expression for r_{out} and r_{id} of the circuit of Fig. 6.3-13.

6.24 Assume that $\lambda = 0.01$ V, $C_{gs} = 0.2$ pF, $C_{gd} = 0.1$ pF, and $C_L = 0.5$ pF for the MOS differential amplifier of Fig. 6.3-4*b*. Find the -3 dB frequency in Hertz and the low-frequency gain (A_{vds0}) if (*a*) $I_5 = 10\ \mu A$ and (*b*) $I_5 = 1$ mA.

6.25 Assume that $\beta_{FN} = 100$, $\beta_{FP} = 50$, $V_{AN} = 100$ V, $V_{AP} = 50$ V, $C_\mu = 1$ pF, $C_\pi = 2$ pF, $C_{CS} = 1$ pF, and $C_L = 5$ pF for the BJT differential amplifier of Fig. 6.3-11. Find the -3 dB frequency in Hertz and the low-frequency gain (A_{vds0}) if (*a*) $I_{EE} = 10\ \mu A$ and (*b*) $I_{EE} = 1$ mA.

6.26 Assume that the MOS differential amplifier of Fig. 6.3-4*c* has the parameters $K'_N = 2K'_P = 25\ \mu A/V^2$, $\lambda = 0.01$ V, $W_1/L_1 = W_2/L_2 = 10$, $W_3/L_3 = W_4/L_4 = 1$, $C_{gs} = 0.2$ pF, $C_{gd} = 0.1$ pF, and $I_{SS} = 100\ \mu A$. Find $A_{vds0}, \omega_1, \omega'_1$, and ω_2 defined in Eq. 6.3-84. Find the -3 dB frequency in Hertz for A_{vds}.

6.27 Assume that the BJT differential amplifier of Fig. 6.3-11 has the parameters of $\beta_F = 100$, $V_{AN} = 100$ V, $V_{AP} = 50$ V, $C_\pi = 5$ pF, $C_\mu = 1$ pF, and $I_{EE} = 100\ \mu A$. Find $A_{vds0}, \omega_1, \omega'_1$, and ω_2 defined in Eq. 6.3-84. Find the -3 dB frequency in Hertz for A_{vds}.

Section 6.4

6.28 If the specifications of an output amplifier include the ability to output a voltage of ± 5 V and a slew rate of 10 V/μs, what is the maximum required output current if (*a*) $R_L = 10\ k\Omega$ and $C_L = 50$ pF, (*b*) $R_L = 5\ k\Omega$ and $C_L = 50$ pF, and (*c*) $R_L = 10\ k\Omega$ and $C_L = 100$ pF?

6.29 If the dc bias current in a Class A amplifier is 400 μA and the power supplies are ± 5 V, find the signal power dissipated in a 10 kΩ load resistance for the maximum output sinusoidal signal. Calculate the power given by the power supplies and divide this value into the signal power to calculate the maximum efficiency of the Class A amplifier.

6.30 Use the small signal models for the MOS and BJT transistors to develop the expression given in Eqs. 6.4-24 and 6.4-25 for the circuit of Fig. 6.4-9*a* and *b*.

6.31 If the n-channel transistors in Fig. 6.4-9*a* have $K'_N = 25\ \mu A/V^2$, $V_{TO} = 1$ V, $V_{GG2} = -3V_g$, $V_{DD} = -V_{SS} = 5$ V, $\gamma = 0.5\ V^{1/2}$, $\phi_N = 0.6\ V$, $W_1/L_1 = 10$, and $W_2/L_2 = 40$, find the maximum peak-to-peak output voltage swing if R_L is 10 kΩ, assuming that the gate of M1 can be driven to within 1 V of the $+5$ V power supply. What are the maximum positive and negative slew rates when the output voltage is passing through zero for a load capacitor of 50 pF (assuming that V_{IN} can be driven to $+4$ V)?

6.32 Show how the MOS differential amplifier of Fig. 6.3-4*c* can be used to implement the error amplifiers of Fig. 6.4-15*a*. Note that the implementation of one of the error amplifiers will require opposite-type devices. If all *W/L* ratios are 1 and each transistor has a bias current of 50 μA, calculate the loop gain and the small signal output resistance of the circuit of Fig. 6.1-15*a* if $K'_N = 2K'_P = 25\ \mu A/V^2$.

Section 6.5

6.33 Assume that V_1 of Fig. 6.5-1 is zero and that a resistor R_1 is connected between a voltage source, V_{IN}, and V_2, and a resistor R_2 is connected from the output, V_O, back to the negative input of the op amp. Use the null port concept to find V_O/V_{IN}.

6.34 Repeat Prob. 6.33 if the resistor R_1 is connected from the negative input to the op amp to ground, and the voltage source, V_{IN}, is connected to the positive input of the op amp. R_2 is still connected between V_O and the negative input to the op amp.

6.35 Analyze the circuit of Fig. 6.5-6*b* and verify the expression given in Eq. 6.5-17. Use the techniques illustrated to derive the root locations as given in Eqs. 6.5-18, 6.5-19, and 6.5-20.

6.36 Determine the ratios of the emitter areas of Q6 to Q8 and Q7 to Q8 of Fig. 6.5-4*a* if I_{C1} is 5 μA and I_{C5} is 25 μA, and the 100 kΩ resistors are connected from the collector of Q8 to $V_{CC} = 5$ V and $V_{EE} = -5$ V.

6.37 For the two-stage BJT op amp, let $A_o = 100{,}000$, $R_{id} = 1$ MΩ, and $C_c = 20$ pF. Find I_{C1}, I_{C5}, GB (in MHz), and SR. Assume that the BJT parameters are $\beta_N = 200, \beta_P = 50, V_{AN} = 100$ V, and $V_{AP} = 50$ V. Give the ratios of the emitter area of Q6 to Q8 and Q7 to Q8, and determine the value of resistance to be connected from the collector of Q8 to V_{CC} if $V_{CC} = -V_{EE} = 5$ V.

6.38 Repeat Prob. 6.37 if each npn and pnp transistor is replaced with a pnp and a npn transistor, respectively.

6.39 On a log-log scale with the vertical axis running from 10^{-3} to 10^3 and the horizontal axis running from 1 μA to 100 μA, plot the low-frequency gain (A_o), the unity-gain bandwidth (GB), the power dissipation (P_d), the slew rate (SR), the output resistance (r_{out}), the magnitude of the dominant pole (p_1), and the magnitude of the RHP zero (z) normalized to their values at a bias current ($I_B = I_{DB}$) of 1 μA as a function of I_B for values of I_B from 1 μA to 100 μA for the CMOS two-stage op amp of Fig. 6.5-5*a*. Assume the op amp uses a Miller compensation capacitor, C_c, with no R_z.

6.40 If $W_1/L_1 = W_2/L_2 = 10\ \mu/10\ \mu$, complete the design of the two-stage CMOS op amp of Fig. 6.5-5*a* (i.e., find $W_3, L_3, W_4, L_4, W_5, L_5, C_c$, and R_z). Assume a minimum transistor dimension of 10 μ and use the smallest devices possible. The dc current is 100 μA in M7 and 200 μA in M8. The op amp is to have a low-frequency gain of 5000 and a unity-gain bandwidth of 1 MHz. In addition, all devices should be in saturation under normal operating conditions, and the effects of the RHP zero should be canceled. The pertinent model parameters are $K'_N = 2K'_P = 10\ \mu$A/V^2, $V_{TN} = -V_{TP} = 1$ V, and $\lambda_N = \lambda_P = 0.01$ V^{-1}. Estimate how much load capacitance, C_L, this amplifier should be able to drive without suffering a significant change in the phase margin. What is the slew rate of this op amp?

6.41 Find all currents in the circuit of Fig. P6.41, A_o, GB, SR, r_{out}, power dissipation (P_d), the dominant pole location (p_1), and the value of R_z required to cancel out the effects of the RHP zero. Assume $V_{DD} = -V_{SS} = 5$ V and $C_L = 10$ pF. The device parameters for this problem are $V_{TN} = -V_{TP} = 1$ V, $K'_N = 2K'_P = 24\ \mu$A/V^2, and $\lambda_N = \lambda_P = 0.01$ V^{-1}. Assume that $W_9/L_9 = 2W_{10}/L_{10}$, and find the value of the ratios that will implement R_z.

6.42 Design a folded cascode CMOS op amp that meets the following specifications: $A_o = 50{,}000$, GB $= 5$ MHz, and SR $= \pm 1$ V/μs for a load capacitance of 20 pF. Assume the device parameters of $K'_N = 2K'_P = 25\ \mu$A/V^2, $V_{TN} = -V_{TP} = 1$ V, $\lambda_N = \lambda_P = 0.01$ V^{-1}, all $V_{SB} = O$ V, and give the values of the W/L ratio and the dc currents for each device. What is the power dissipation of your design if the power supplies are ± 5 V?

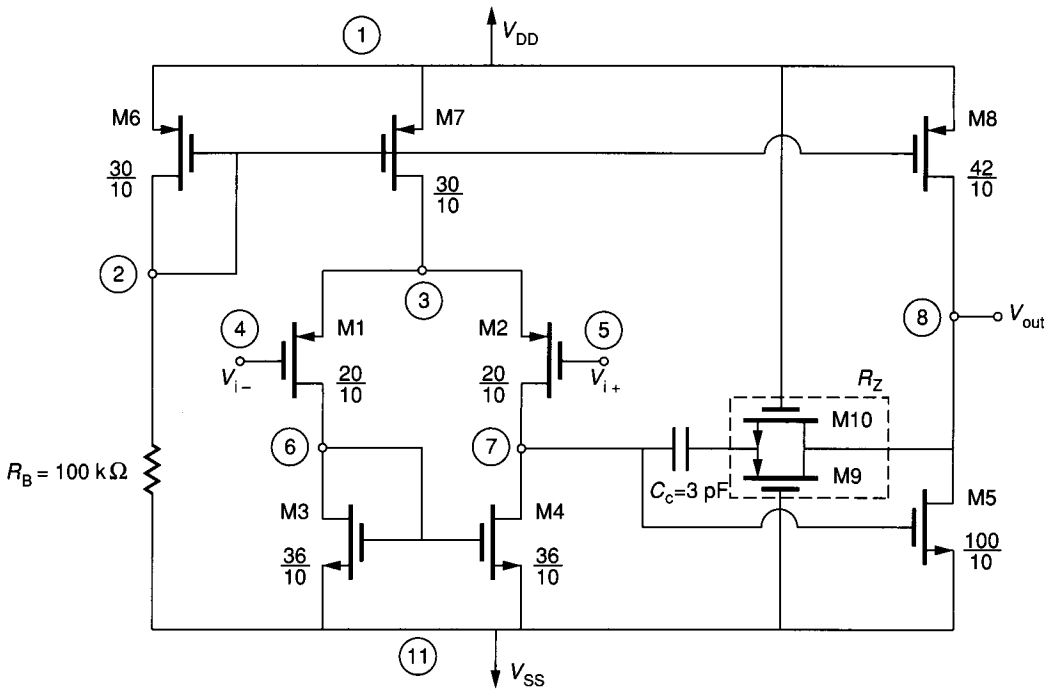

FIGURE P6.41

6.43 Use SPICE to obtain the open-loop magnitude and phase response of the two-stage CMOS op amp of Fig. 6.5-5*a* with a 20 pF load capacitance using the W and L values of Table 6.5-2. What is the phase margin of this op amp?

6.44 Propose and justify a method of measuring the open loop output resistance of an op amp.

Section 6.6

6.45 If $C_{II} = 0.7$ pF and $I_{SS} = 10\ \mu$A, find the time required for the CMOS differential comparator of Fig. 6.6-7*a* to slew 5 V. If $C_{II} = 7$ pF and $I_{EE} = 20\ \mu$A, find the time required for the BJT differential comparator of Fig. 6.6-7*b* to slew 5 V. Assume $I_6 = 10I_7$ and $C_I = 0$.

6.46 Repeat Example 6.6-1 for the calculation of the systematic offset for the BJT two-stage comparator. Use the device numbering scheme of Fig. 6.6-7. Also, assume that $V_{CC} = 10$ V, $V_{EE} = 0$ V, $V_{CE7} = 3$ V, and $V_{CE3} = V_{CE4} = 2$ V. The values of V_{AFN} and V_{AFP} are 100 V and 50 V, respectively, and the bias current in Q7 is 20 μA.

6.47 If $C_{gd} = 0.2$ pF, $C_{gs} = 0.3$ pF, and $C_L = 1$ pF, find the propagation delay times T_p^+, T_p^-, and T_p for the two-stage CMOS comparator of Example 6.6-3.

6.48 If $C_\mu = 1$ pF, $C_\pi = 5$ pF, and $C_L = 5$ pF, find the following propagation delay times T_p^+, T_p^-, and T_p for the two-stage BJT comparator of Example 6.6-3 if $I_7 = 40\ \mu$A and $I_5 = 100\ \mu$A.

Design Problems

6.49 Design a voltage-driven, inverting voltage amplifier that will provide a gain of at least -10 and a -3 dB frequency of at least 100 kHz when driving a load of 50 pF in parallel with 50 kΩ. Use the device parameters of Table 3.1-2 or Table 6.1-1.

6.50 Design a BJT inverter that will meet the specifications of Example 6.1-5.

6.51 Repeat Example 6.2-2 using a MOS current-sourcing cascode inverter.

6.52 Design a BJT differential amplifier with a differential to single-ended voltage gain of at least 100 and a common-mode voltage gain of at most 0.1. The differential input resistance should be greater than 100 kΩ. Use the parameters of Table 6.1-1.

6.53 Design a CMOS op amp using the topology of Fig. 6.5-5*a* that meets the following specifications:

$$A_v > 4000$$

$$V_{DD} = +5 \text{ V}$$

$$V_{SS} = -5 \text{ V}$$

$$\text{GB} \geq 1 \text{ MHz } (C_2 = 20 \text{ pF})$$

$$\text{SR} > 2 \text{ V}/\mu\text{s } (C_2 = 20 \text{ pF})$$

$$\text{Input common-mode range} \geq \pm 3 \text{ V}$$

$$\text{Output voltage swing} \geq \pm 4 \text{ V} (R_L = 200 \text{ k}\Omega)$$

$$P_{\text{diss}} < 10 \text{ mW}$$

Use the parameters of Table 3.1-2, and let all drawn channel lengths be 10 μ.

6.54 Design a BJT op amp that will meet the specifications of Prob. 6.6. Use the parameters of Table 6.1-1.