VLSI DESIGN TECHNIQUES
FOR ANALOG AND DIGITAL CIRCUITS

Randall L. Geiger
Department of Electrical Engineering
Texas A&M University

Phillip E. Allen
Department of Electrical Engineering
Georgia Institute of Technology

Noel R. Strader
MCC
Austin, Texas

McGraw-Hill Publishing Company
New York  St. Louis  San Francisco  Auckland  Bogotá  Caracas
Hamburg  Lisbon  London  Madrid  Mexico  Milan
Montreal  New Delhi  Oklahoma City  Paris  San Juan
São Paulo  Singapore  Sydney  Tokyo  Toronto
McGraw-Hill Series in Electrical Engineering

Consulting Editor

Stephen W. Director, Carnegie-Mellon University

CIRCUITS AND SYSTEMS
COMMUNICATIONS AND SIGNAL PROCESSING
CONTROL THEORY
ELECTRONICS AND ELECTRONIC CIRCUITS
POWER AND ENERGY
ELECTROMAGNETICS
COMPUTER ENGINEERING
INTRODUCTORY
RADAR AND ANTENNAS
VLSI

Previous Consulting Editors


VLSI

Consulting Editor

Stephen W. Director, Carnegie-Mellon University

Elliott: Microlithography: Process Technology for IC Fabrication
Geiger, Allen, and Strader: VLSI Design Techniques for Analog and Digital Circuits
Offen: VLSI Image Processing
Ruska: Microelectronic Processing: An Introduction to the Manufacture of Integrated Circuits
Seraphim: Principles of Electronic Packaging
Sze: VLSI Technology
Tsividis: Operation and Modeling of the MOS Transistor
Walsh: Choosing and Using CMOS
# CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preface</td>
<td>xiii</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Practical Considerations</td>
<td>1</td>
</tr>
<tr>
<td>1.0</td>
<td>Introduction</td>
<td>2</td>
</tr>
<tr>
<td>1.1</td>
<td>Size and Complexity of Integrated Circuits</td>
<td>4</td>
</tr>
<tr>
<td>1.2</td>
<td>The Microelectronics Field</td>
<td>10</td>
</tr>
<tr>
<td>1.3</td>
<td>IC Design Process</td>
<td>12</td>
</tr>
<tr>
<td>1.4</td>
<td>Economics</td>
<td>16</td>
</tr>
<tr>
<td>1.5</td>
<td>Yield</td>
<td>19</td>
</tr>
<tr>
<td>1.6</td>
<td>Trends in VLSI Design</td>
<td>28</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>29</td>
</tr>
<tr>
<td></td>
<td>Problems</td>
<td>29</td>
</tr>
<tr>
<td>2</td>
<td>Technology</td>
<td>32</td>
</tr>
<tr>
<td>2.0</td>
<td>Introduction</td>
<td>32</td>
</tr>
<tr>
<td>2.1</td>
<td>IC Production Process</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>2.1.1 Processing Steps</td>
<td>33</td>
</tr>
<tr>
<td></td>
<td>2.1.2 Packaging and Testing</td>
<td>41</td>
</tr>
<tr>
<td>2.2</td>
<td>Semiconductor Processes</td>
<td>42</td>
</tr>
<tr>
<td></td>
<td>2.2.1 MOS Processes</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>2.2.1a NMOS Process</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td>2.2.1b CMOS Process</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td>2.2.1c Practical Process Considerations</td>
<td>59</td>
</tr>
<tr>
<td></td>
<td>2.2.2 Bipolar Technology</td>
<td>64</td>
</tr>
<tr>
<td></td>
<td>2.2.3 Hybrid Technology</td>
<td>68</td>
</tr>
<tr>
<td>2.3</td>
<td>Design Rules and Process Parameters</td>
<td>72</td>
</tr>
<tr>
<td>2.4</td>
<td>Layout Techniques and Practical Considerations</td>
<td>78</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>85</td>
</tr>
<tr>
<td></td>
<td>Problems</td>
<td>85</td>
</tr>
<tr>
<td>Appendixes</td>
<td></td>
<td>95</td>
</tr>
<tr>
<td>2A</td>
<td>Process Characterization of a Generic NMOS Process</td>
<td>95</td>
</tr>
<tr>
<td>2B</td>
<td>Process Characterization of a Generic CMOS Process</td>
<td>108</td>
</tr>
</tbody>
</table>
3 Device Modeling

3.0 Modeling
3.0.1 dc Models
3.0.2 Small Signal Models
3.0.3 Use of Device Models in Circuit Analysis

3.1 MOS Models
3.1.1 dc MOSFET Model
3.1.2 Small Signal MOSFET Model
3.1.3 High Frequency MOSFET Model
3.1.4 Measurement of MOSFET Model Parameters
3.1.5 Short Channel Devices
3.1.6 Subthreshold Operation
3.1.7 Operation in the Third Quadrant of the $I_D - V_{DS}$ Plane
3.1.8 Modeling Noise Sources in MOSFETs
3.1.9 Simple MOSFET Models for Digital Applications

3.2 Diode Models
3.2.1 dc Diode Model
3.2.2 Small Signal Diode Model
3.2.3 High-Frequency Diode Model

3.3 Bipolar Models
3.3.1 dc BJT Model
3.3.2 Small Signal BJT Model
3.3.3 High-Frequency BJT Model
3.3.4 Measurement of BJT Model Parameters

3.4 Passive Component Models
3.4.1 Monolithic Capacitors
3.4.2 Monolithic Resistors

3.5 Summary
References
Problems

4 Circuit Simulation

4.0 Introduction
4.1 Circuit Simulation Using Spice
4.2 MOSFET Model
4.2.1 Level 1 Large Signal Model
4.2.2 Level 2 Large Signal Model
4.5.3 High-Frequency Model
4.2.4 Noise Model of the MOSFET
4.2.5 Temperature Dependence of the MOSFET
4.3 Diode Model
4.3.1 Large Signal Diode Current
4.3.2 High-Frequency Diode Model
4.4 BJT Model
4.4.1 Large Signal BJT Model
4.4.2 High-Frequency BJT Model
### 4.4.3 BJT Noise Model
4.4.4 Temperature Dependence of the BJT

#### 4.5 Summary

| References | 264 |
| Problems   | 265 |

### Appendixes

| 4A Mosfet Parameter Definitions | 271 |
| 4B Diode Parameter Definitions  | 280 |
| 4C BJT Parameter Definitions    | 282 |

### 5 Basic Integrated Circuit Building Blocks

| 5.0 Introduction | 287 |
| 5.1 Switches     | 289 |
| 5.2 Active Resistors | 302 |
| 5.3 Current Sources and Sinks | 318 |
| 5.4 Current Mirrors/Amplifiers | 333 |
| 5.5 Voltage and Current References | 354 |
| 5.6 Summary      | 372 |
| References       | 372 |
| Problems         | 373 |
| Design Problems  | 376 |

### 6 Amplifiers

| 6.0 Introduction | 378 |
| 6.1 Inverting Amplifiers |
| 6.1.1 General Concepts of Inverting Amplifiers | 379 |
| 6.1.2 MOS Inverting Amplifiers | 389 |
| 6.1.3 BJT Inverting Amplifiers | 407 |
| 6.2 Improving the Performance of Inverting Amplifiers |
| 6.2.1 Current-Driven CMOS Cascode Amplifier | 414 |
| 6.2.2 Voltage-Driven CMOS Cascode Amplifier | 418 |
| 6.2.3 Improving the Gain of the CMOS Cascode Amplifier | 419 |
| 6.2.4 The BJT Cascode Amplifier | 426 |
| 6.3 Differential Amplifiers |
| 6.3.1 CMOS Differential Amplifiers | 431 |
| 6.3.2 BJT Differential Amplifiers | 432 |
| 6.3.3 Frequency Response of Differential Amplifiers | 444 |
| 6.3.4 Noise Performance of Differential Amplifiers | 449 |
| 6.4 Output Amplifiers |
| 6.4.1 Output Amplifiers without Feedback | 454 |
| 6.4.2 Output Amplifiers with Feedback | 455 |
| 6.5 Operational Amplifiers |
| 6.5.1 Characterization of Op Amps | 466 |
| 6.5.2 The BJT Two-Stage Op Amp | 473 |
| 6.5.3 The CMOS Two-Stage Op Amp | 481 |
| 6.5.4 Cascode Op Amps | 485 |
| 6.5.5 Op Amps with an Output Stage | 488 |
| 6.5.6 Simulation and Measurement of Op Amps | 491 |
# CONTENTS

6.6 Comparators 499
  6.6.1 Characterization of Comparators 499
  6.6.2 High-Gain Comparators 502
  6.6.3 Propagation Delay of Two-Stage Comparators 507
  6.6.4 Comparators Using Positive Feedback 511
  6.6.5 Autozeroing 514

6.7 Summary 518
  References 518
  Problems 519
  Design Problems 524

## 7 Digital Circuits 525

7.0 Introduction 525
7.1 Design Abstraction 526
7.2 Characteristics of Digital Circuits 528
  7.2.1 Logic Level Standards 528
  7.2.2 Inverter Pair Characteristics 530
  7.2.3 Logic Fan-out Characteristics 532
  7.2.4 Digital Logic Analysis 532

7.3 Single-Channel MOS Inverters 534
  7.3.1 Basic Inverter 534
  7.3.2 Inverter Device Sizing 537
  7.3.3 Enhancement-Load versus Depletion-Load Inverters 539

7.4 NMOS NOR and NAND Logic Circuits 540
  7.4.1 Basic NMOS NOR Logic Circuits 540
  7.4.2 Basic NMOS NAND Logic Circuits 542
  7.4.3 Multi-Input NAND and NOR Logic Circuits 543

7.5 Complementary MOS Inverters 544
  7.5.1 A Basic CMOS Inverter 546
  7.5.2 CMOS Inverter Logic Levels 546
  7.5.3 Inverter Device Sizing 548

7.6 CMOS Logic Gates 551
  7.6.1 CMOS NOR Logic Gate 551
  7.6.2 CMOS NAND Logic Gate 553
  7.6.3 Multi-Input CMOS Logic Gates 556

7.7 Transmission Gates 558
  7.7.1 NMOS Pass Transistor 559
  7.7.2 CMOS Transmission Gate 562

7.8 Signal Propagation Delays 564
  7.8.1 Ratio-Logic Model 565
  7.8.2 Process Characteristic Time Constant 570
  7.8.3 Inverter-Pair Delay 570
  7.8.4 Superbuffers 573
  7.8.5 NMOS NAND and NOR Delays 575
  7.8.6 Enhancement versus Depletion Loads 578
  7.8.7 CMOS Logic Delays 579
  7.8.8 Interconnection Characteristics 582

7.9 Capacitive Loading Considerations 584
  7.9.1 Capacitive Loading 584
  7.9.2 Logic Fan-out Delays 585
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.9.3</td>
<td>Distributed Drivers</td>
<td>587</td>
</tr>
<tr>
<td>7.9.4</td>
<td>Driving Off-Chip Loads</td>
<td>588</td>
</tr>
<tr>
<td>7.9.5</td>
<td>Cascaded Drivers</td>
<td>590</td>
</tr>
<tr>
<td>7.10</td>
<td>Power Dissipation</td>
<td>593</td>
</tr>
<tr>
<td>7.10.1</td>
<td>NMOS Power Dissipation</td>
<td>595</td>
</tr>
<tr>
<td>7.10.2</td>
<td>CMOS Power Dissipation</td>
<td>597</td>
</tr>
<tr>
<td>7.11</td>
<td>Noise in Digital Logic Circuits</td>
<td>599</td>
</tr>
<tr>
<td>7.11.1</td>
<td>Resistive Noise Coupling</td>
<td>599</td>
</tr>
<tr>
<td>7.11.2</td>
<td>Capacitive Noise Coupling</td>
<td>601</td>
</tr>
<tr>
<td>7.11.3</td>
<td>Definition of Noise Margins</td>
<td>602</td>
</tr>
<tr>
<td>7.11.4</td>
<td>NMOS Noise Margins</td>
<td>603</td>
</tr>
<tr>
<td>7.11.5</td>
<td>CMOS Noise Margins</td>
<td>605</td>
</tr>
<tr>
<td>7.12</td>
<td>Summary</td>
<td>607</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>608</td>
</tr>
<tr>
<td></td>
<td>Problems</td>
<td>608</td>
</tr>
<tr>
<td>8</td>
<td>Analog Systems</td>
<td>612</td>
</tr>
<tr>
<td>8.0</td>
<td>Introduction</td>
<td>612</td>
</tr>
<tr>
<td>8.1</td>
<td>Analog Signal Processing</td>
<td>612</td>
</tr>
<tr>
<td>8.2</td>
<td>Digital-to-Analog Converters</td>
<td>615</td>
</tr>
<tr>
<td>8.2.1</td>
<td>Current-Scaling D/A Converters</td>
<td>623</td>
</tr>
<tr>
<td>8.2.2</td>
<td>Voltage-Scaling D/A Converters</td>
<td>626</td>
</tr>
<tr>
<td>8.2.3</td>
<td>Charge-Scaling D/A Converters</td>
<td>629</td>
</tr>
<tr>
<td>8.2.4</td>
<td>D/A Converters Using Combinations of Scaling Approaches</td>
<td>633</td>
</tr>
<tr>
<td>8.2.5</td>
<td>Serial D/A Converters</td>
<td>638</td>
</tr>
<tr>
<td>8.3</td>
<td>Analog-to-Digital Converters</td>
<td>642</td>
</tr>
<tr>
<td>8.3.1</td>
<td>Serial A/D Converters</td>
<td>648</td>
</tr>
<tr>
<td>8.3.2</td>
<td>Successive Approximation A/D Converters</td>
<td>651</td>
</tr>
<tr>
<td>8.3.3</td>
<td>Parallel A/D Converters</td>
<td>659</td>
</tr>
<tr>
<td>8.3.4</td>
<td>High-Performance A/D Converters</td>
<td>664</td>
</tr>
<tr>
<td>8.3.5</td>
<td>Summary</td>
<td>671</td>
</tr>
<tr>
<td>8.4</td>
<td>Continuous-Time Filters</td>
<td>673</td>
</tr>
<tr>
<td>8.4.1</td>
<td>Low-Pass Filters</td>
<td>674</td>
</tr>
<tr>
<td>8.4.2</td>
<td>High-Pass Filters</td>
<td>685</td>
</tr>
<tr>
<td>8.4.3</td>
<td>Bandpass Filters</td>
<td>688</td>
</tr>
<tr>
<td>8.5</td>
<td>Switched Capacitor Filters</td>
<td>692</td>
</tr>
<tr>
<td>8.5.1</td>
<td>Resistor Realization</td>
<td>693</td>
</tr>
<tr>
<td>8.5.2</td>
<td>Passive RLC Prototype Switched Capacitor Filters</td>
<td>703</td>
</tr>
<tr>
<td>8.5.3</td>
<td>Z-Domain Synthesis Techniques</td>
<td>716</td>
</tr>
<tr>
<td>8.6</td>
<td>Analog Signal Processing Circuits</td>
<td>729</td>
</tr>
<tr>
<td>8.6.1</td>
<td>Precision Breakpoint Circuits</td>
<td>729</td>
</tr>
<tr>
<td>8.6.2</td>
<td>Modulators and Multipliers</td>
<td>735</td>
</tr>
<tr>
<td>8.6.3</td>
<td>Oscillators</td>
<td>747</td>
</tr>
<tr>
<td>8.6.4</td>
<td>Phase-Locked Loops</td>
<td>762</td>
</tr>
<tr>
<td>8.7</td>
<td>Summary</td>
<td>765</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>770</td>
</tr>
<tr>
<td></td>
<td>Problems</td>
<td>773</td>
</tr>
<tr>
<td>9</td>
<td>Structured Digital Circuits and Systems</td>
<td>778</td>
</tr>
<tr>
<td>9.0</td>
<td>Introduction</td>
<td>778</td>
</tr>
<tr>
<td>9.1</td>
<td>Random Logic versus Structured Logic Forms</td>
<td>779</td>
</tr>
</tbody>
</table>
9.2 Programmable Logic Arrays
  9.2.1 PLA Organization 784
  9.2.2 Automatic PLA Generation 790
  9.2.3 Folded PLAs 791
  9.2.4 Large PLAs 792
9.3 Structured Gate Layout
  9.3.1 Weinberger Arrays 794
  9.3.2 Gate Matrix Layout 796
9.4 Logic Gate Arrays 799
9.5 MOS Clocking Schemes 805
9.6 Dynamic MOS Storage Circuits 808
  9.6.1 Dynamic Charge Storage 808
  9.6.2 Simple Shift Register 811
  9.6.3 Other Shift Registers 814
9.7 Clocked CMOS Logic 815
  9.7.1 C²MOS 815
  9.7.2 Precharge-Evaluate Logic 817
  9.7.3 Domino CMOS 819
9.8 Semiconductor Memories 821
  9.8.1 Memory Organization 822
9.9 Read-Only Memory 824
  9.9.1 Erasable Programmable Read-Only Memory 825
  9.9.2 Electrically Erasable Programmable Read-Only Memory 826
9.10 Static RAM Memories 827
9.11 Dynamic RAM Memory 835
9.12 Register Storage Circuits 839
  9.12.1 Quasi-Static Register Cells 840
  9.12.2 A Static Register Cell 842
9.13 PLA-Based Finite-State Machines 845
9.14 Microcoded Controllers 848
9.15 Microprocessor Design 853
  9.15.1 Data Path Description 856
  9.15.2 Barrel Shifter 857
  9.15.3 Arithmetic Logic Unit 858
  9.15.4 Microcoded Controller 860
9.16 Systolic Arrays 861
  9.16.1 Systolic Matrix Multiplication 861
  9.16.2 General Linear System Solver 862
  9.16.3 Bit-Serial Processing Elements 863
9.17 Summary 866
  References 866
  Problems 867

10 Design Automation and Verification 872
10.0 Introduction 872
10.1 Integrated Circuit Layout 873
  10.1.1 Geometrical Specification Languages 875
  10.1.2 Layout Styles 878
10.2 Symbolic Circuit Representation 880
  10.2.1 Parameterized Layout Representation 880
  10.2.2 Parameterized Module Generation 883
10.2.3 Graphical Symbolic Layout 884
10.2.4 Logic Equation Symology 885

10.3 Computer Check Plots 889

10.4 Design Rule Checks 894
10.4.1 Geometrical Design Rules 894
10.4.2 Computer Design Rule Checks 897
10.4.3 Design Rule Checker Output 898

10.5 Circuit Extraction 901
10.5.1 A Simple Circuit Extraction Algorithm 902
10.5.2 Circuit Extractor Output 903
10.5.3 Interface to Other Programs 908

10.6 Digital Circuit Simulation 908

10.7 Logic and Switch Simulation 909
10.7.1 Logic-level Simulation 909
10.7.2 Switch-level Simulation 913
10.7.3 Hardware Logic Simulation 917

10.8 Timing Analysis 918
10.8.1 Timing Analysis Methodology 918
10.8.2 Timing Analysis Tools 919

10.9 Register-Transfer-Level Simulation 923
10.9.1 Simple RTL 923
10.9.2 ISPS Specification and Simulation 925
10.9.3 RTL Simulation with LISP 926

10.10 Hardware Design Languages 929
10.10.1 EDIF Design Description 930
10.10.2 EDIF Net List View of Full Adder 931
10.10.3 EDIF Mask Layout View of Full Adder 931
10.10.4 VHDL Design Description 935

10.11 Algorithmic Layout Generation 938
10.11.1 Bristle Blocks Silicon Compiler 938
10.11.2 MacPitts Silicon Compiler 941
10.11.3 Commercial Silicon Compilers 943

10.12 Summary 944
References 945
Problems 946

Index 951
Growing technological requirements and the widespread acceptance of sophisticated electronic devices have created an unprecedented demand for large-scale, complex, integrated circuits. Meeting these demands has required technological advances in materials and processing equipment, significant increases in the number of individuals involved in integrated circuit design, and an increased emphasis on effectively utilizing the computer to aid in the design.

Advances in growing fields, such as Very Large Scale Integrated Circuits (VLSI), generally parallel "graduate level" academic and industrial research efforts. As a result, these concepts quite naturally appear initially in university curricula at the graduate level. However, one must inevitably consider how to present this new material to a wider range of students with less sophisticated backgrounds. Integrated circuit design of LSI and VLSI systems is an area where both the required technical background and demand indicate that the material can and should be introduced at the undergraduate level. It is the purpose of this text to accomplish this objective.

The textbook has grown out of notes prepared for a one-semester senior level course that presents the fundamentals of integrated circuit design. This course has been offered every semester at Texas A&M University since the fall of 1981. Sufficient technical background for this text can be provided by an introductory level circuits course and an introductory digital logic course. Limited knowledge of material covered in an introductory electronics course is also assumed, but those sections requiring this knowledge can be either skipped or be augmented by the instructor without a major loss of continuity.

Each semester, students in the course participate in an integrated circuit design project using the multiprocessor chip (MPC) approach. Both NMOS and CMOS technologies have been used for the MPC. Process discussions closely parallel those available through the MOSIS program, thus facilitating participation in the MOSIS fabrication program by students who have MOSIS access. Past design projects have been intentionally limited in scope to keep the student's time...
commitments at a reasonable level. Past projects have included ring oscillators, PLAs, flip-flops, simple comparators and operational amplifiers, and 16-bit static RAMs. Although the availability of the processing capability helps provide an appreciation of all the details involved in the design of an integrated circuit, the material in this text is designed to be useful with or without access to foundary services.

The text includes a qualitative discussion of semiconductor processing in order to make the student cognizant of the processing steps required. Beyond this, a set of process parameters used in device modeling are assumed to serve as the interface between the process and the design engineers. The physical relationship between circuit design and actual silicon layout and area is strongly emphasized as is the anticipated performance of the circuit as affected by typical variations in the process parameters, temperature, and so on.

This book adopts the philosophy that the design engineer should be comfortable with either analog or digital circuitry and that the basic differences in the fundamental blocks are minimal. Integrated circuit design is presented as a systematic merging of a set of design rules, device models, and process parameters in a personnel- and area-efficient manner to develop a circuit that meets required electrical specifications. With this approach, the NMOS, CMOS, Bipolar, thick film, and thin film technologies are introduced in parallel. Each of these maintains a uniqueness through a specific set of design rules and device models. Advantages and tradeoffs in regard to area, performance, and processing costs among the technologies are considered. A typical set of design rules and a list of process parameters, sufficient for actual design, are given for each of the processes. These characteristics are used to maintain proper performance perspectives and to make that crucial link between circuit schematic and silicon layout. Since the size of components has been steadily decreasing, the design rules are given in terms of a variable, $\lambda$, whenever practical. Although design rules for the MOS and Bipolar processes scale quite well for typical 3, 5, and 8 micron processes, it is emphasized that the actual design rules and process parameters corresponding to the specific fabrication process employed should be adopted.

The ultimate goal of the circuit designer is not a clever circuit schematic or a computer simulation that predicts the circuit works as anticipated, but an efficiently designed physical piece of silicon that satisfies the original specifications. To this end, practical considerations are discussed including limitations of device models, parasitic and nonlinear effects, and clever component placement on the circuit layout, along with their effects on performance.

This book is directed to individuals with no previous integrated circuit design experience who need a working understanding of the subject. The text will also provide a broadened perspective for experienced designers. In addition to the university classroom, this text should find application in industrial training programs, as an interface for groups using or planning to use silicon foundries, and as a resource for the non-semiconductor-based industries that use electronic circuitry and must make the decision of when, if, and how to integrate their systems. It may also serve as a reference book on the subject of integrated circuit design.
Chapter 1 presents an overview of the field of integrated circuit design while focusing on past and present techniques, trends, and performance along with the technological challenges. A discussion of both yield and economics is included in this chapter.

Technology is discussed in Chapter 2. Processing steps are presented from a qualitative point of view, followed by detailed discussions of the NMOS, CMOS, and Bipolar processes along with the thick and thin film technologies. Design rules, layout techniques, and the role of the computer are discussed.

Models for the MOS and Bipolar transistors suitable for design are presented in Chapter 3, as are more sophisticated models necessary for computer simulation. The characteristics of various types of semiconductor passive components are also investigated.

Computer-aided circuit analysis is discussed in Chapter 4. Use of the widely available SPICE program for this purpose is investigated.

Chapter 5 is used to introduce basic analog building blocks.

Building blocks that are useful for constructing analog circuits are discussed in Chapter 6. Both MOS and Bipolar versions are developed in parallel because of the similarity of the circuit topologies.

A digital counterpart to Chapter 5 is presented in Chapter 7. This discussion originates with the inverter, followed by the generation of basic logic gates. Methods of driving large external loads while maintaining acceptable speed are investigated. The emphasis in Chapter 7 is on the MOS technologies because of their widespread acceptance for large digital systems.

In Chapter 8, the design of analog systems is considered. These systems employ some of the basic building blocks discussed in Chapters 5 and 6. Systems considered include A/D and D/A converters, continuous-time filters, switched-capacitor filters, oscillators, multipliers, and modulators.

Digital systems are discussed in Chapter 9. These include PLAs, gate arrays, static and dynamic memories, microprocessors, and systolic arrays.

Design automation is addressed in Chapter 10. The variety of design aids necessary for layout verification is discussed.

Much of the material in the book comes as an outgrowth of the design and testing of integrated circuits that have been included on past MPCs as well as the instruction that has been necessary to prepare students to participate in these designs. The fabrication of the MPCs by Texas Instruments, Inc., and the MOSIS Program is gratefully acknowledged.

McGraw-Hill and the authors would like to thank the following reviewers for their many helpful comments and suggestions: Jorge J. Santiago-Aviles; Steven Biblyk, Ohio State University; David J. Dumin, Clemson University; Yu Hen Hu, University of Wisconsin; David L. Landis, University of South Florida; H.C. Lin, University of Maryland; M.A. Littlejohn, North Carolina State University; R.A. Saleh, University of Illinois; S.M. Sze, AT&T Bell Laboratories; and Herbert Taub, City College of the City University of New York.

Randall L. Geiger
Phillip E. Allen
Noel R. Strader