EE 508
Switched Capacitor Amplifiers and Filters

Capacitor ratios can be very accurately controlled in an integrated circuit with the right sizing and layout strategies and thus they offer potential for making precision amplifiers. The good matching properties also is attractive for building filters. The most natural structure for a capacitor-based amplifier is shown in Fig. 1 where, if the op amp is ideal, the gain of the circuit is

$$A_V = \frac{V_{OUT}}{V_{IN}} = -\frac{C_1}{C_F} \qquad (1)$$

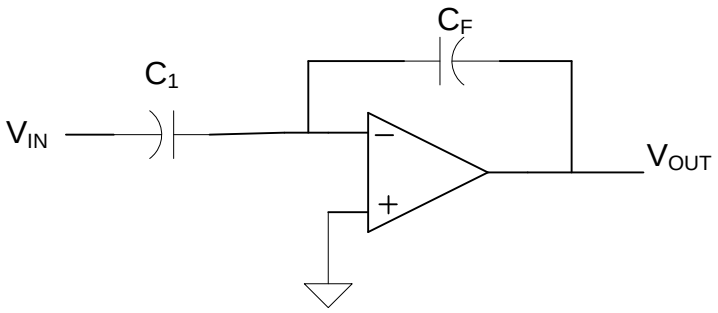


Figure 1 Voltage Amplifier with Capacitive Beta Feedback Network

It is argued that since the capacitor ratio can be very accurately controlled, the gain of this amplifier can be very accurately controlled. Unfortunately, this circuit does not perform as desired. Invariably there will be a small bias current drawn from the input terminals of the Op Amp. This bias current will cause charge to accumulate on the node connecting C_1 and C_F and this accumulation of charge will eventually (maybe after a few msec) cause the output of the op amp to saturate even if the capacitors were initially uncharged when power was applied to the circuit.

But a variant of this amplifier is shown in Fig. 2. This is termed a charge-redistribution amplifier or a switched-capacitor amplifier. The switches are controlled by ϕ_1 and ϕ_2 which are nonoverlapping clock signals. If a sinusoidal input is applied, the frequency of the two clock signals is usually much larger than the frequency of the input. The relationship between the period of the clock signals, T, and the input frequency is shown in Fig. 3. The nonoverlap of the clock signals themselves is shown in Fig. 4. In this amplifier, the feedback capacitor is discharged during phase ϕ_1 and charge proportional to V_{IN} is stored on C_1. A the end of phase ϕ_1 this charge is sampled onto C_1. At the start of phase ϕ_2 this charge is transferred to C_F and the output voltage becomes

$$V_{OUT} = -\frac{C_1}{C_F} V_{IN} \qquad (2)$$

Thus during phase ϕ_2 the output signal is an amplified version of the input signal with gain equal to $A_V = -\frac{C_1}{C_F}$. The output signal is, however, valid only during phase ϕ_2. The fact that the output is valid only during phase ϕ_2 is not a major limitation and the gain can be accurately controlled with the capacitor ratio.

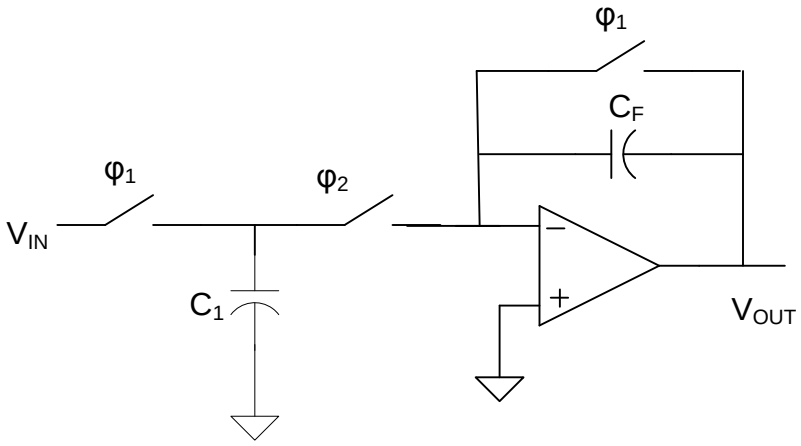


Figure 2 Basic Switched Capacitor Amplifier

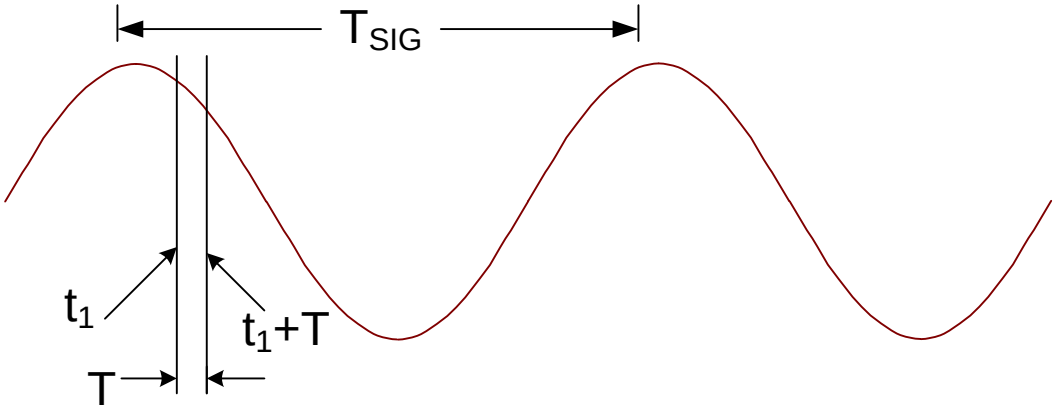


Figure 3 Timing of Switched Capacitor Clock and Input Signals

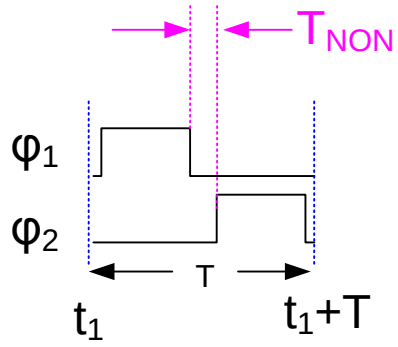


Figure 4 Non-overlapping Complimentary Clock Signals

The SC amplifier circuit of Fig. 2 works well in discrete form where the parasitic capacitors can be relatively small but in integrated form, the parasitic capacitance from the top plate of C1 also transfers charge to the output thus limiting the accuracy. Two variants of the SC amplifier that are insensitive to the parasitic capacitances are shown in Fig. 5. These are termed stray-insensitive amplifier. One has an inverting gain and one a noninverting gain. The signals ϕ_{1A} are termed "advanced" clock signals with the switch ϕ_{1A} opening slightly in advance of the switch $\phi_{1.}$ The advanced clock signal effectively eliminates the signal-dependent delay associated with the slewing of the clock signals.

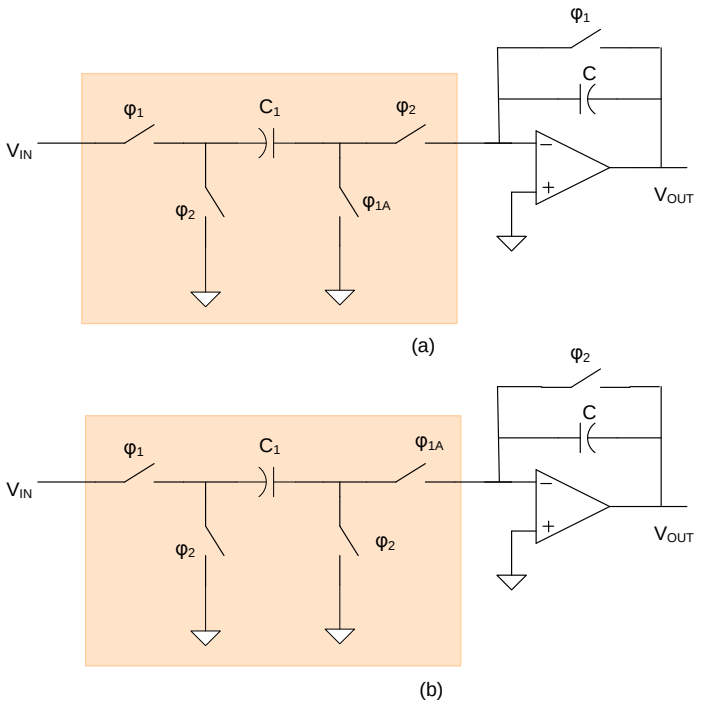


Figure 5 Stray Insensitive Switched Capacitor Amplifier a) noninverting, b) inverting

Switched capacitor circuits can also be used to build filters. It can be shown that a rapidly switched capacitor acts like a resistor. The basic building block in most SC filters is the SC integrator. A switched capacitor integrator is shown in Fig. 6 along with a continuous-time integrator.

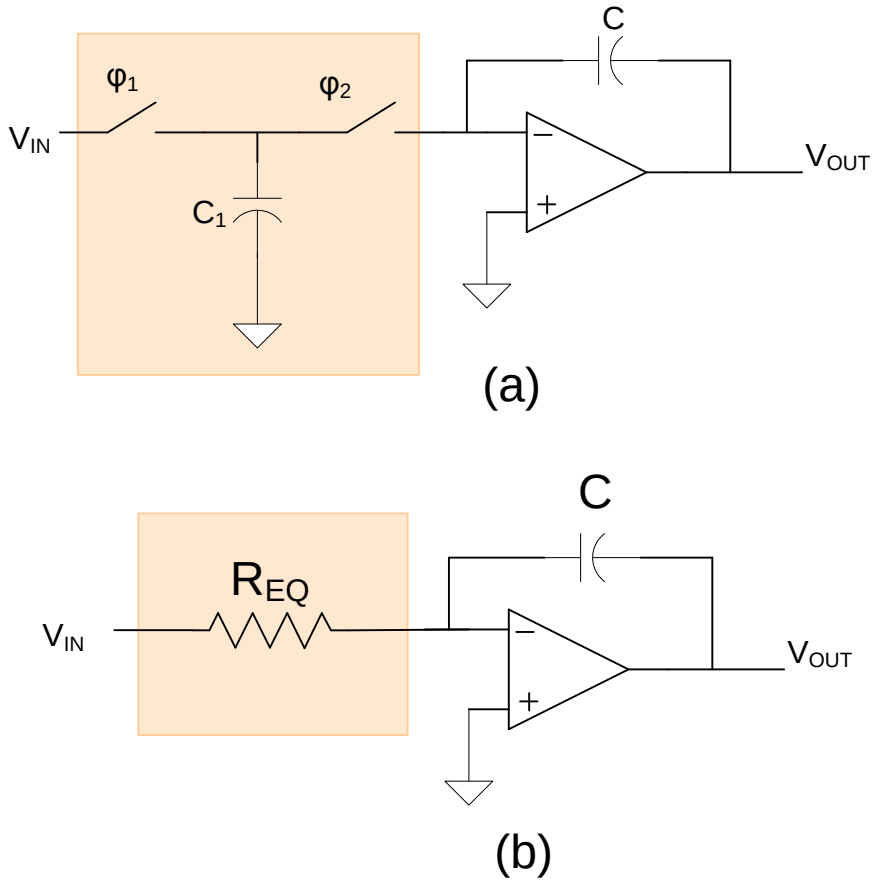


Figure 6 Integrators a) Switched-Capacitor Integrator b)RC Integrator

The switched capacitor block in Fig. 6a, when rapidly switched, performs nearly the same as a resistor in the sense that in any clock period, both transfer charge to the output capacitor that is proportional to V_{IN}. The equivalence is depicted in Fig. 7. The approximate equivalence is given by the expression

$$R_{EQ} = \frac{T_{CLK}}{C_1} = \frac{1}{C_1 f_{CLK}} \qquad (3)$$

The subscript "CLK" has been added to the period of the clock signal T to emphasize that it is the clock signal.

Thus, the unity gain frequency to the two integrators are given by

$$I_{0RC} = \frac{1}{RC}$$

$$I_{0RC} = f_{CLK}\frac{C_1}{C} \qquad (4)$$

The switched capacitor integrator offers two major advantages over the continuous-time integrator. First, large resistors correspond to small capacitors. It can be readily shown that this property makes integrated audio frequency SC filters viable. The second is accuracy. Since the capacitor ratio can be accurately controlled and since the clock frequency can be generated from an external crystal, the accuracy of integrated SC filters can be very good.

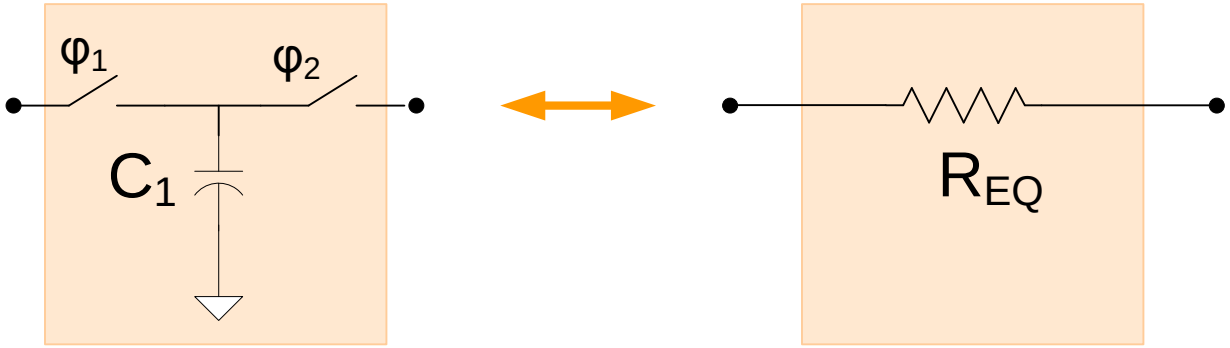


Figure 7 Equivalence of switched capacitor to a resistor for high clock frequencies

In integrated form, the SC integrator of Fig. 6 is plagued with parasitic capacitances in the same way the SC amplifier of Fig. 2 was plagued. Stray insensitive inverting and noninverting integrators are shown in Fig. 8. These are widely used in integrated form.

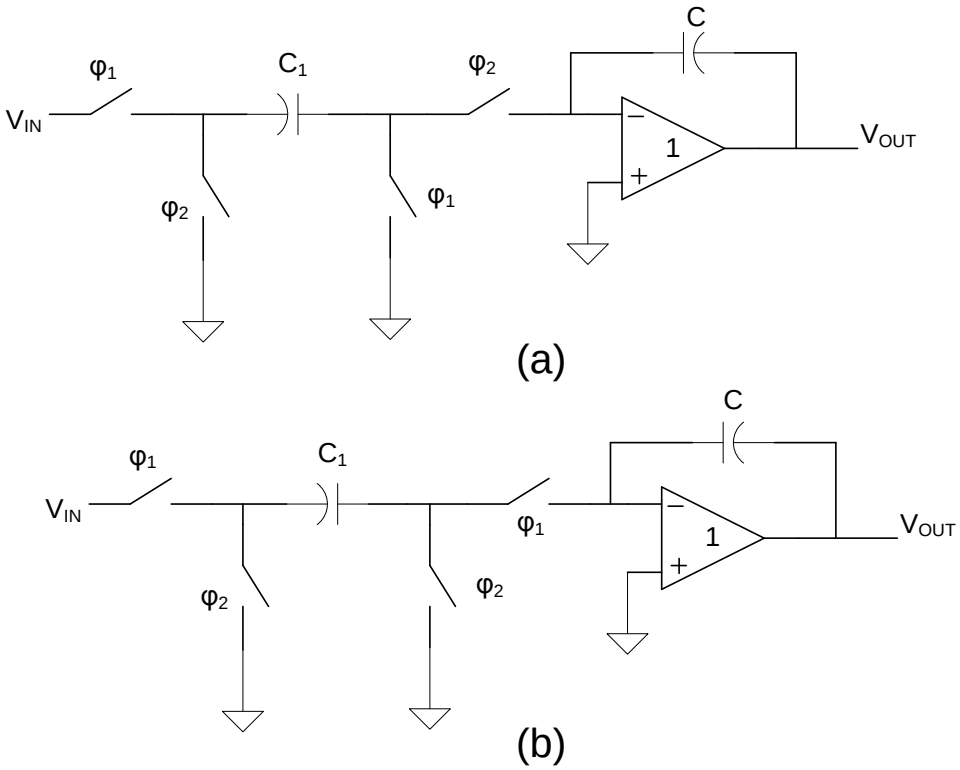
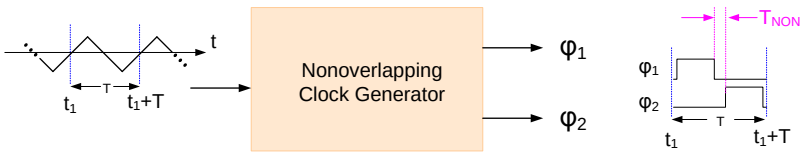


Figure 8 Stray Insensitive Switched Capacitor Integrators a) Noninverting b) Inverting

Laboratory Procedure

Part 1 Design a nonoverlapping clock generator using 741 op amps that has a programmable clock frequency with a non-overlap time (T_{NON} in Fig. 4) of approximately 10% of the period. A triangular 10Vpp triangular waveform should serve as the input to the clock generator and the two nonoverlapping phases ϕ_1 and ϕ_2 should appear at the output. ϕ_1 and ϕ_2 should nominally swing between 0V and 5V. The frequency of the nonoverlapping clock generator should be controlled by the frequency of the triangular signal. You might want to pass the output of your clock generator through a Schmitt Trigger (e.g. 74HC14 or 74HC17) to sharpen the output transitions.



Part 2 Design and test a Switched Capacitor Amplifier that has a voltage gain of -20. Use either the MAX 326 or the MAX 364 analog switches. Use a 100KHz clock and the nonoverlapping

clock generator developed in Part 1 of this experiment. Use 741-type op amps. Compare the 3dB bandwidth of the switched capacitor amplifier with that of a continuous-time inverting amplifier that has the same gain but uses the standard two-resistor beta network for feedback.

Part 3 Design and test the performance of a switched-capacitor inverting integrator and compare it with the standard active RC integrator. Assume both integrators are designed for a nominal unity gain frequency of 1KHz. Identify any challenges you find in measuring the performance of an integrator and point out how you addressed these challenges in your measurements. (Hint: You may want to simulate the transient response of an ideal integrator with 1KHz unity gain frequency for each of the following inputs: $V_{in1}=\sin(2000\pi t)$ and $V_{in2}=\sin(2000\pi t)+.00001V$ to see what happens)

Part 4 Design and test a second-order switched capacitor bandpass filter that has a peak frequency of 1KHz and a 3dB bandwidth of 200 Hz. Use the two integrator loop architecture.