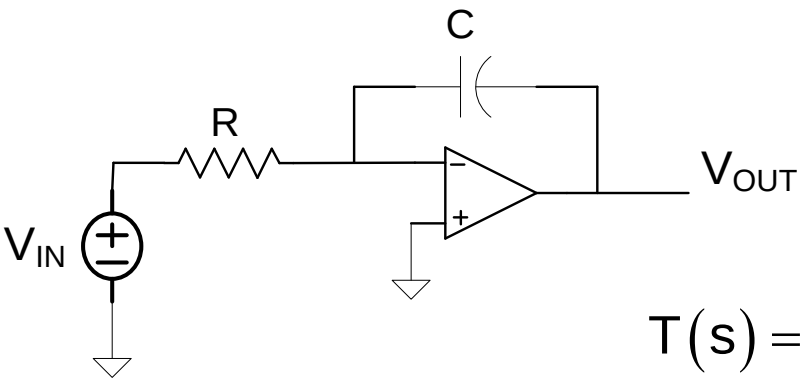
EE 508
Lecture 27

Integrator Design

Switched Capacitor Integrators

Review from last time

Consider the Basic Integrator



$$T(s) = -\frac{1}{RCs}$$

$$I_0 = \frac{1}{RC}$$

1. Accuracy of R and C difficult to accurately control – particularly in integrated applications (often 2 or 3 orders of magnitude to variable)

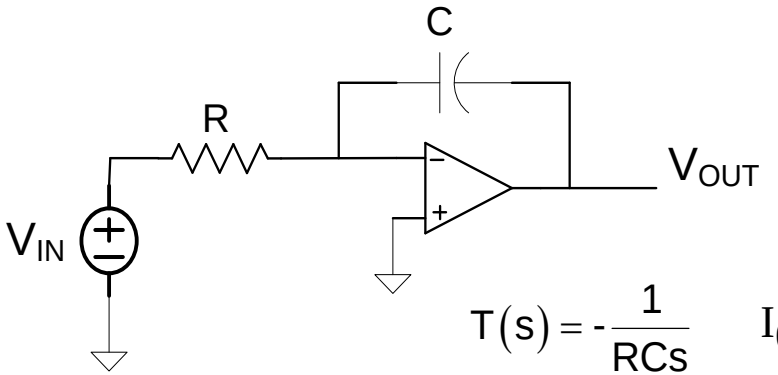
2. Size of R and C unacceptably large if I_0 is in audio frequency range (2 or 3 orders of magnitude too large)

3. Amplifier GB limits performance

Incredible Challenge to Building Filters on Silicon!

Review from last time

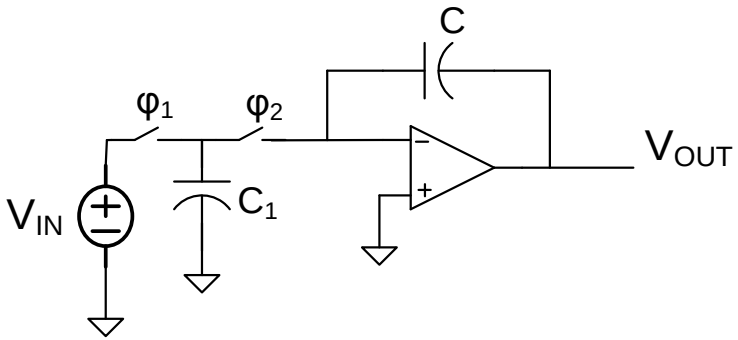
Switched-Capacitor Circuits

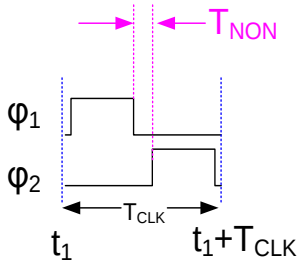


$$T(s) = -\frac{1}{RCs} \qquad I_0 = \frac{1}{RC}$$

Consider:

$$V_{IN} = V_M \sin(2\pi f_{SIG} t + \theta)$$





Assume $T_{CLK} << T_{SIG}$

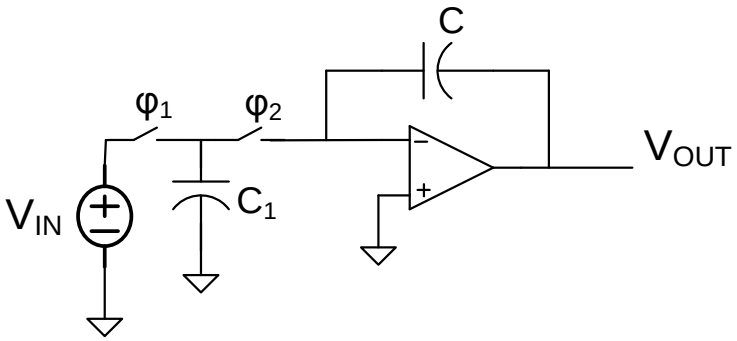
Φ_1 and Φ_2 are complimentary non-overlapping clocks

Φ_1 and Φ_2 are periodic signals "clocks" shown for one period

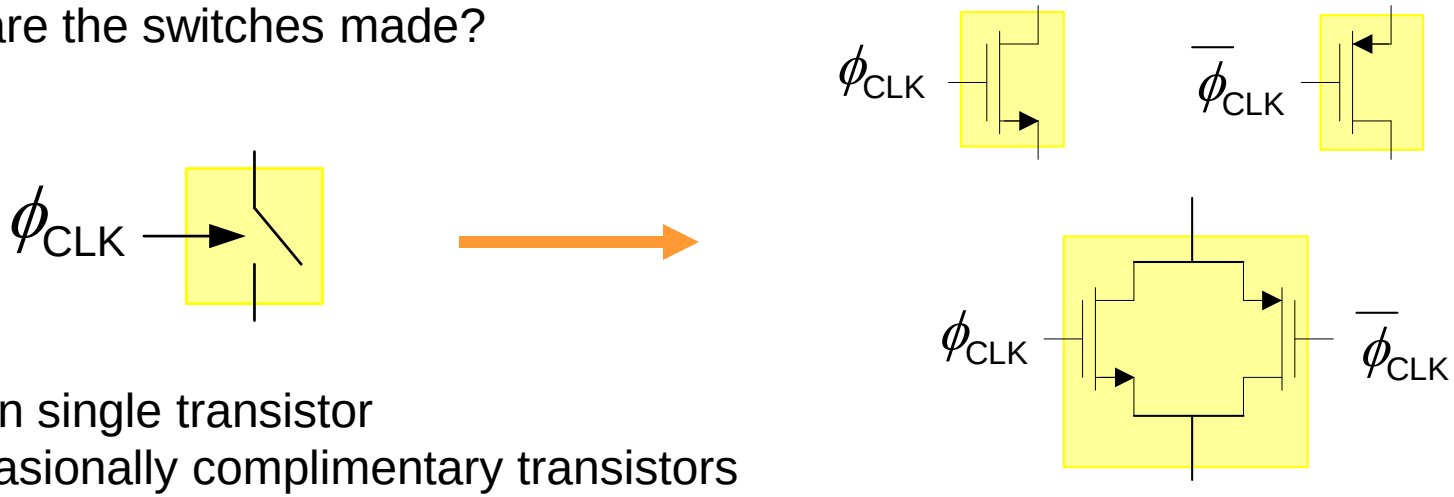
Termed a Switched-Capacitor circuit

Review from last time

Switched-Capacitor Circuits



How are the switches made?

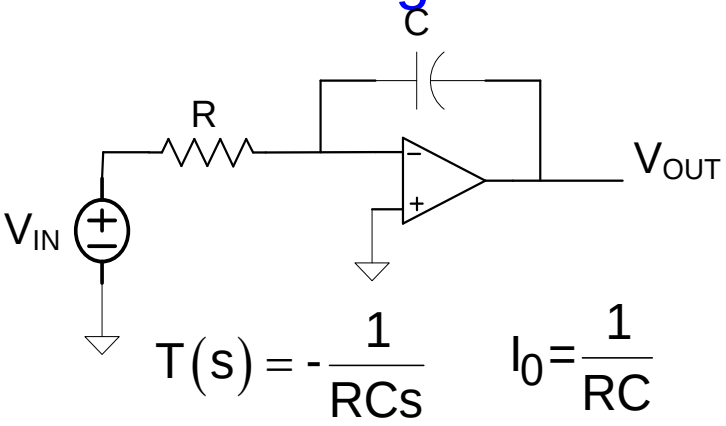


- Often single transistor
- Occasionally complimentary transistors
- On rare occasion more complicated
- Area overhead for switches small, clock routing a little more of concern
- Sizing of devices is important
- Clocking of switches may be important

Although originating in SC filters, switched charge redistribution circuits widely used in other non-filtering applications

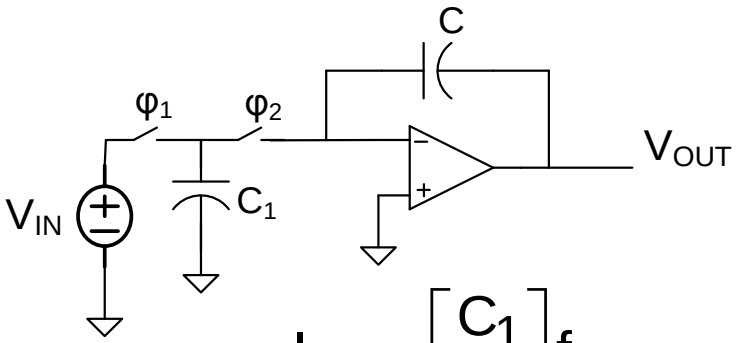
Review from last time

The SC integrator



$$T(s) = -\frac{1}{RCs} \qquad I_0 = \frac{1}{RC}$$

1. **Accuracy of R and C difficult to accurately control (often 2 or 3 orders of magnitude to variable)**
2. **Area of R and C too large in audio frequency range (2 or 3 orders of magnitude too large)**
3. **Amplifier GB limits performance**



$$I_{0eq} = \left[\frac{C_1}{C}\right] f_{CLK}$$

1. **Accuracy of cap ratio and f_{CLK} very good**
2. **Area of C1 and C not too large**
3. **Amplifier GB limits performance less**

Two of these properties were discovered independently by Gray, Broderson and Hosticka at Berkelev and by Copeland of Carelton

[1] J. T. Caves, M. A. Copeland, C. F. Rahim, and S. D. Rosenbaum, "Sampled analog filtering using switched capacitors as resistor equivalents," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 592–599, Dec. 1977.

[2] B. J. Hosticka, R. W. Brodersen, and P. R. Gray, "MOS sampled data recursive filters using switched capacitor integrators," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 600–608, Dec. 1977.

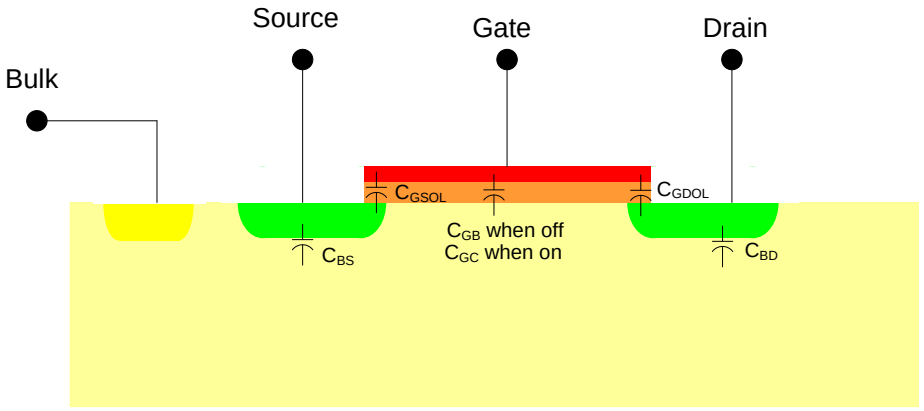
77 citations

108 citations

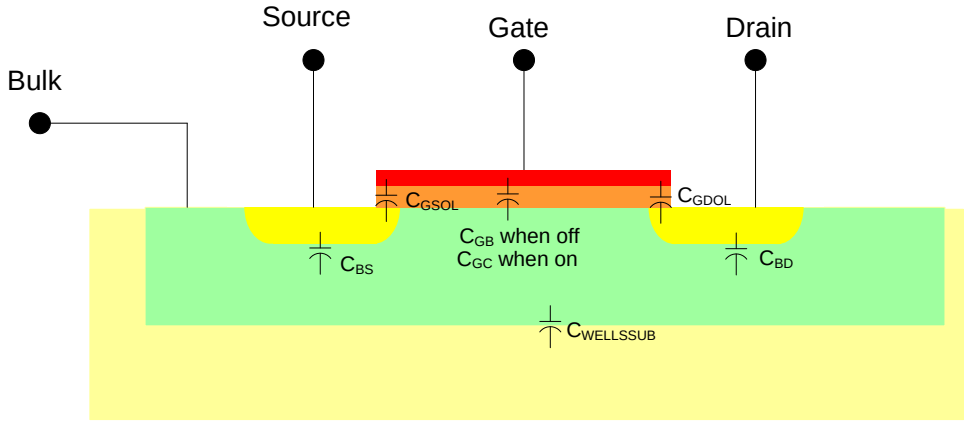
Seminal source of SC concept received few citations!

But cited as a key contribution when Brodersen and Gray elected to NAE

Parasitic Capacitors in MOS Transistors

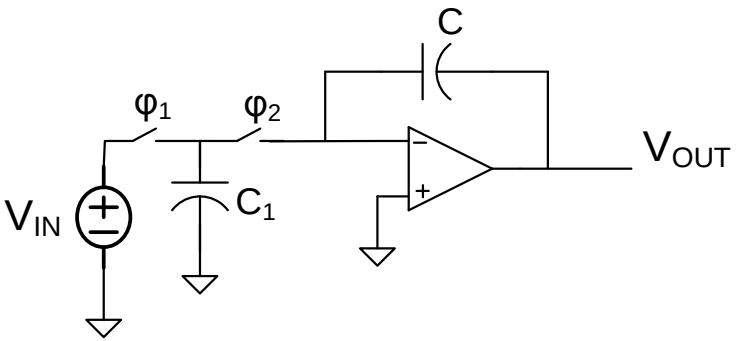


n-channel MOSFET



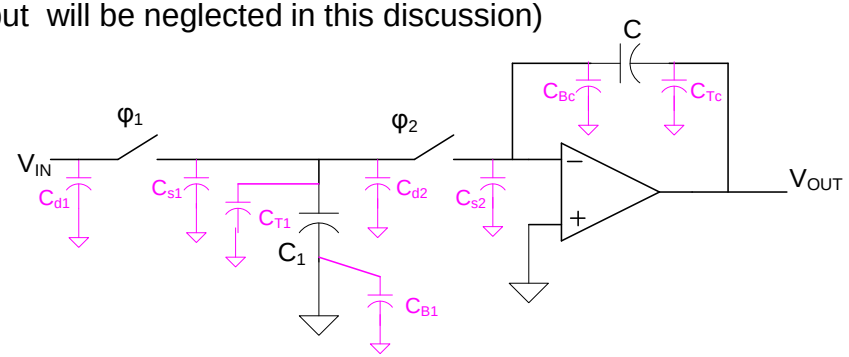
p-channel MOSFET

The SC integrator



$$I_{0eq}=\left[\frac{C_1}{C}\right]f_{CLK}$$

Observe this circuit has considerable parasitics (gate parasitics cause offset in this circuit and some signal-dependent distortion but will be neglected in this discussion)



$C_{1EQ}=C_1+C_{s1}+C_{d2}+C_{T1}$

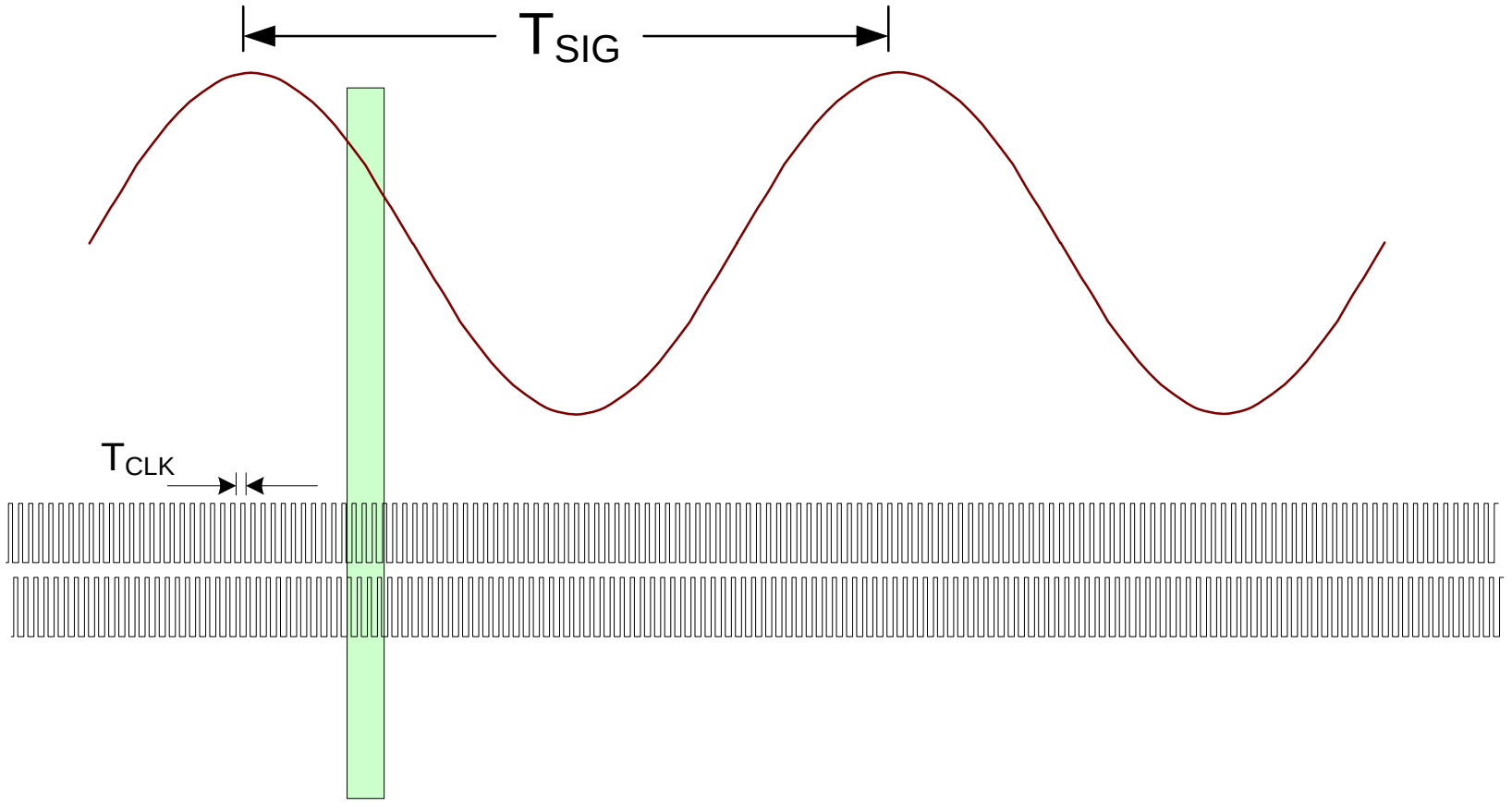
Parasitic capacitors $C_{s1}+C_{d2}+C_{T1}$ difficult to accurately match

- Parasitic capacitors of THIS SC integrator limit performance
- Other SC integrators (discussed later) offer same benefits but are not affected by parasitic capacitors

Switched-Capacitor Filter Issues

What if T_{CLK} is not much-much smaller than T_{SIG}?

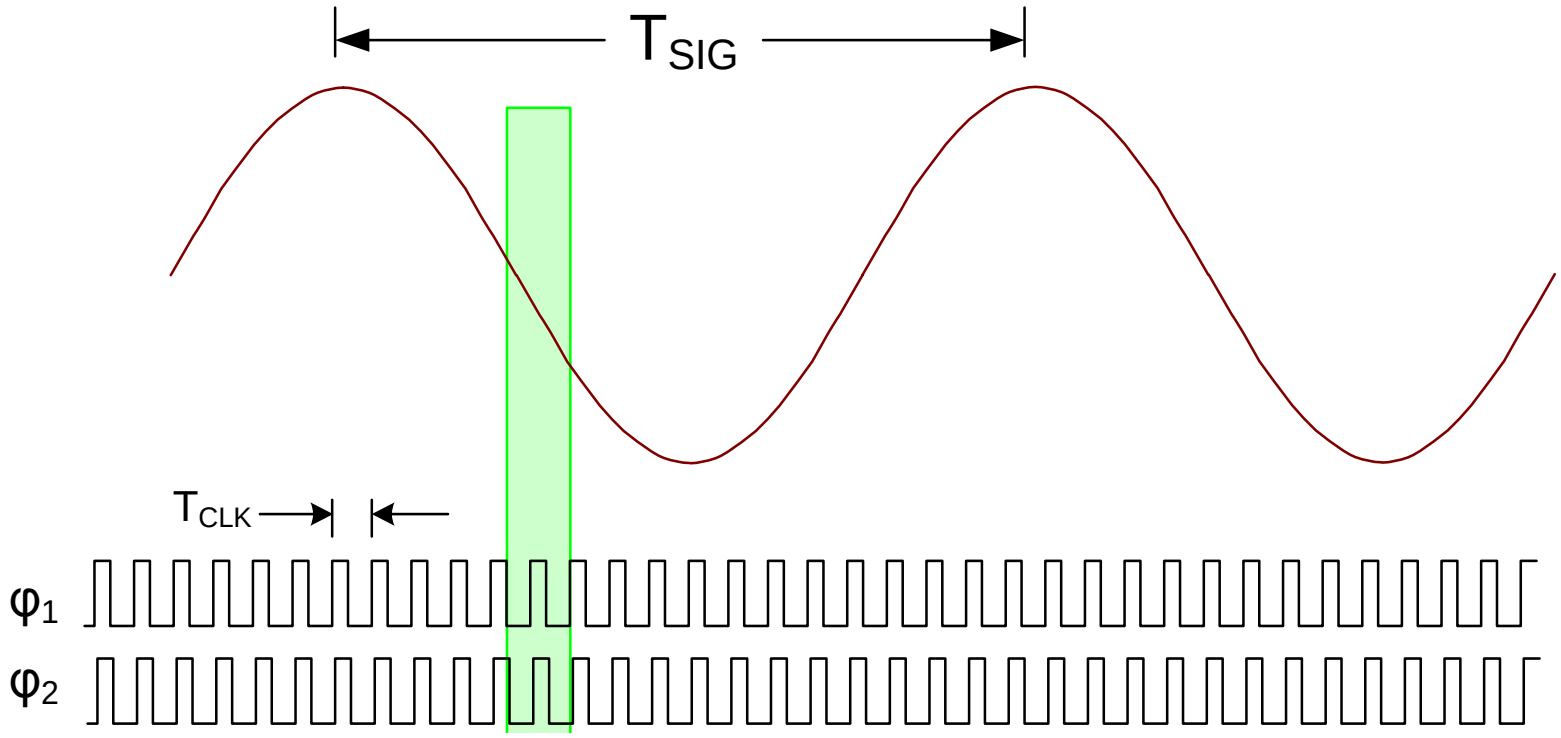
For $T_{CLK} << T_{SIG}$



Switched-Capacitor Filter Issues

What if T_{CLK} is not much-much smaller than T_{SIG}?

For $T_{CLK} < T_{SIG}$



Switched-Capacitor Filter Issues

What if T_{CLK} is not much-much smaller than T_{SIG}?

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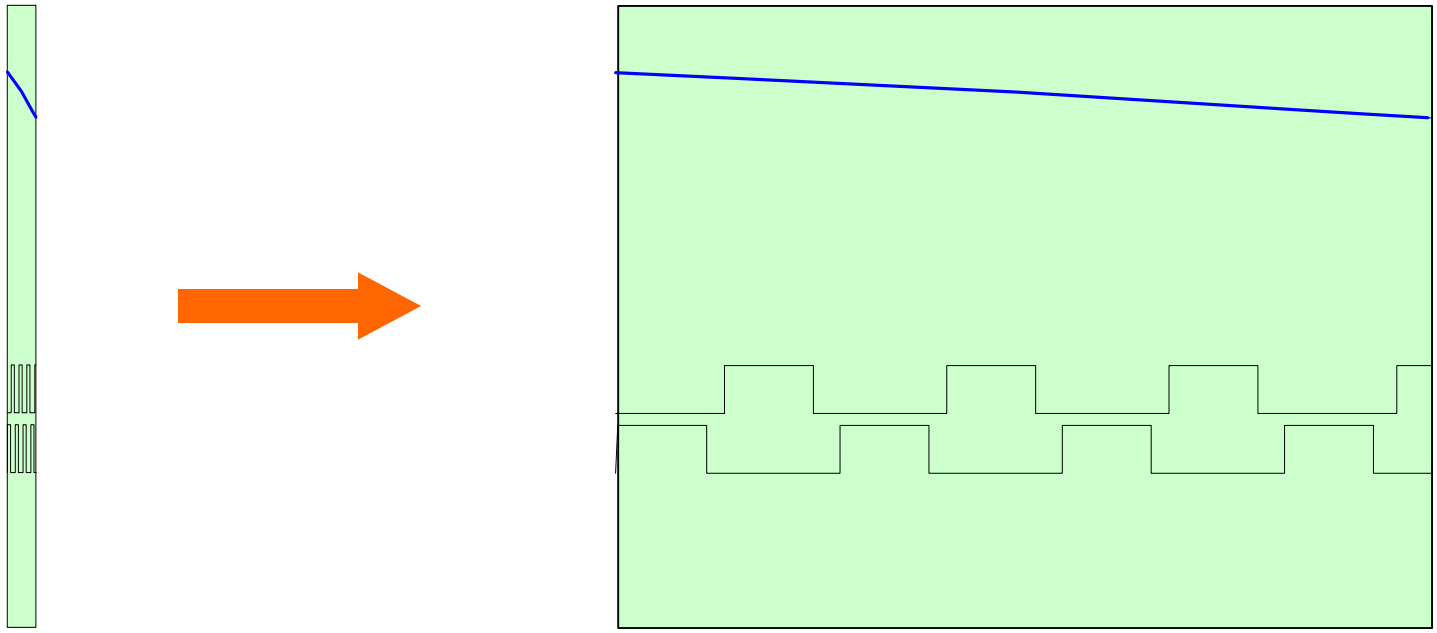
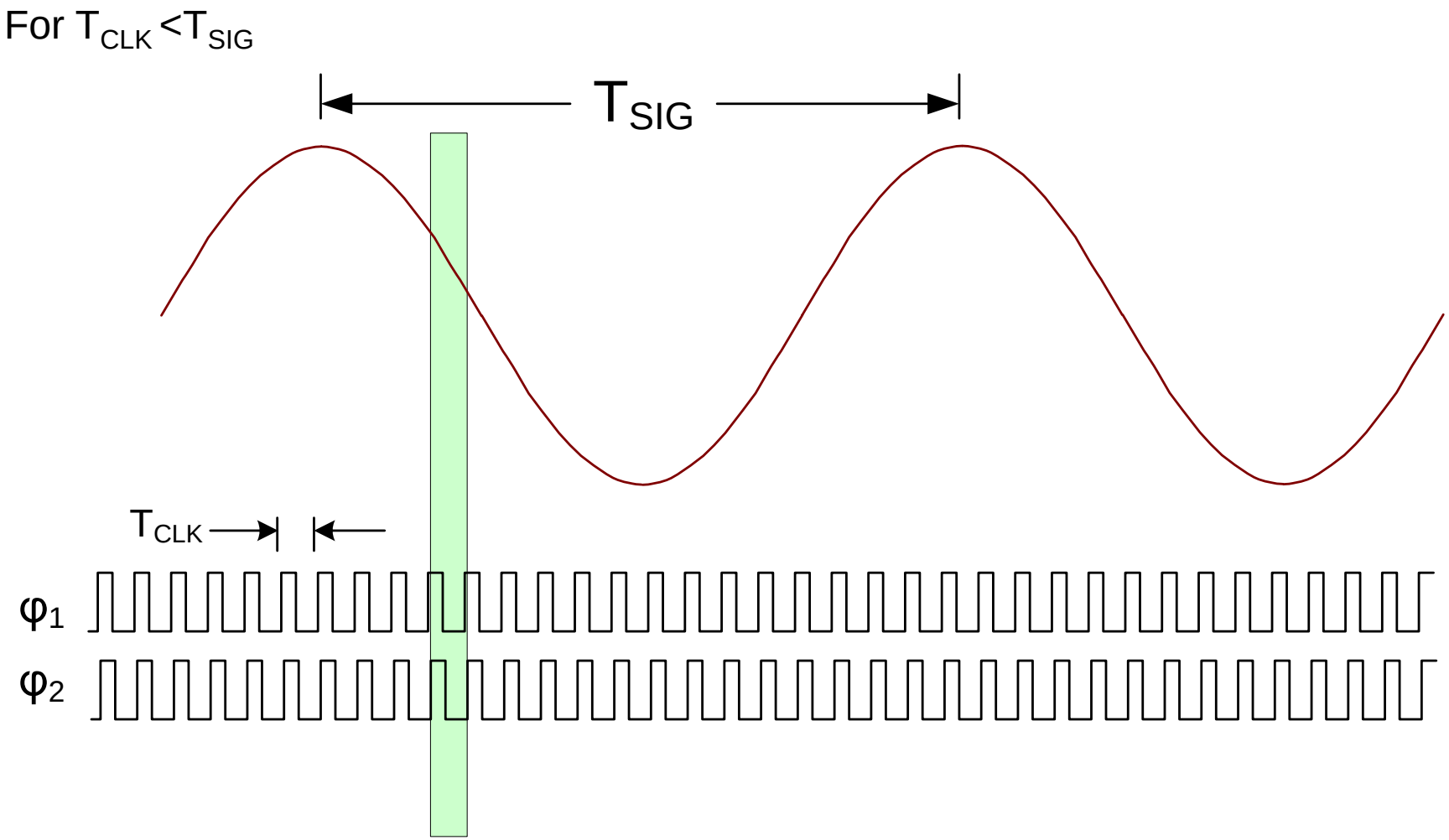


Switched-Capacitor Filter Issues

What if T_{CLK} is not much-much smaller than T_{SIG}?



Switched-Capacitor Filter Issues

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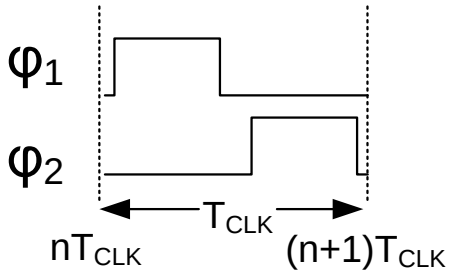
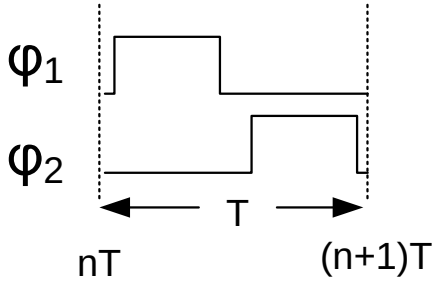
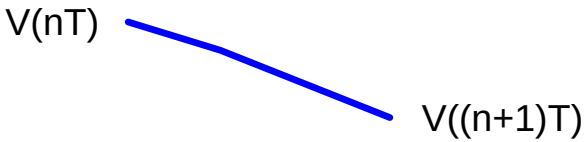
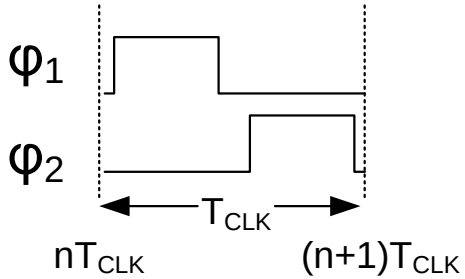


Define $T=T_{CLK}$

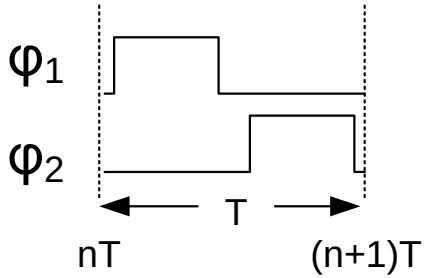


For $T_{CLK} < T_{SIG}$





Define $T=T_{CLK}$

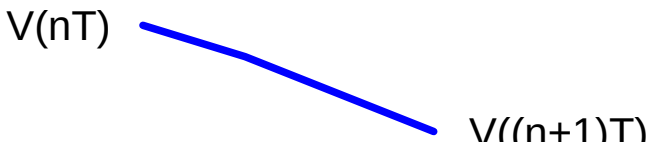


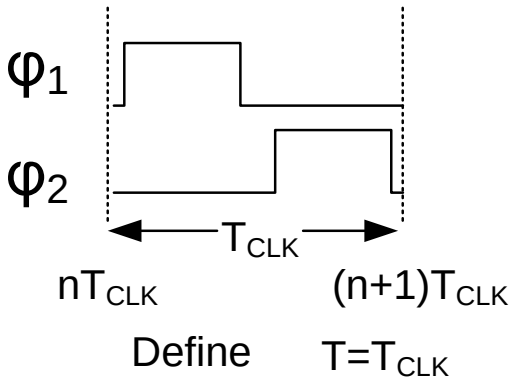
Considerable change in V(t) in clock period

Switched-Capacitor Filter Issues

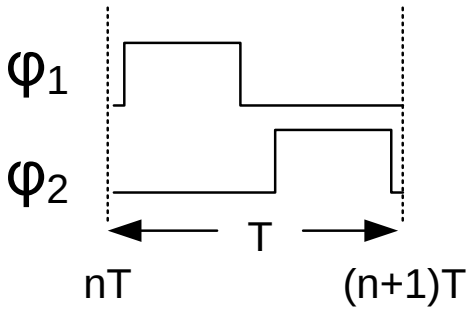
What if T_{CLK} is not much-much smaller than T_{SIG}?

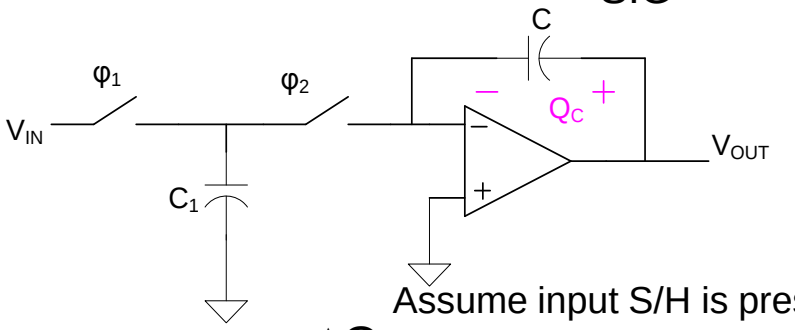
For $T_{CLK} < T_{SIG}$





Define $T = T_{CLK}$





Assume input S/H is present

$$V_0(nT+T) = V_0(nT) + \frac{\Delta Q_c}{C}$$

but $-Q_c$ is the charge on C_1 at the time φ_1 opens

$$-\Delta Q_c \simeq C_1 V_{IN}(nT+T/2)$$

$$\therefore V_{OUT}(nT+T) = V_{OUT}(nT) - (C_1/C) V_{IN}(nT+T/2)$$

Due to input S/H, V_{IN} constant over periods of length T thus, assume $V_{IN}(nT+T/2) \simeq V_{IN}(nT)$

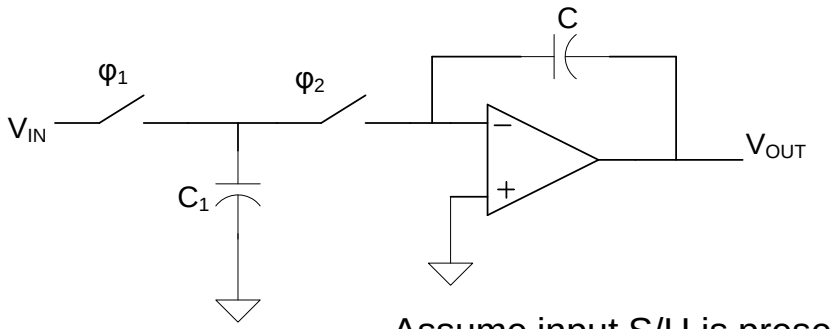
So obtain

$$V_{OUT}(nT+T) = V_{OUT}(nT) - (C_1/C) V_{IN}(nT)$$

How does this analysis differ from what we did earlier?

Switched-Capacitor Filter Issues

What if T_{CLK} is not much-much smaller than T_{SIG}?



Assume input S/H is present

$$V_{OUT}(nT+T)=V_{OUT}(nT)-(C_1/C)V_{IN}(nT)$$

for any T_{CLK}, characterized in time domain by difference equation

This can be characterized in the discrete-time frequency domain by transfer function obtained by taking z-transform of the difference equation

$$zV_{OUT}(z)=V_{OUT}(z)-(C_1/C)V_{IN}(z)$$

$$H(z)=-\frac{C_1/C}{z-1}$$

This is a standard integrator transfer function in the z-domain (but not unique)

Note pole at z=1

Switched-Capacitor Filter Issues

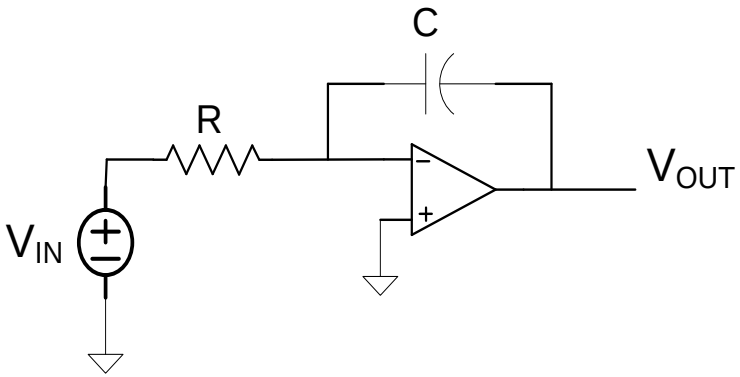
What if T_{CLK} is not much-much smaller than T_{SIG}?

Claim: The transfer function of any Switched-Capacitor Filter is a rational fraction in z with all coefficients in both the numerator and denominator determined totally by capacitor ratios

$$H(z) = \frac{\sum_{i=0}^{m} a_i z^i}{\sum_{i=0}^{n} b_i z^i}$$

What is really required for building a filter that has high-performance features?

Consider an integrator:



Frequency domain:

Transfer function

$$T(s) = -\frac{1}{RCs}$$

Time domain:

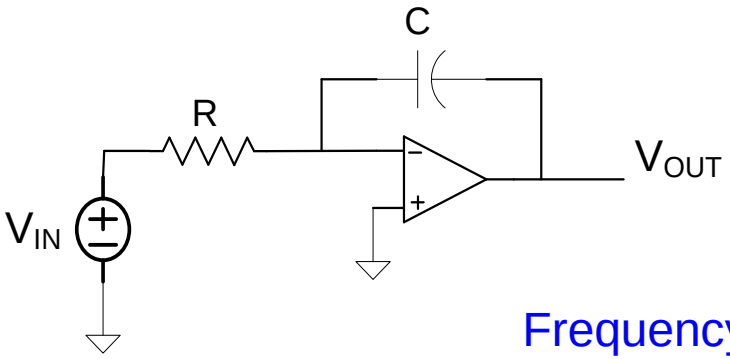
Differential Equation

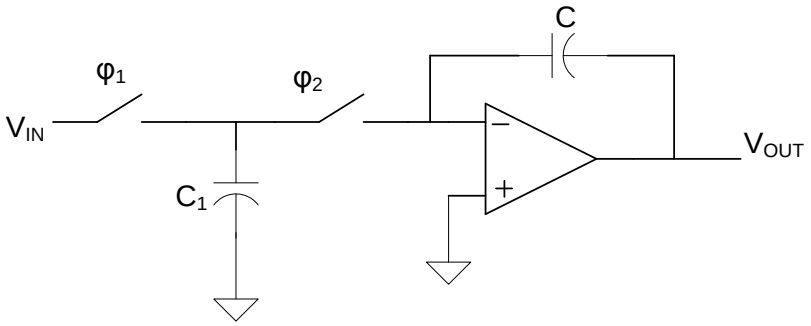
$$V_{OUT}(t) = V_{OUT}(t_0) - \frac{1}{RC}\int_{t_0}^{t} V_{IN}(\tau)\,d\tau$$

- Accurate control of polynomial coefficients in transfer function or accurate control of coefficients in the differential equation
- Absence of over-ordering terms due to parasitics

What is really required for building a filter that has high-performance features?

Consider continuous-time and discrete-time integrators:





Frequency domain:

Transfer function

$$T(s) = -\frac{1}{RCs}$$

$$H(z) = -\frac{C_1/C}{z-1}$$

Time domain:

Differential Equation

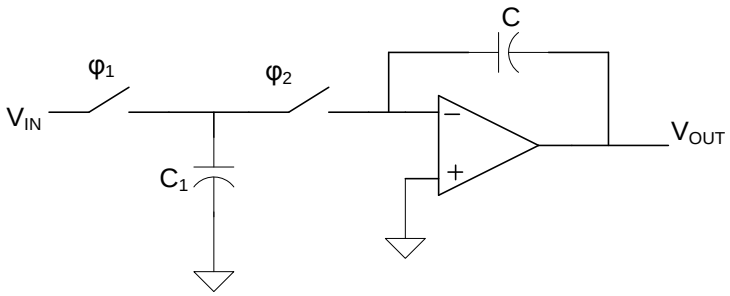
$$V_{OUT}(t) = V_{OUT}(t_0) - \frac{1}{RC}\int_{t_0}^{t} V_{IN}(\tau)\,d\tau$$

Difference Equation

$$V_{OUT}(nT+T) = V_{OUT}(nT) - (C_1/C)V_{IN}(nT)$$

- Accurate control of polynomial coefficients in transfer function or accurate control of coefficients in the differential/difference equation needed for good filter performance
- Absence of over-ordering terms due to parasitics

Switched-Capacitor Filter Issues



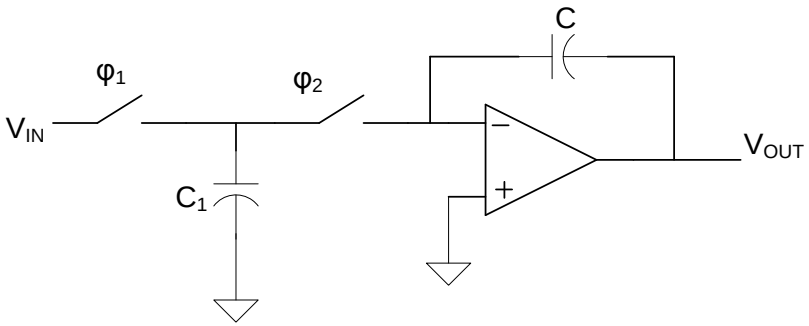
Transfer function of any SC filter of form:

$$H(z) = \frac{\sum_{i=0}^{m} a_i z^i}{\sum_{i=0}^{n} b_i z^i}$$

Switched-capacitor circuits have potential for good accuracy and attractive area irrespective of how T_{CLK} relates to T_{SIG}

But good layout techniques and appropriate area need to be allocated to realize this potential !

Switched-Capacitor Integrators

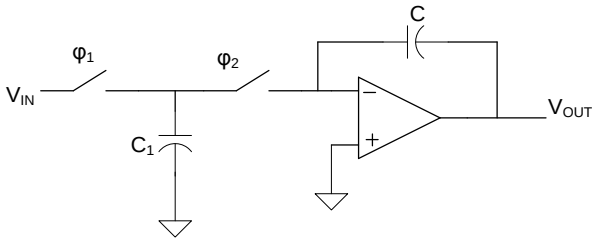


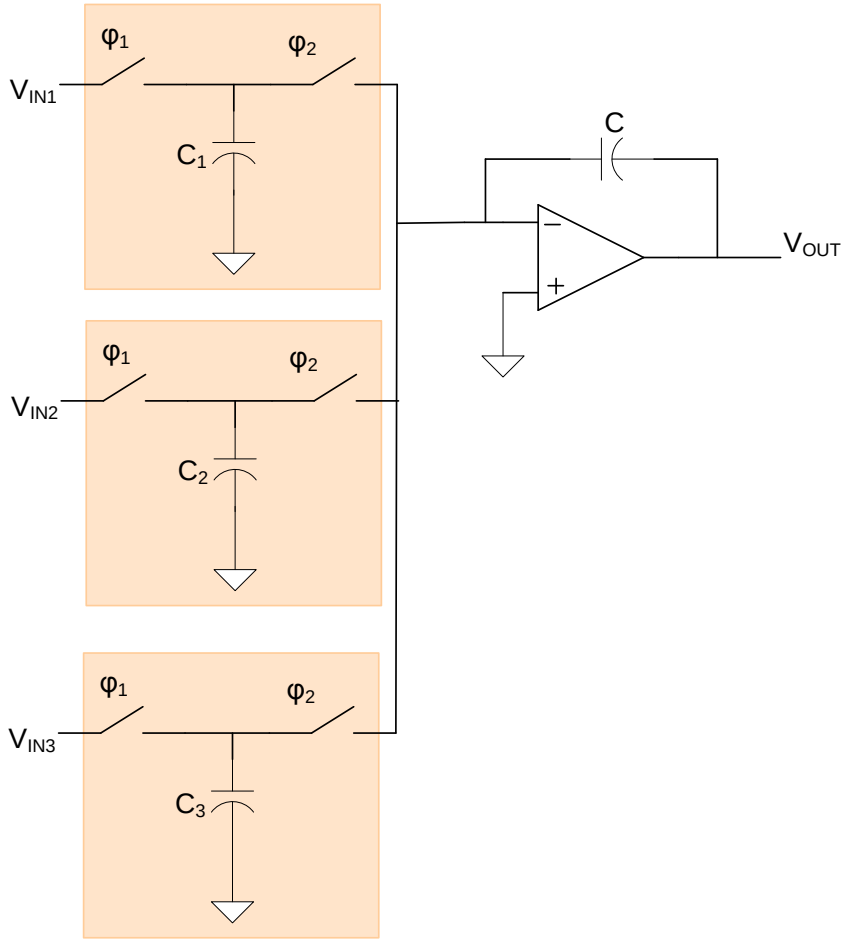
$$V_{OUT}(nT+T)=V_{OUT}(nT)-(C_1/C)V_{IN}(nT)$$

$$H(z)= -\frac{C_1/C}{z-1}$$

Sensitive to parasitic capacitances

Switched-Capacitor Integrators

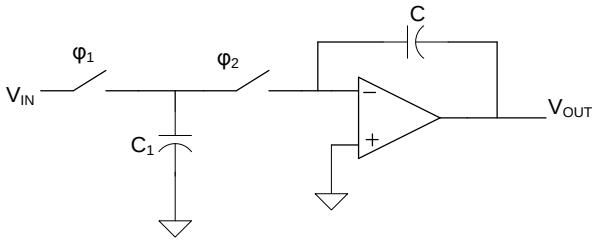


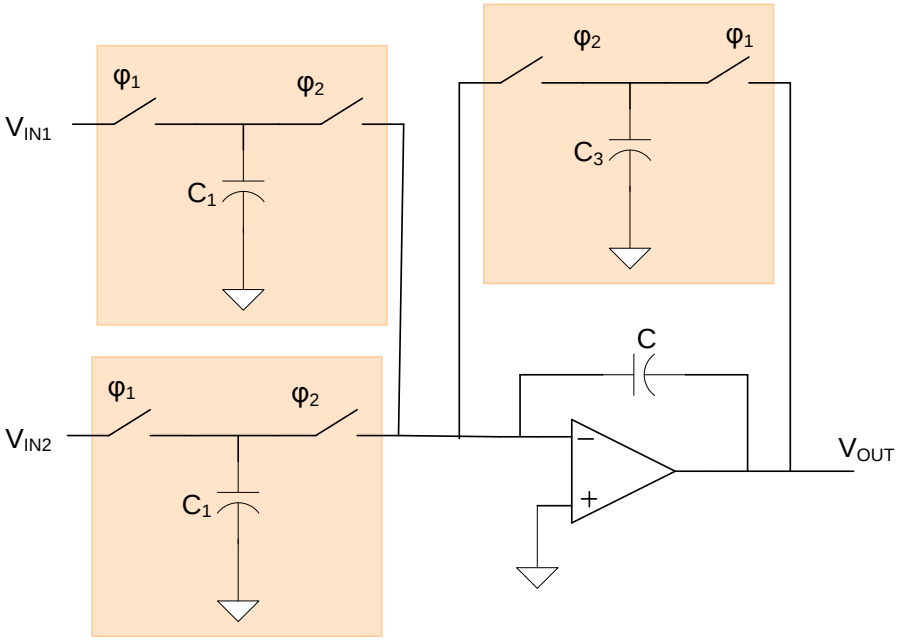


Summing Inputs

Sensitive to parasitic capacitances

Switched-Capacitor Integrators



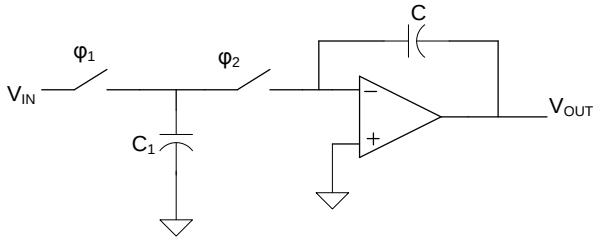


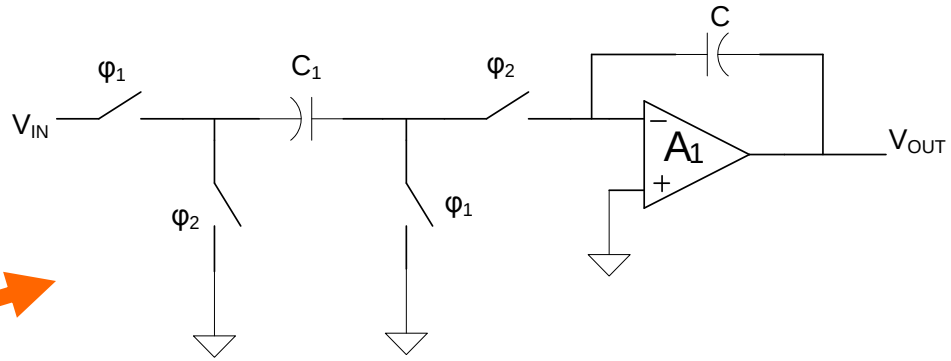
Summing Inputs and Lossy

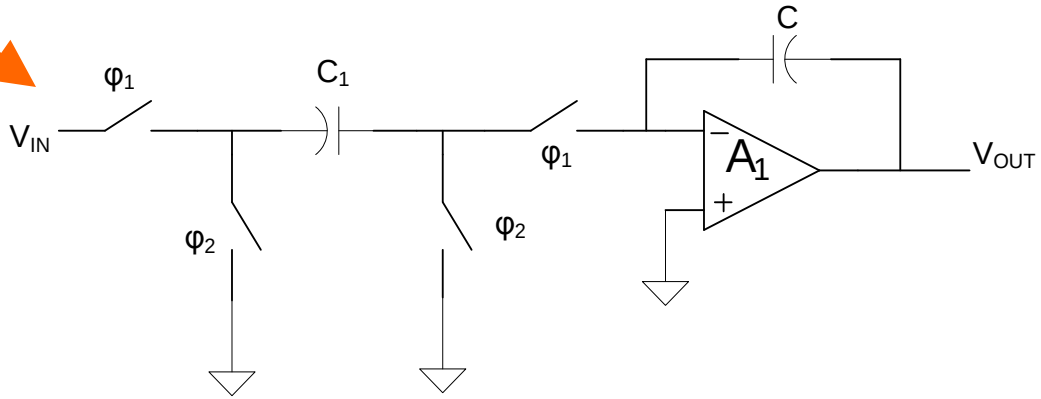
Sensitive to parasitic capacitances

Switched-Capacitor Integrators

Consider the following two SC circuits





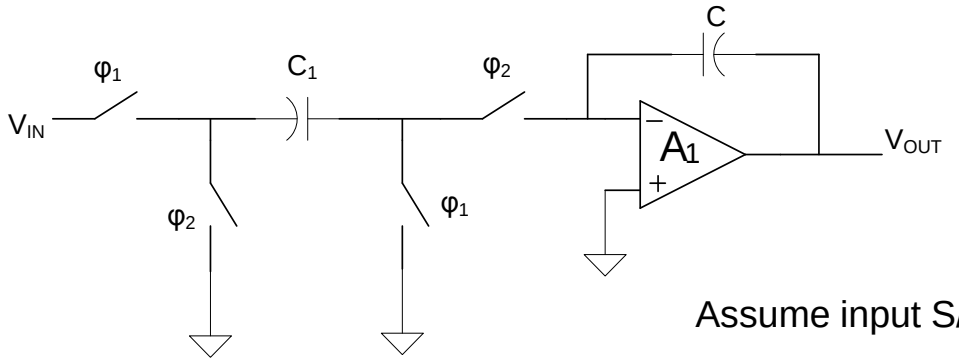


Still have two capacitors but twice as many switches !

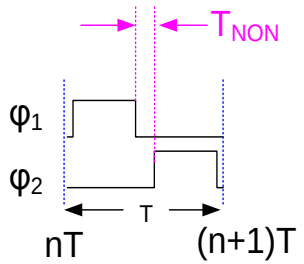
But switches can be pretty small !

Switched-Capacitor Integrators

Consider the first SC circuit



Assume input S/H



During phase Φ_1, capacitor V_{IN} is charged up to $V_{IN}(nT)$

During phase Φ_2, this charge is transferred to C and increasing V_{OUT}

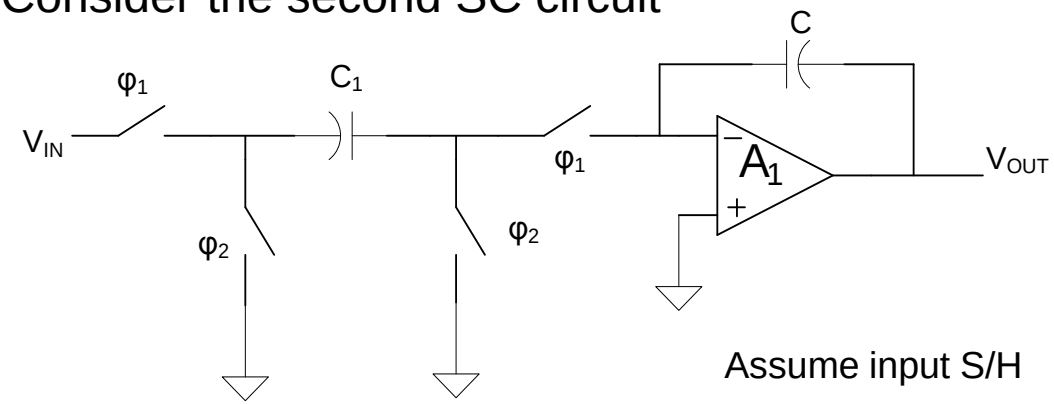
$$V_{OUT}(nT+T) = V_{OUT}(nT) + \frac{C_1}{C} V_{IN}(nT)$$

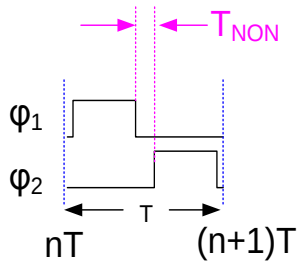
$$H(z) = \frac{C_1 / C}{z-1}$$

Serves as a non-inverting integrator

Switched-Capacitor Integrators

Consider the second SC circuit





Assume input S/H

Prior to the start of phase Φ_1, the capacitor C_1 was discharged by Φ_2

During phase Φ_1, capacitor V_{IN} charges up to $V_{IN}(nT)$

While charge is flowing into C_1, it is also flowing into C thus decreasing V_{OUT}

$$V_{OUT}(nT+T) = V_{OUT}(nT) - \frac{C_1}{C} V_{IN}(nT+T)$$

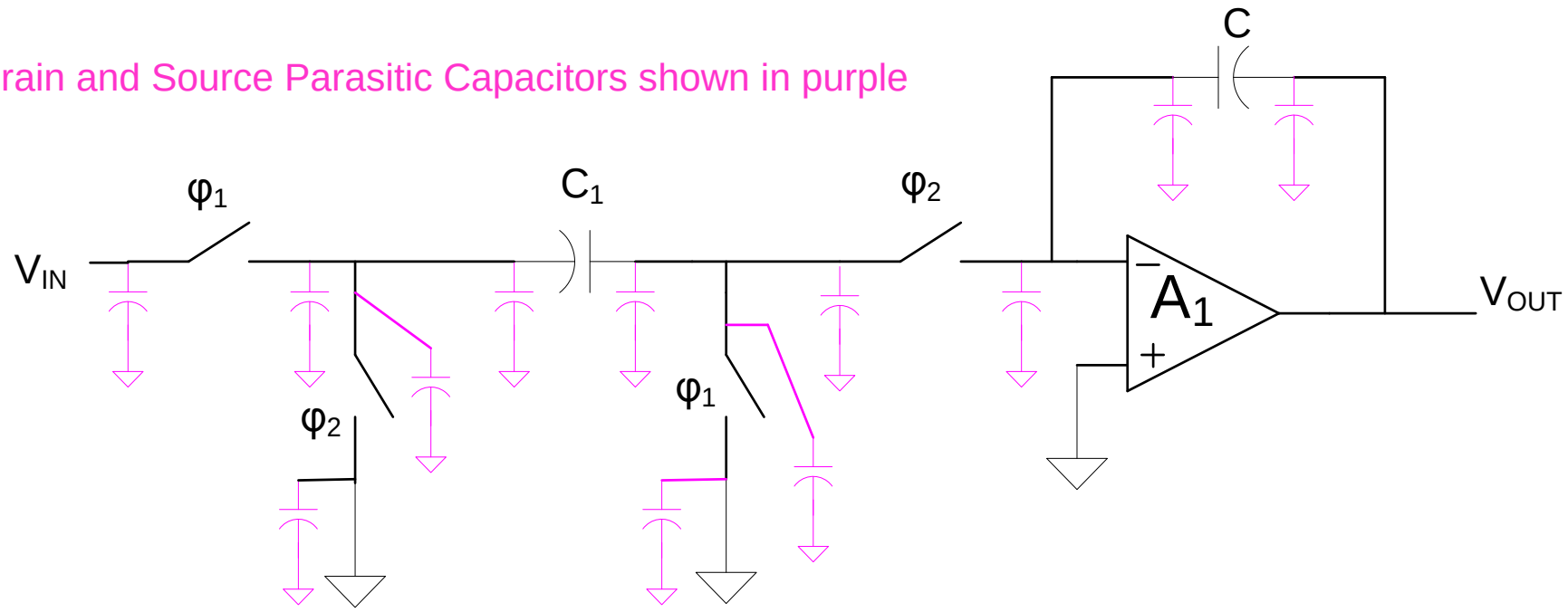
$$H(z) = \frac{z^{C_1/C}}{z-1}$$

Since $|z|_{z=e^{j\omega T}} = 1$

Serves as an inverting integrator

Switched-Capacitor Integrators

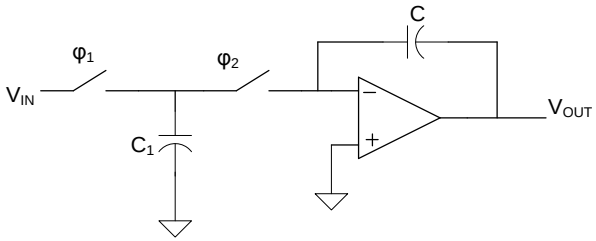
Drain and Source Parasitic Capacitors shown in purple

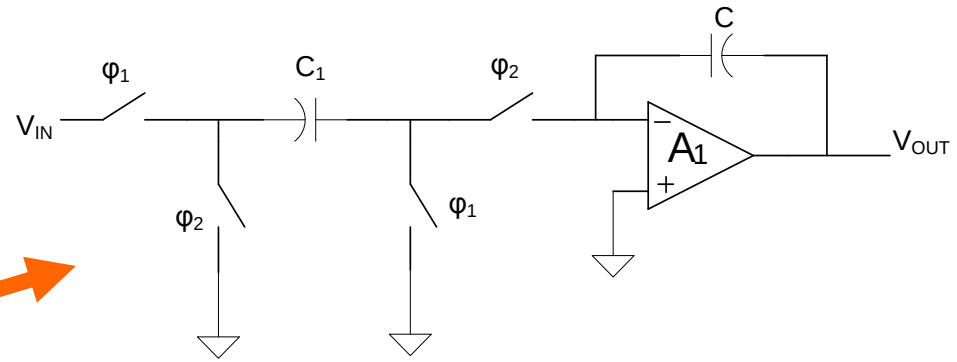


Stray-Insensitive Properties

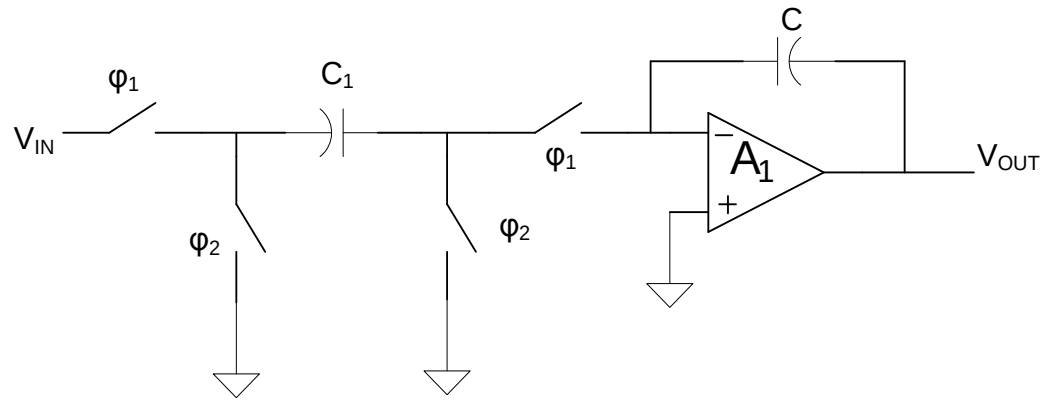
C_{GD} does not affect gain of integrator
$C_{GCHANNEL}$ doe not affect gain of integrator if switch not too fast

Switched-Capacitor Integrators





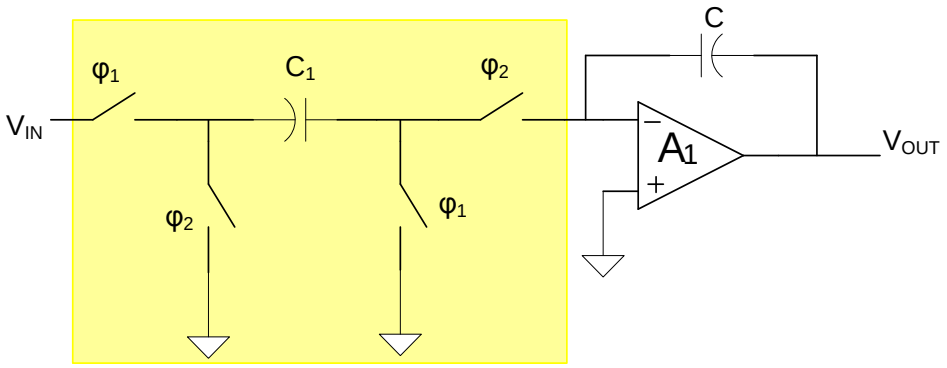
Stray-Insensitive Noninverting



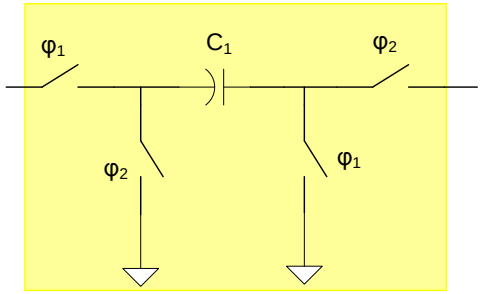
Stray-Insensitive Inverting

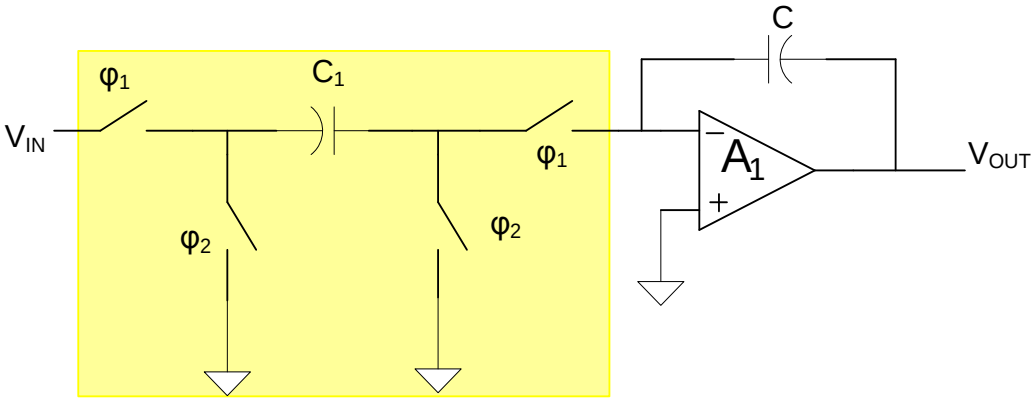
Switched-Capacitor Integrators

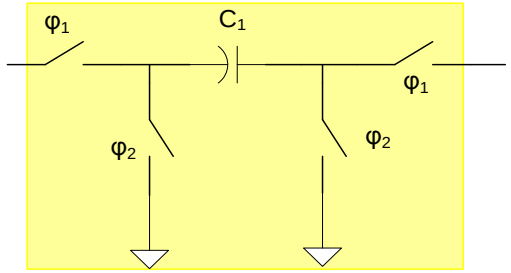
Stray-Insensitive SC Integrators



“Resistor Blocks”



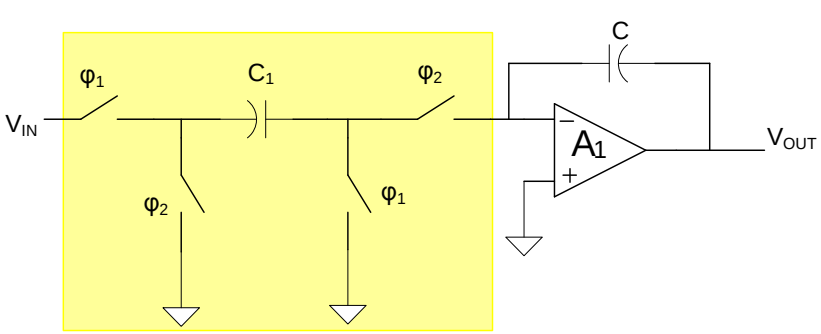


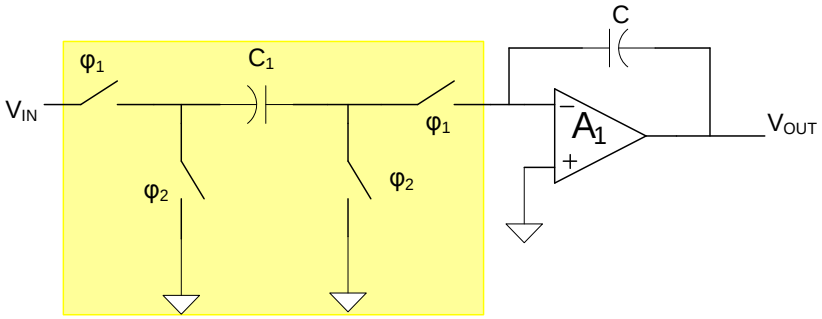


- Resistor blocks can be repeated and combined to provide summing inverting or noninverting inputs
- Resistor block can be placed in FB path to form lossy SC integrator

Switched-Capacitor Integrators

Stray-Insensitive SC Integrators



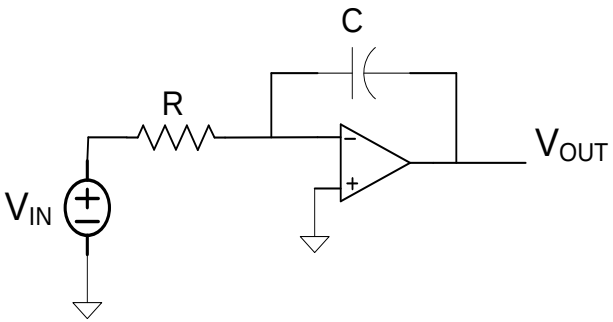


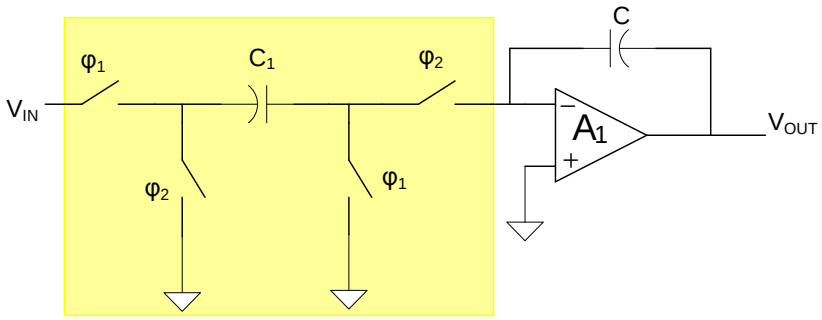
Many different SC filter structures have been proposed

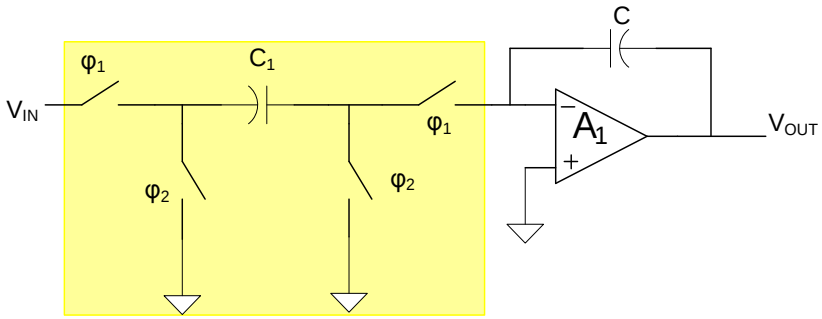
But most that are actually used are based upon these two circuits with the summing inputs or loss added as needed

Switched-Capacitor Integrators

Effects of Op Amp limitations

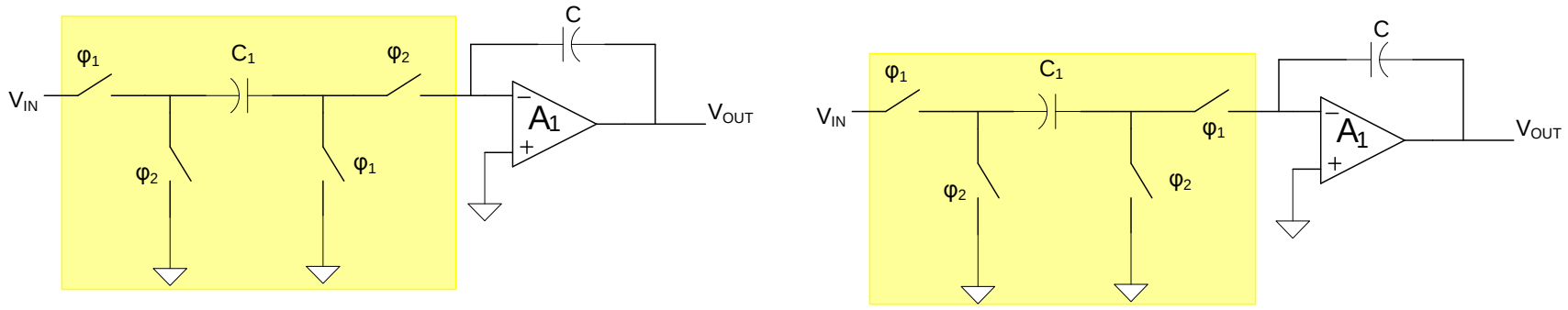






Can be shown that for a given band-edge, the GB requirements for the SC circuit are more relaxed than what is required for the corresponding Active RC integrator

Switched-Capacitor Integrators



Switched-capacitor filters are characterized in the z-domain

SC filters have continuous-amplitude inputs but outputs valid only at discrete times

Digital filters implemented with ADC/DAC approach have discrete amplitude and discrete time

What effects does the discrete-time property of a SC filter have on the filter performance?

End of Lecture 27