Integrator Design

Alaising in SC Circuits
Elimination of redundant switches
Switched Resistor Integrators
Consider the Switched-Capacitor Circuit

Assume $T_{CLK} \ll T_{SIG}$

$\Phi_1$ and $\Phi_2$ are complimentary nonoverlapping clocks

Review from Last Lecture
The SC integrator

Review from Last Lecture

\[ T(s) = -\frac{1}{RC_s}, \quad I_0 = \frac{1}{RC} \]

1. Accuracy of R and C difficult to accurately control (often 2 or 3 orders of magnitude to variable)

2. Area of R and C too large in audio frequency range (2 or 3 orders of magnitude too large)

3. Amplifier GB limits performance

Two of these properties were discovered independently by Gray, Broderson and Hosticka at Berkeley and by Copeland of Carlton

1. Accuracy of cap ratio and \( f_{CLK} \) very good

2. Area of C1 and C not too large

3. Amplifier GB limits performance less

Two of these properties were discovered independently by Gray, Broderson and Hosticka at Berkeley and by Copeland of Carlton


Seminal source of SC concept received few citations!

But cited as a key contribution when Brodersen and Gray elected to NAE
Nonideal Effects in Switched Capacitor Circuits

• Parasitic Capacitances
• Charge Injection
• Aliasing
• Redundant Switch Removal
• Matching
• Noise
Parasitic Capacitors in MOS Transistors

**n-channel MOSFET**

- Source
- Gate
- Drain
- Bulk
- $C_{GSOL}$
- $C_{GDOL}$
- $C_{GB}$ when off
- $C_{GC}$ when on
- $C_{BS}$

**p-channel MOSFET**

- Source
- Gate
- Drain
- Bulk
- $C_{GSOL}$
- $C_{GDOL}$
- $C_{GB}$ when off
- $C_{GC}$ when on
- $C_{BS}$

Review from Last Lecture
Observe this circuit has considerable parasitics (gate parasitics cause offset in this circuit and some signal-dependent distortion but will be neglected in this discussion)

Parasitic capacitors $C_{s1} + C_{d2} + C_{T1}$ difficult to accurately match

- Parasitic capacitors of THIS SC integrator limit performance
- Other SC integrators (discussed later) offer same benefits but are not affected by parasitic capacitors
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much smaller than $T_{SIG}$?

For $T_{CLK} < T_{SIG}$

Review from Last Lecture
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much-much smaller than $T_{SIG}$?

For $T_{CLK} \ll T_{SIG}$

Considerable change in $V(t)$ in clock period.
Switched-Capacitor Filter Issues

What if \( T_{CLK} \) is not much-much smaller than \( T_{SIG} \)?

For \( T_{CLK} < T_{SIG} \)

\[
V(nT) \quad \text{to} \quad V((n+1)T)
\]

\[
\phi_1 \quad \text{for} \quad nT_{CLK} \quad \text{to} \quad (n+1)T_{CLK}
\]

\[
\phi_2 \quad \text{for} \quad nT \quad \text{to} \quad (n+1)T
\]

\[
C
\]

\[
\Delta Q_c
\]

Assume input S/H is present

\[
V_0(nT+T) = V_0(nT) + \frac{\Delta Q_c}{C}
\]

but \(-Q_c\) is the charge on \( C_1 \) at the time \( \phi_1 \) opens

\[
-Q_c \approx C_1 V_{IN}(nT+T/2)
\]

\[
: \quad V_{OUT}(nT+T) = V_{OUT}(nT) - (C_1/C) V_{IN}(nT+T/2)
\]

Due to input S/H, \( V_{IN} \) constant over periods of length \( T \)
thus, assume \( V_{IN}(nT+T/2) \approx V_{IN}(nT) \)

So obtain

\[
V_{OUT}(nT+T) = V_{OUT}(nT) - (C_1/C) V_{IN}(nT)
\]

How does this analysis differ from what we did earlier?
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much much smaller than $T_{SIG}$?

Assume input S/H is present

$$V_{OUT}(nT+T) = V_{OUT}(nT) - \frac{C_1}{C} V_{IN}(nT)$$

for any $T_{CLK}$, characterized in time domain by difference equation

This can be characterized in the discrete-time frequency domain by transfer function obtained by taking $z$-transform of the difference equation

$$z V_{OUT}(z) = V_{OUT}(z) - \frac{C_1}{C} V_{IN}(z)$$

$$H(z) = -\frac{C_1}{C} z^{-1}$$

This is a standard integrator transfer function in the $z$-domain (but not unique)

Note pole at $z=1$
Switched-Capacitor Filter Issues

What if $T_{CLK}$ is not much smaller than $T_{SIG}$?

Claim: The transfer function of any Switched-Capacitor Filter is a rational fraction in $z$ with all coefficients in both the numerator and denominator determined totally by capacitor ratios.

$$H(z) = \frac{\sum_{i=0}^{m} a_i z^i}{\sum_{i=0}^{n} b_i z^i}$$
What is really required for building a filter that has high-performance features?

Consider an integrator:

Frequency domain:

Transfer function

\[ T(s) = \frac{1}{RCs} \]

Time domain:

Differential Equation

\[ V_{OUT}(t) = V_{OUT}(t_0) - \frac{1}{RC} \int_{t_0}^{t} V_{IN}(\tau) d\tau \]

- Accurate control of polynomial coefficients in transfer function or accurate control of coefficients in the differential equation
- Absence of over-ordering terms due to parasitics
What is really required for building a filter that has high-performance features?

Consider continuous-time and discrete-time integrators:

Frequency domain:

Transfer function

\[ T(s) = -\frac{1}{RCs} \]

Time domain:

Differential Equation

\[ V_{OUT}(t) = V_{OUT}(t_0) - \frac{1}{RC} \int_{t_0}^{t} V_{IN}(\tau) d\tau \]

Difference Equation

\[ V_{OUT}(nT+T) = V_{OUT}(nT) - (C_1/C)V_{IN}(nT) \]

• Accurate control of polynomial coefficients in transfer function or accurate control of coefficients in the differential/difference equation needed for good filter performance
• Absence of over-ordering terms due to parasitics
Switched-Capacitor Filter Issues

Transfer function of any SC filter of form:

\[ H(z) = \sum_{i=0}^{m} a_i z^i / \sum_{i=0}^{n} b_i z^i \]

Switched-capacitor circuits have potential for good accuracy and attractive area irrespective of how \( T_{\text{CLK}} \) relates to \( T_{\text{SIG}} \)

But good layout techniques and appropriate area need to be allocated to realize this potential!
Switched-Capacitor Integrators

\[ V_{\text{OUT}}(nT+T) = V_{\text{OUT}}(nT) - \left( \frac{C_1}{C} \right) V_{\text{IN}}(nT) \]

\[ H(z) = -\frac{C_1}{z-1} \]

Sensitive to parasitic capacitances
Switched-Capacitor Integrators

Summing Inputs

Sensitive to parasitic capacitances
Switched-Capacitor Integrators

Summing Inputs and Lossy

Sensitive to parasitic capacitances
Switched-Capacitor Integrators

Consider the following two SC circuits

Still have two capacitors but twice as many switches! 😞
But switches can be pretty small! 😊
Switched-Capacitor Integrators

Consider the first SC circuit

![Diagram of a switched-capacitor integrator circuit]

Assume input S/H

During phase $\Phi_1$, capacitor $V_{IN}$ is charged up to $V_{IN}(nT)$

During phase $\Phi_2$, this charge is transferred to $C$ and increasing $V_{OUT}$

$$V_{OUT}(nT+T) = V_{OUT}(nT) + \frac{C_1}{C} V_{IN}(nT)$$

$$H(z) = \frac{C_1}{C} \frac{1}{z-1}$$

Serves as a non-inverting integrator
Switched-Capacitor Integrators

Consider the second SC circuit

Prior to the start of phase $\Phi_1$, the capacitor $C_1$ was discharged by $\Phi_2$

During phase $\Phi_1$, capacitor $V_{IN}$ charges up to $V_{IN}(nT)$

While charge is flowing into $C_1$, it is also flowing into $C$ thus decreasing $V_{OUT}$

$$V_{OUT}(nT+T) = V_{OUT}(nT) - \frac{C_1}{C} V_{IN}(nT+T)$$

$$H(z) = \frac{C_1}{z-1}$$

Since $|z|_{z=e^{j\omega T}} = 1$

Serves as an inverting integrator
Nonideal Effects in Switched Capacitor Circuits

- Parasitic Capacitances
- Charge Injection
- Aliasing
- Redundant Switch Removal
- Matching
- Noise
Switched-Capacitor Integrators

Drain and Source Parasitic Capacitors shown in purple

Stray-Insensitive Properties

$C_{GD}$ does not affect gain of integrator

$C_{GCHANNEL}$ does not affect gain of integrator if switch not too fast
Switched-Capacitor Integrators

Stray-Insensitive Noninverting

Stray-Insensitive Inverting
Switched-Capacitor Integrators

Stray-Insensitive SC Integrators

- Resistor blocks can be repeated and combined to provide summing inverting or noninverting inputs
- Resistor block can be placed in FB path to form lossy SC integrator
Switched-Capacitor Integrators

Stray-Insensitive SC Integrators

Many different SC filter structures have been proposed

But most that are actually used are based upon these two circuits with the summing inputs or loss added as needed
Switched-Capacitor Integrators

Effects of Op Amp limitations

Can be shown that for a given band-edge, the GB requirements for the SC circuit are more relaxed than what is required for the corresponding Active RC integrator.
Switched-capacitor filters are characterized in the z-domain.

SC filters have continuous-amplitude inputs but outputs valid only at discrete times.

Digital filters implemented with ADC/DAC approach have discrete amplitude and discrete time.

What effects does the discrete-time property of a SC filter have on the filter performance?
End of Lecture 27