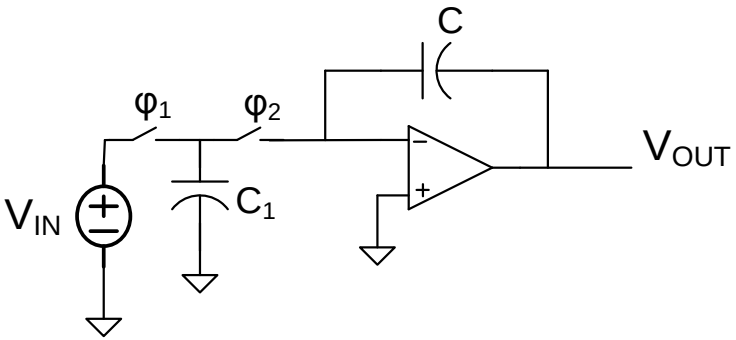
EE 508
Lecture 28

Integrator Design

Alaising in SC Circuits
Elimination of redundant switches
Switched Resistor Integrators

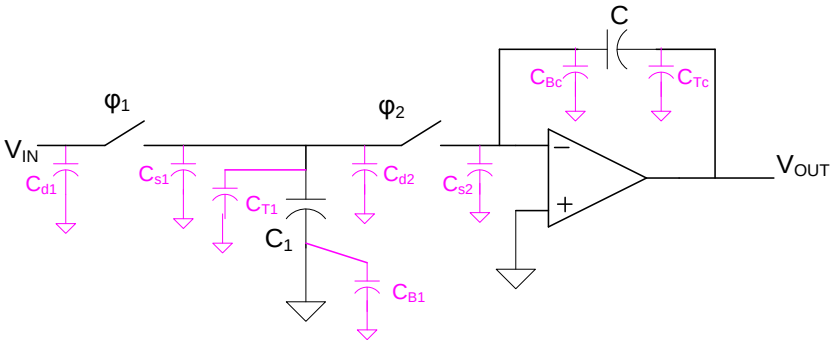
Review from last time

The SC integrator



$$I_{0eq}=\left[\frac{C_1}{C}\right]f_{CLK}$$

Observe this circuit has considerable parasitics



$C_{1EQ}=C_1+C_{s1}+C_{d2}+C_{T1}$

Parasitic capacitors $C_{s1}+C_{d2}+C_{T1}$ difficult to accurately match

- Parasitic capacitors of THIS SC integrator limit performance
- Other SC integrators (discussed later) offer same benefits but are not affected by parasitic capacitors

Review from last time

Switched-Capacitor Filter Issues

What if T_{CLK} is not much-much smaller than T_{SIG}?

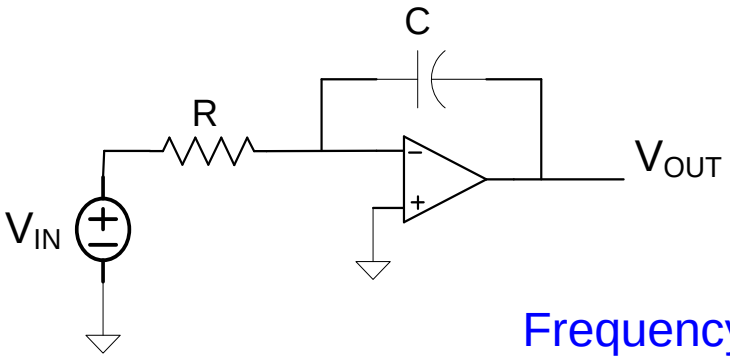
Claim: The transfer function of any Switched-Capacitor Filter is a rational fraction in z with all coefficients in both the numerator and denominator determined totally by capacitor ratios

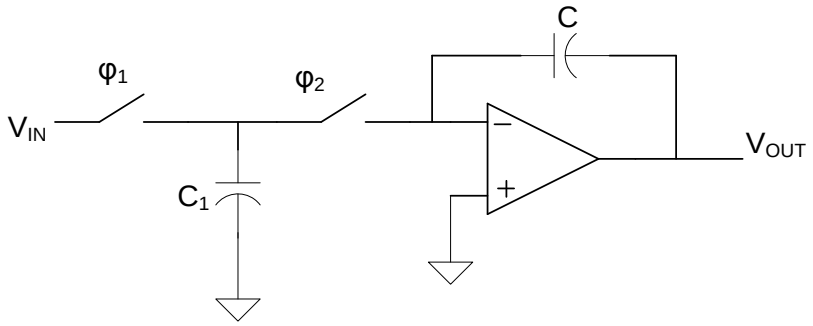
$$H(z) = \frac{\sum_{i=0}^{m} a_i z^i}{\sum_{i=0}^{n} b_i z^i}$$

Review from last time

What is really required for building a filter that has high-performance features?

Consider continuous-time and discrete-time integrators:





Frequency domain:

Transfer function

$$T(s) = -\frac{1}{RCs}$$

$$H(z) = -\frac{C_1/C}{z-1}$$

Time domain:

Differential Equation

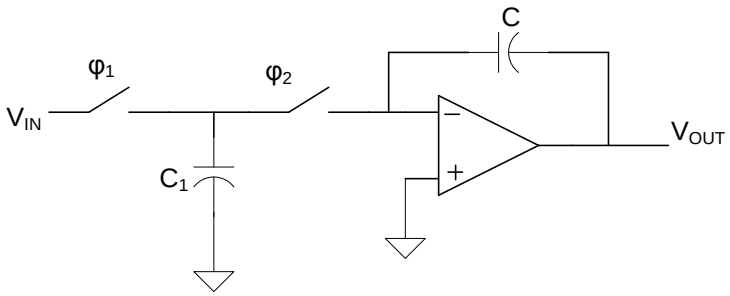
$$V_{OUT}(t) = V_{OUT}(t_0) - \frac{1}{RC}\int_{t_0}^{t} V_{IN}(\tau)\,d\tau$$

Difference Equation

$$V_{OUT}(nT+T) = V_{OUT}(nT) - (C_1/C)V_{IN}(nT)$$

- Accurate control of polynomial coefficients in transfer function or accurate control of coefficients in the differential/difference equation needed for good filter performance
- Absence of over-ordering terms due to parasitics

Switched-Capacitor Filter Issues



Transfer function of any SC filter of form:

$$H(z) = \frac{\sum_{i=0}^{m} a_i z^i}{\sum_{i=0}^{n} b_i z^i}$$

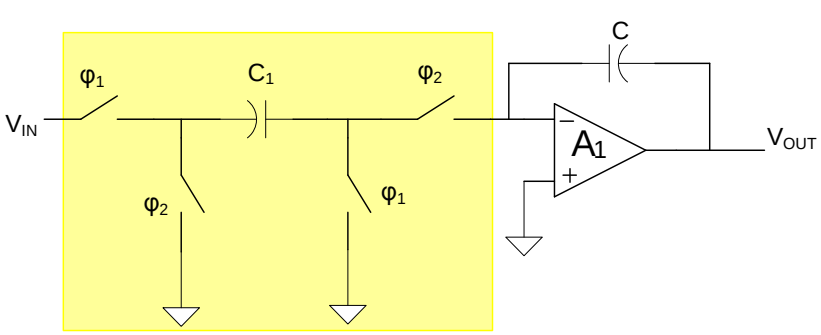
Switched-capacitor circuits have potential for good accuracy and attractive area irrespective of how T_{CLK} relates to T_{SIG}

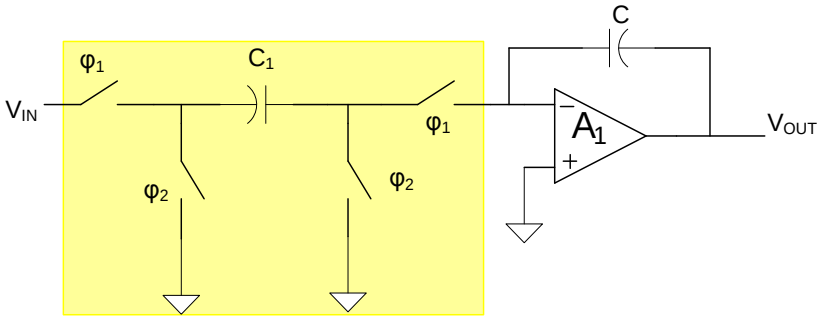
But good layout techniques and appropriate area need to be allocated to realize this potential !

Review from last time

Switched-Capacitor Integrators

Stray-Insensitive SC Integrators





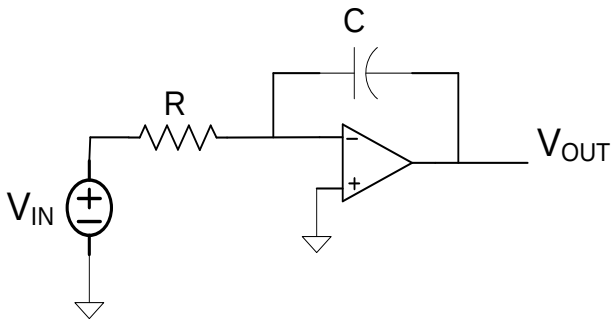
Many different SC filter structures have been proposed

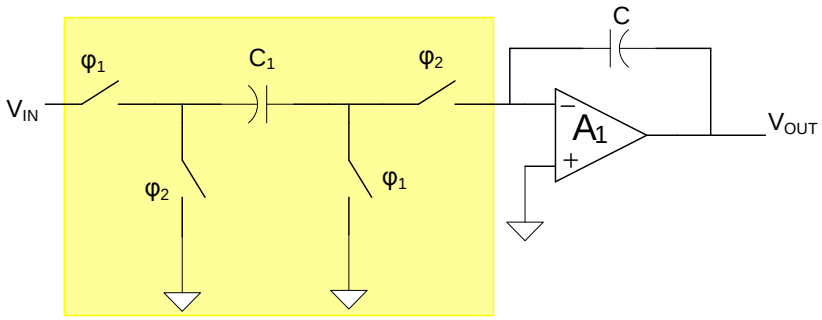
But most that are actually used are based upon these two circuits with the summing inputs or loss added as needed

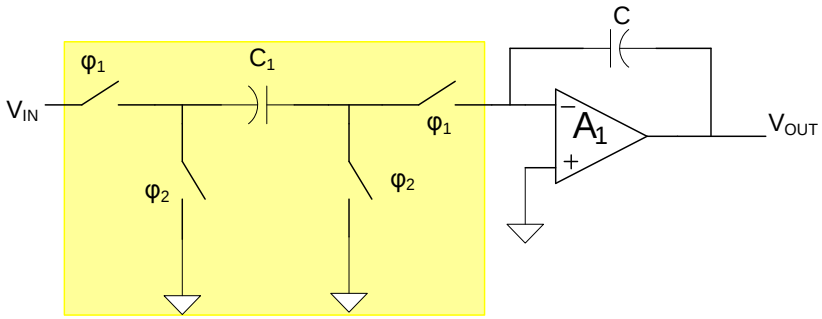
Review from last time

Switched-Capacitor Integrators

Effects of Op Amp limitations



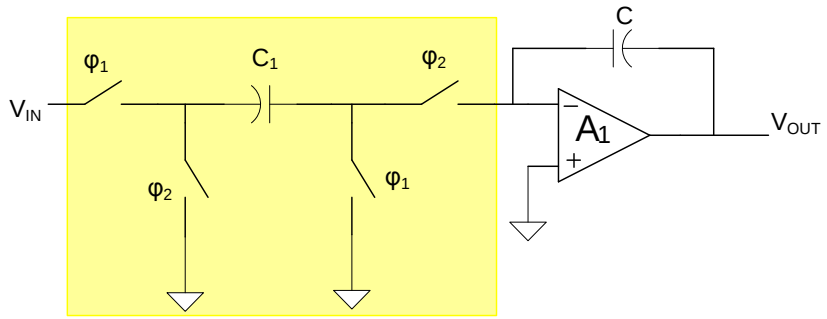


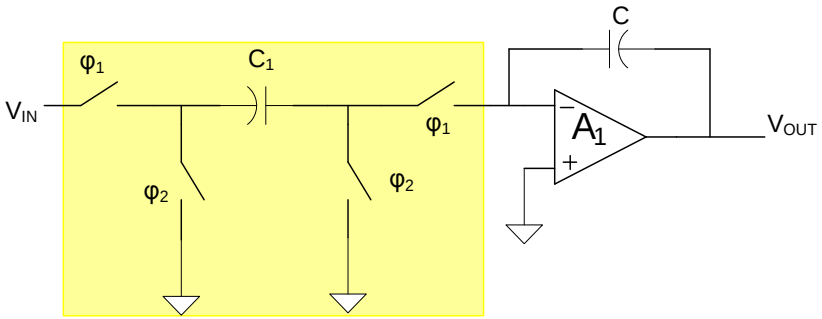


Can be shown that for a given band-edge, the GB requirements for the SC circuit are more relaxed than what is required for the corresponding Active RC integrator

Review from last time

Switched-Capacitor Integrators





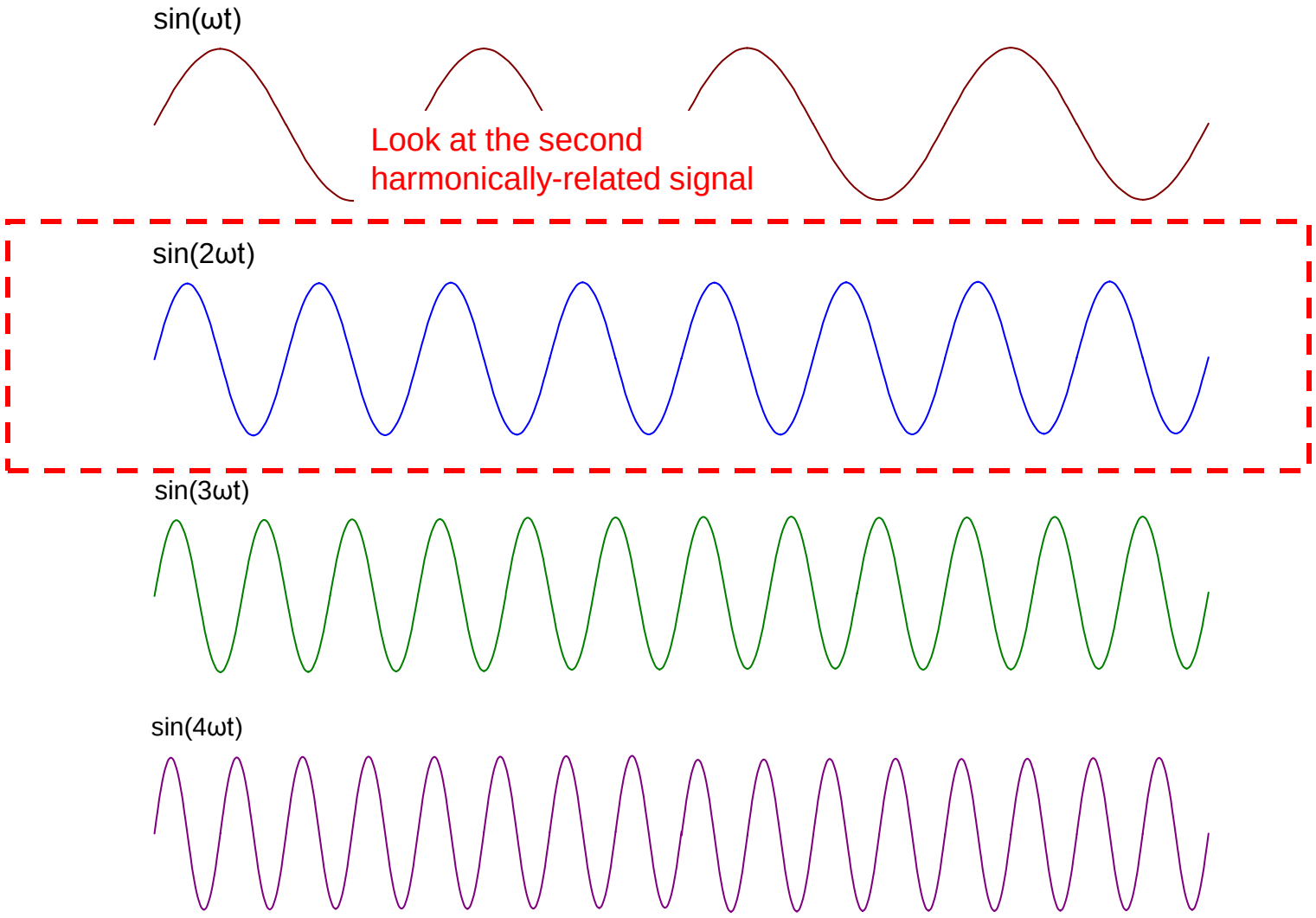
Switched-capacitor filters are characterized in the z-domain

SC filters have continuous-amplitude inputs but outputs valid only at discrete times

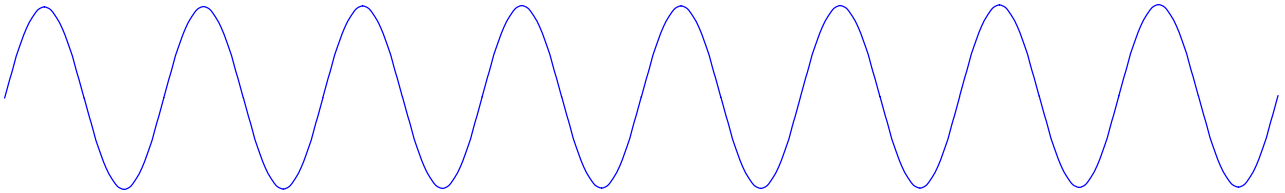
Digital filters implemented with ADC/DAC approach have discrete amplitude and discrete time

What effects does the discrete-time property of a SC filter have on the filter performance?

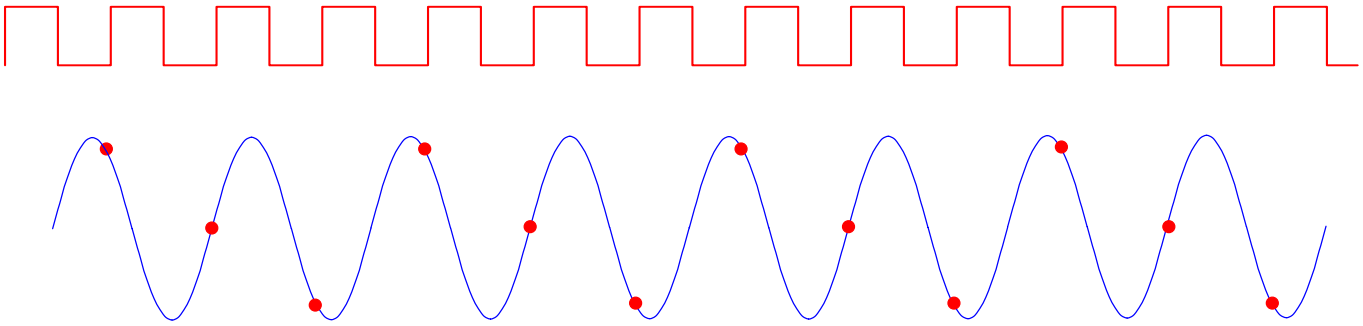
Consider a signal and harmonically-related signals



Consider a signal and harmonically-related signals

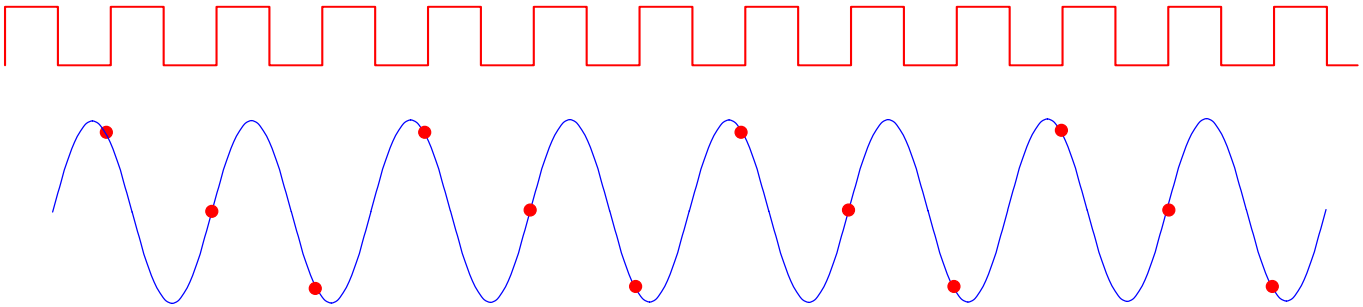


Sample with rising edges on the following clock (this could be Φ_1 for a SC filter)

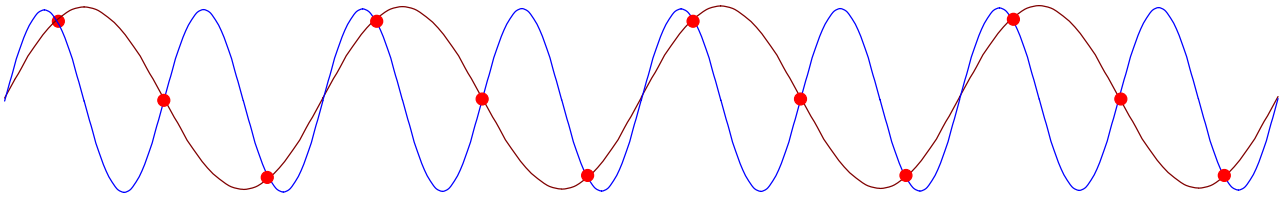


Consider a signal and harmonically-related signals

Sample with rising edges on the following clock (this could be Φ_1 for a SC filter)



Now overlay the fundamental frequency signal on this sampled waveform

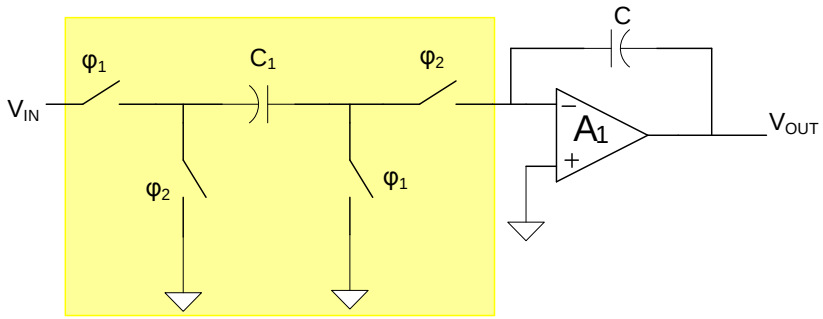


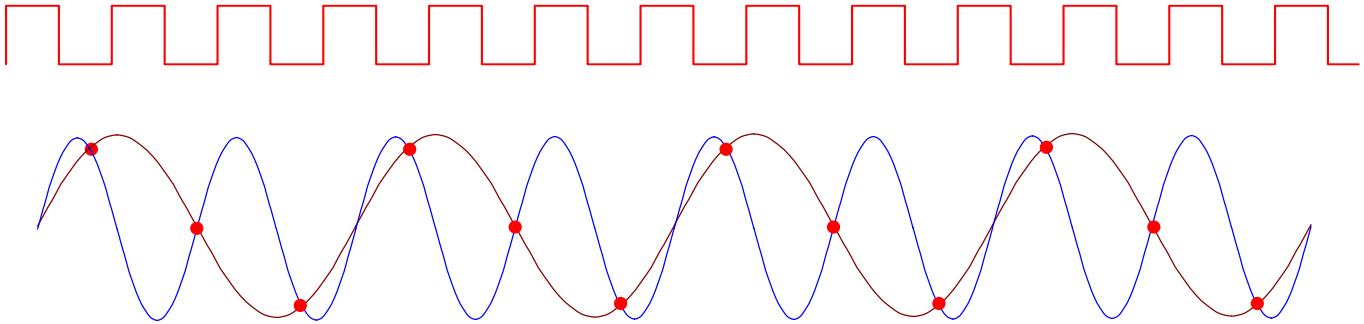
At these sample points, the samples of the two signals are indistinguishable

A similar observation will be observed if any of the other harmonically related signals are overlayed

A switched-capacitor filter can not distinguish between a fundamental and the harmonics if the ratio of the clock frequency to the signal frequency is too low

Consider a signal and harmonically-related signals

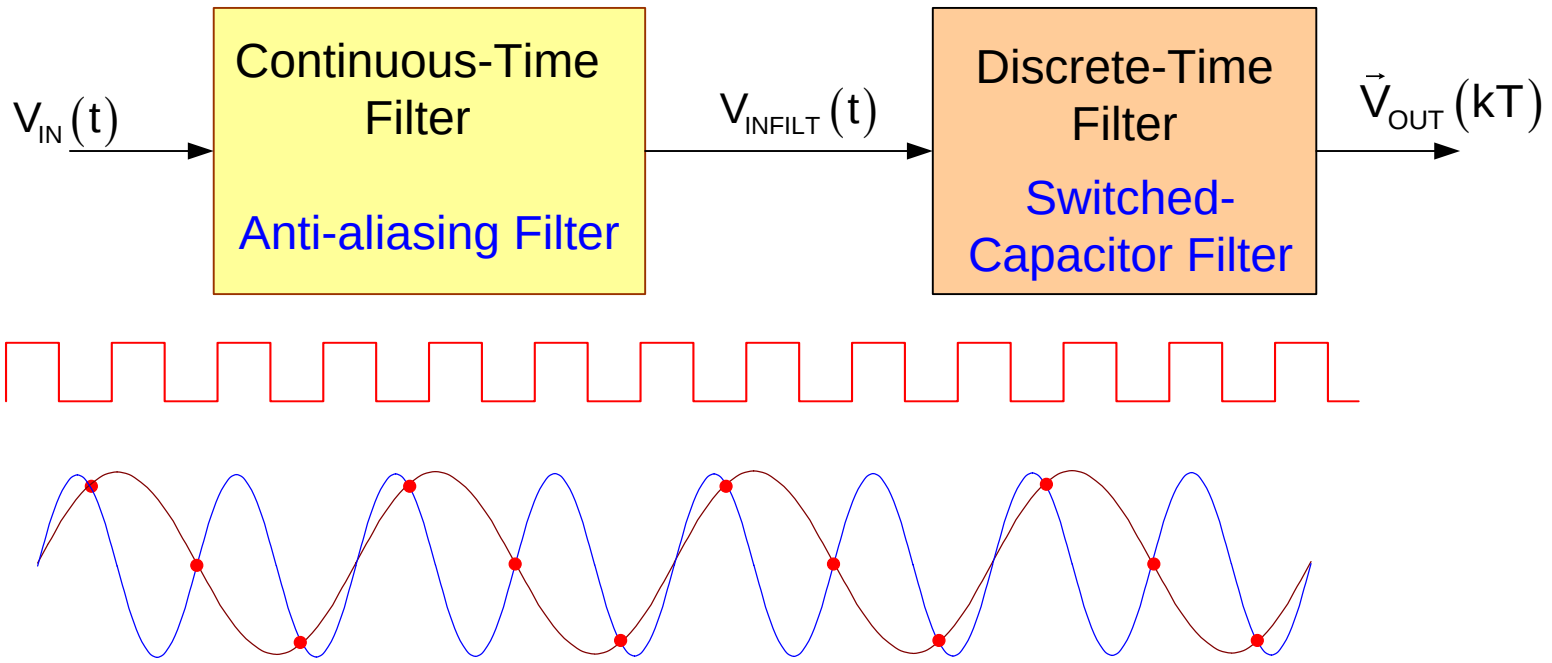




This aliases high frequency inputs (signals, noise, or even distortion) down to lower frequencies where it is indistinguishable from the lower frequency inputs

How can this problem be resolved?

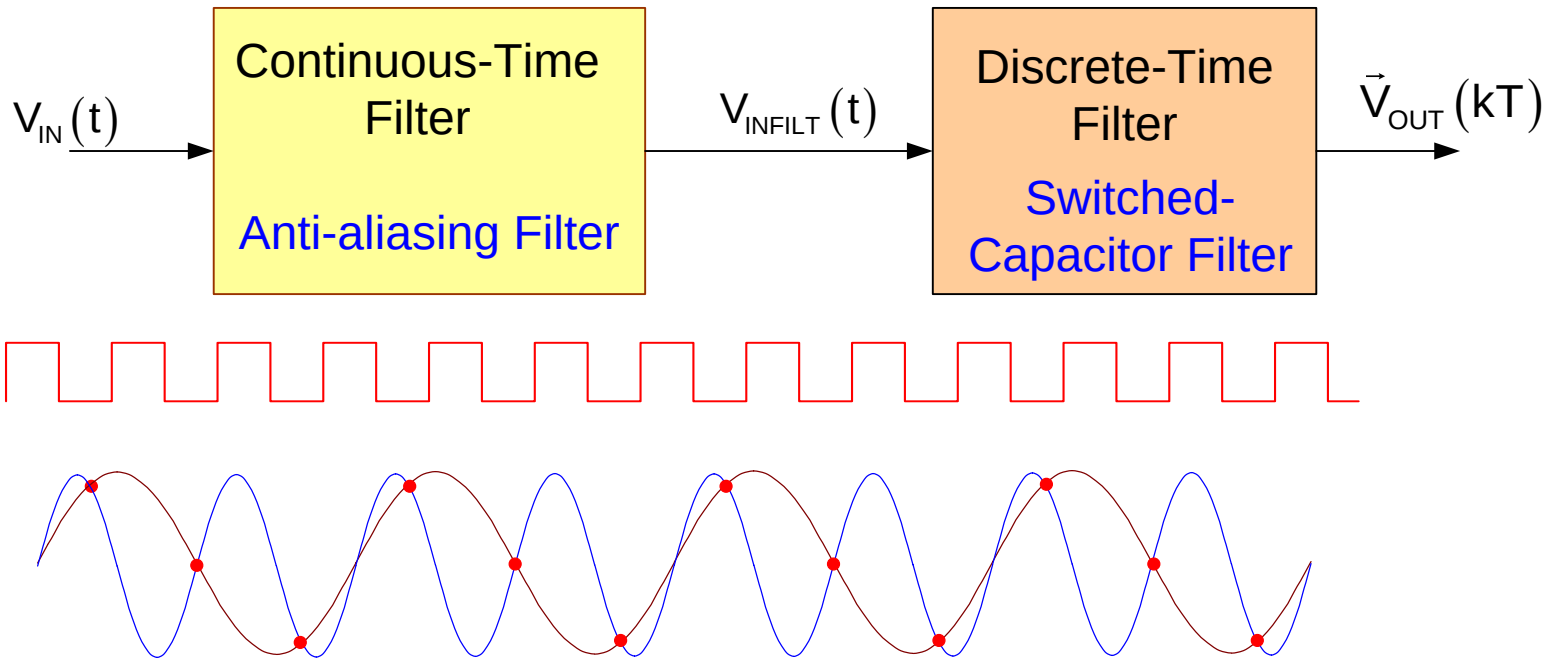
Anti-aliasing filter often required to limit frequency content at input to SC filters



Does this completely negate the benefits of the SC filter?

- Anti-aliasing filter not needed if input is already band limited
- Anti-aliasing filter often continuous-time and occasionally off-chip
- Linearity requirements of anti-aliasing filter in passband are high
- Good passband linearity can be practically attained
- Transition sharpness and accuracy typically very relaxed in the anti-aliasing filter
- Passive first-order anti-aliasing filter often adequate

Anti-aliasing filter often required to limit frequency content at input to SC filters



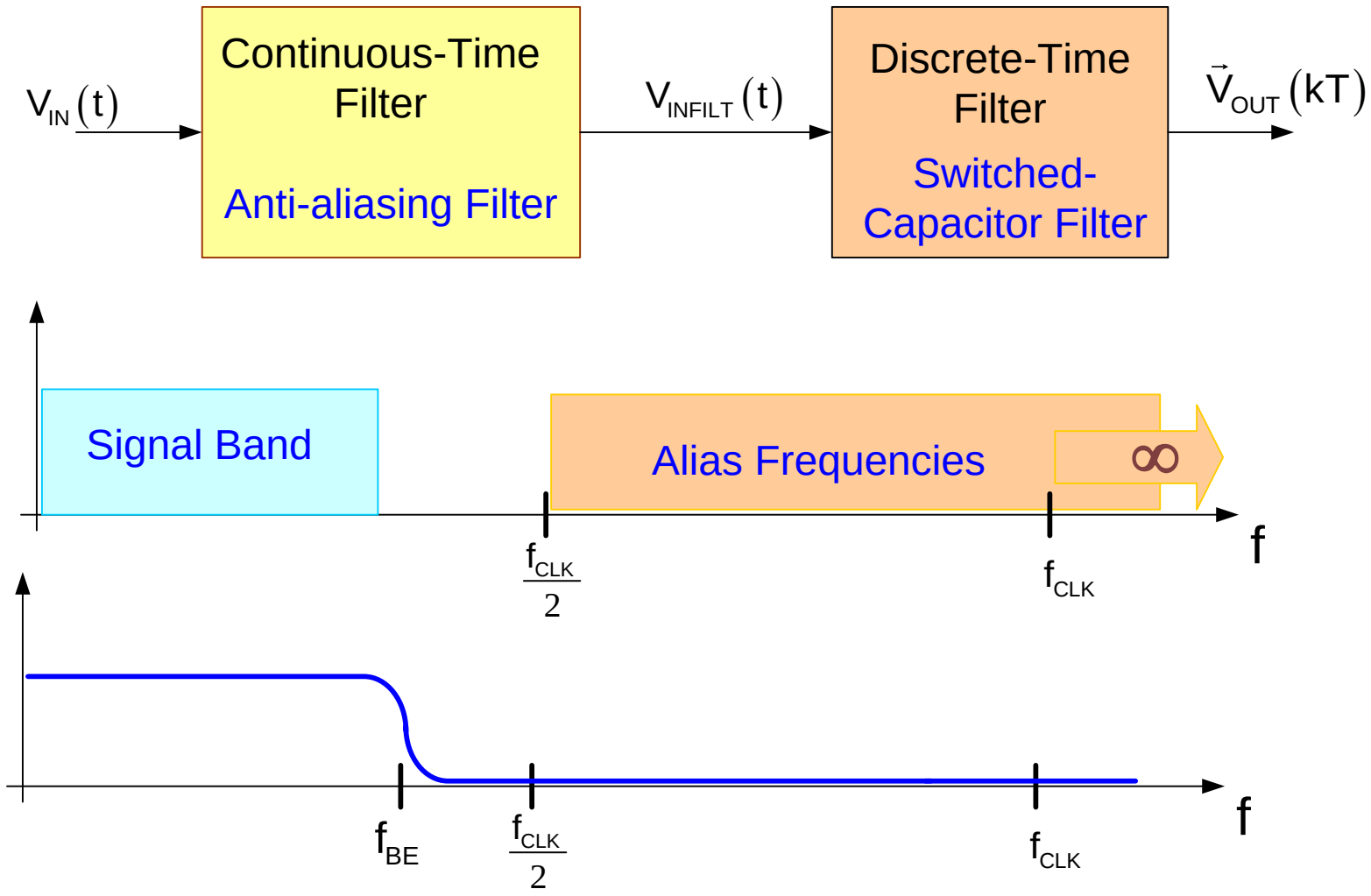
What are the band-edge requirements for the anti-aliasing filter?

Band edge of filter should limit all signals (and noise) at frequencies that are not wanted

What are SC clock requirements?

f_{CLK} must be at least twice the frequency of the signals that are to be passed by the SC filter

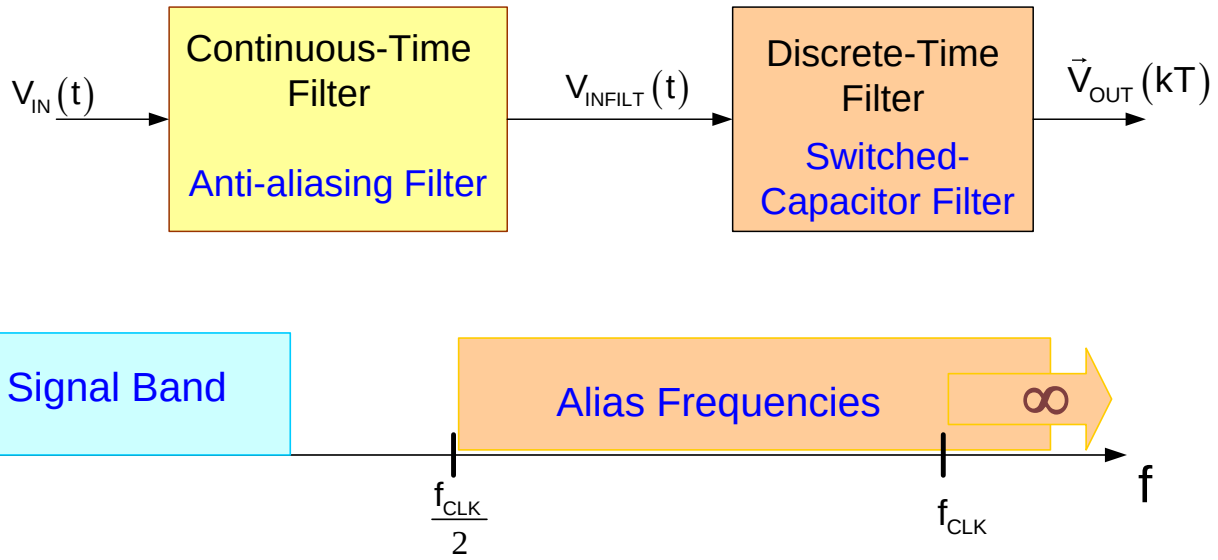
Anti-aliasing filter often required to limit frequency content at input to SC filters

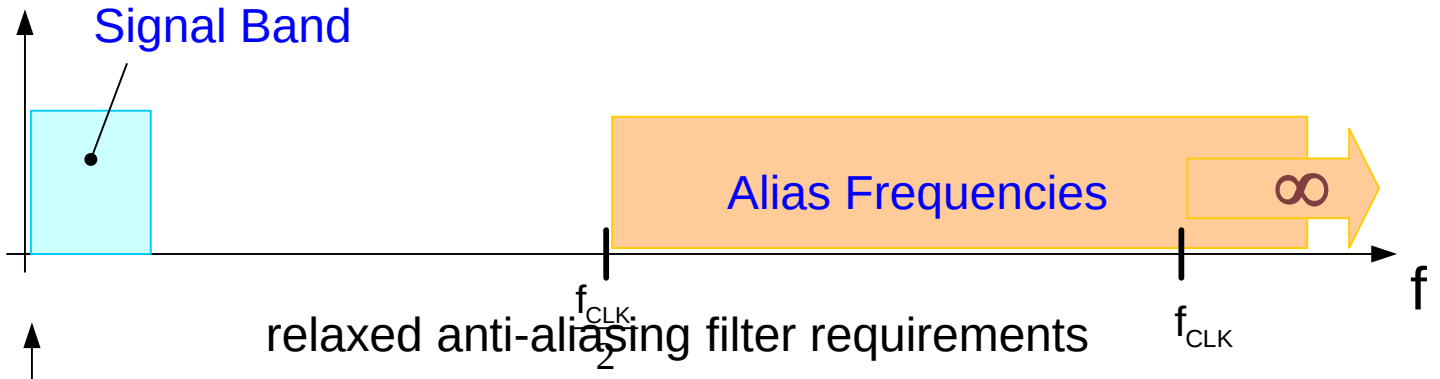


Antialiasing Filter

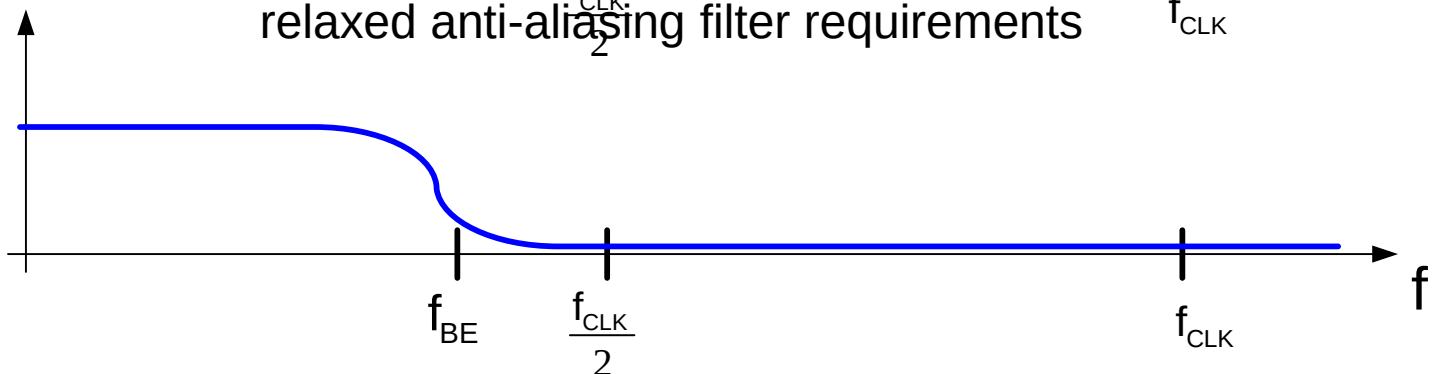
Must only attenuate at frequencies where energy is above an unacceptable level in the alias band

Anti-aliasing filter often required to limit frequency content at input to SC filters

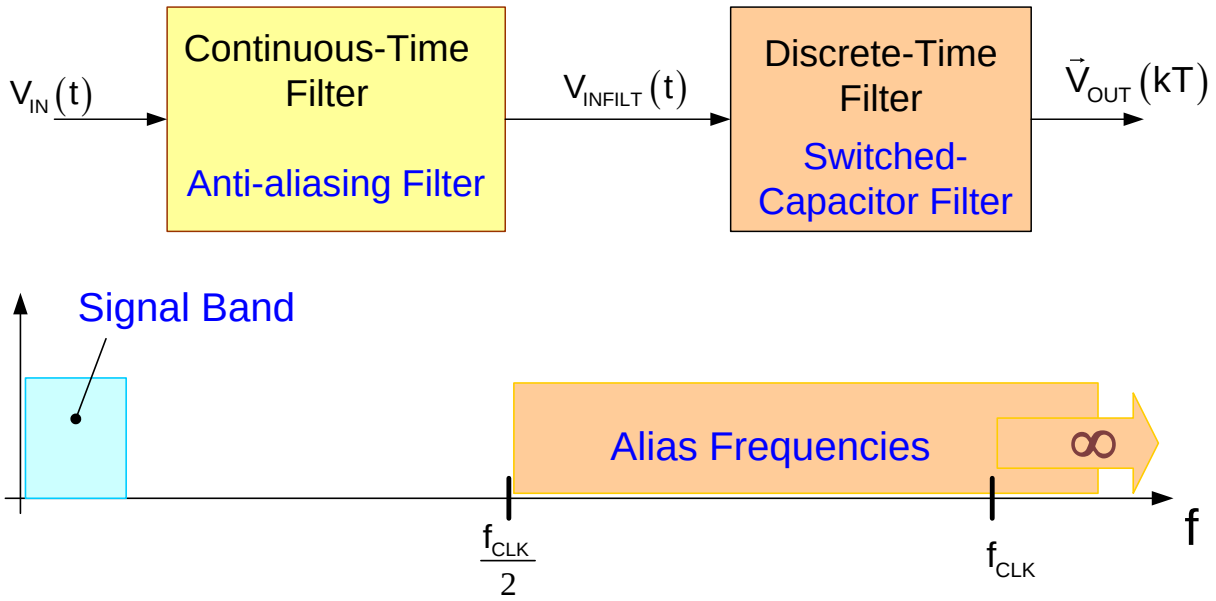




relaxed anti-aliasing filter requirements



Anti-aliasing filter often required to limit frequency content at input to SC filters



Why not just make the clock frequency >> signal band edge ?

Recall in the continuous-time RC-SC counterparts

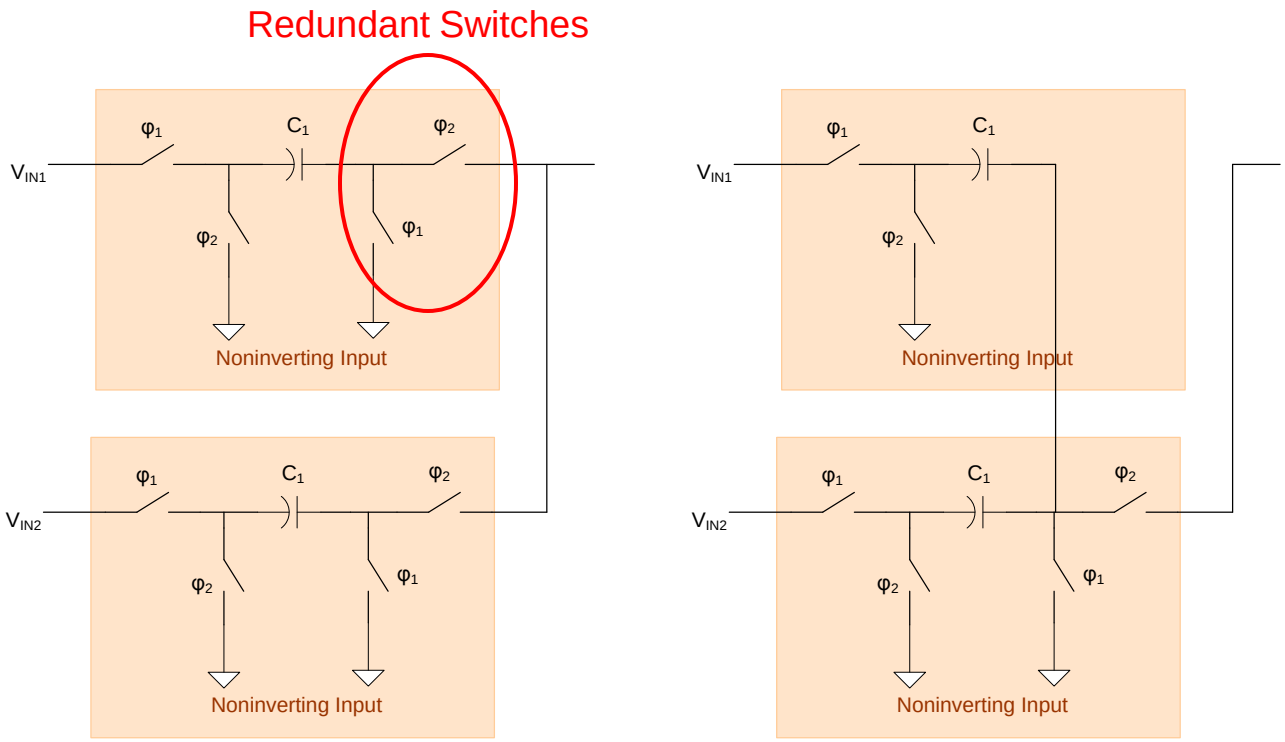
$$f_{POLES} \sim \frac{1}{RC} \simeq f_{CLK} \frac{C_1}{C}$$

Since f_{POLES} will be in the signal band (that is why we are building a filter) large f_{CLK} will require large capacitor ratios if $f_{CLK} >> f_{POLES}$

- Large capacitor ratios not attractive on silicon (area and matching issues)
- High f_{CLK} creates need for high GB in the op amps (area,power, and noise increase)

Often f_{CLK}/f_{POLES} in the 10:1 range proves useful (20:1 to 5:1 typical)

Elimination of Redundant Switches

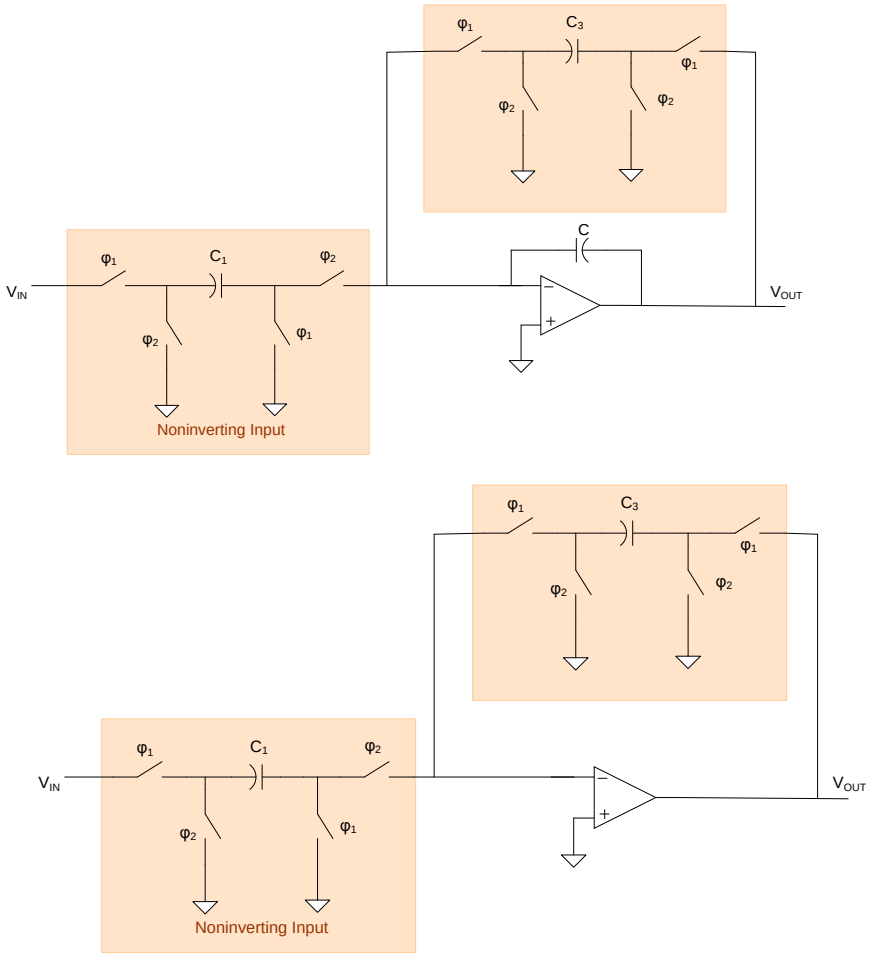


Switched-Capacitor Input with Redundant Switches

Switched-Capacitor Input with Redundant Switches Removed

Although developed from the concept of SC-resistor equivalence, SC circuits often have no Resistor-Capacitor equivalents

Elimination of the Integration Capacitor

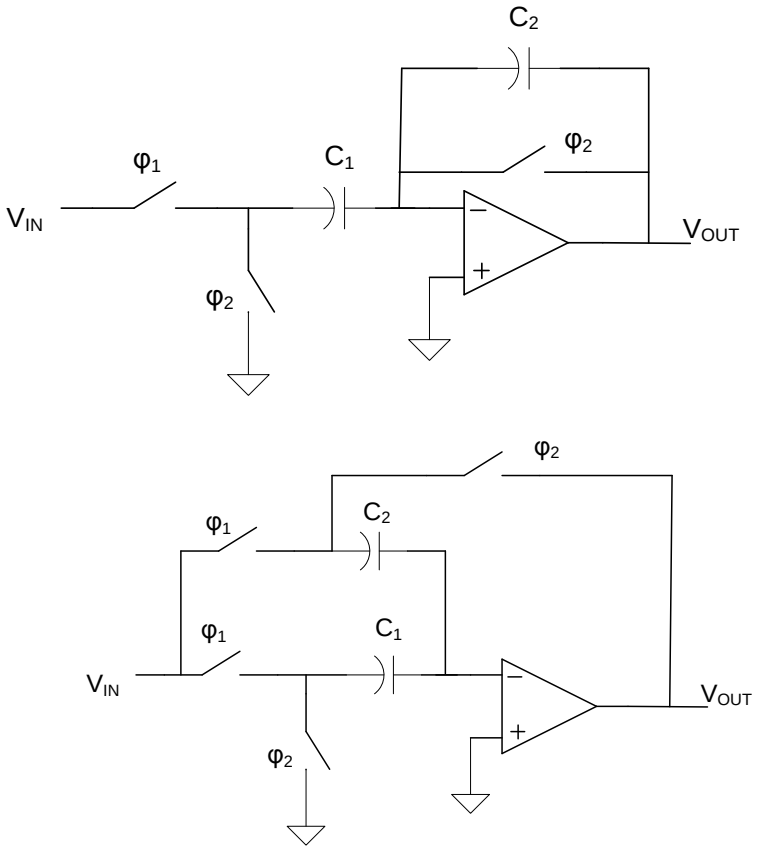


What happens if the integration capacitor is eliminated?

Serves as a SC amplifier with gain of $A_V=C_1/C_2$

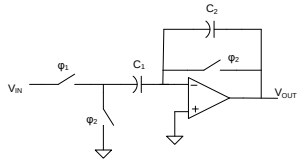
SC amplifiers and SC summing amplifiers are widely used in filter and non-filter applications

Switched Capacitor Amplifiers

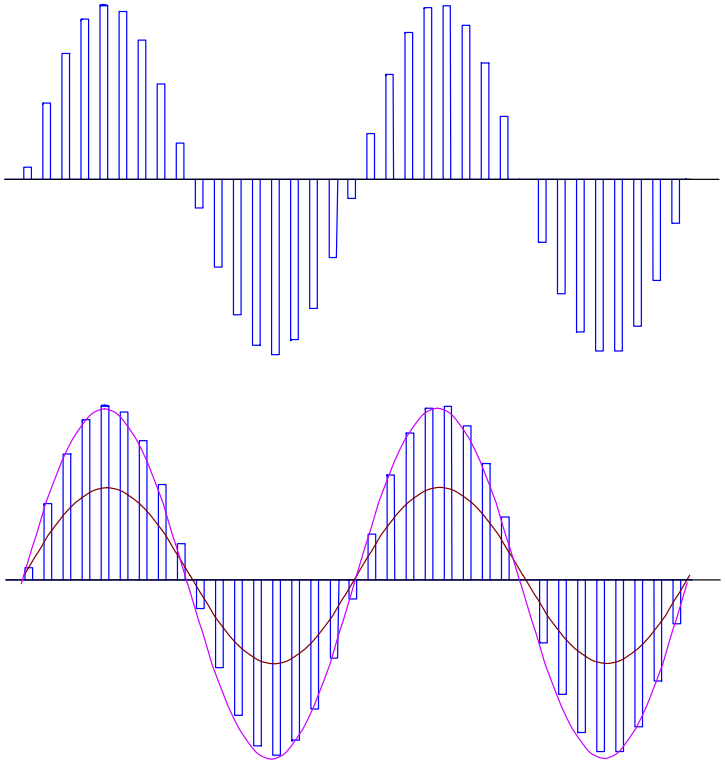


- Summing, Differencing, Inverting, and Noninverting SC Amplifiers Widely Used
- Significant reduction in switches from what we started with by eliminating C in SC integrator
- Must be stray insensitive in most applications
- Outputs valid only during one phase

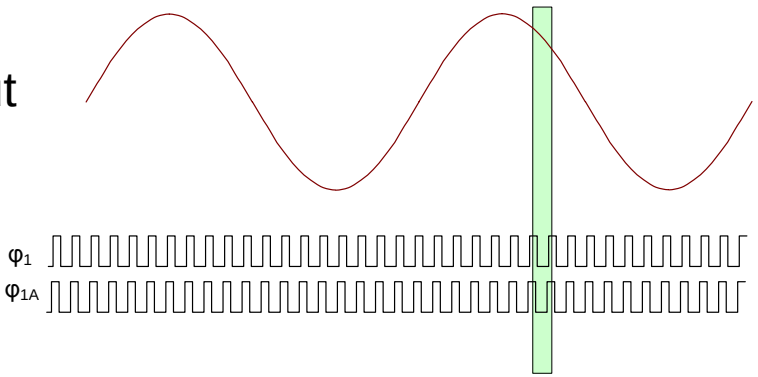
Switched Capacitor Amplifiers



Output



Input



Voltage Mode Integrators

- Active RC (Feedback-based)
- MOSFET-C (Feedback-based)
- OTA-C
- TA-C

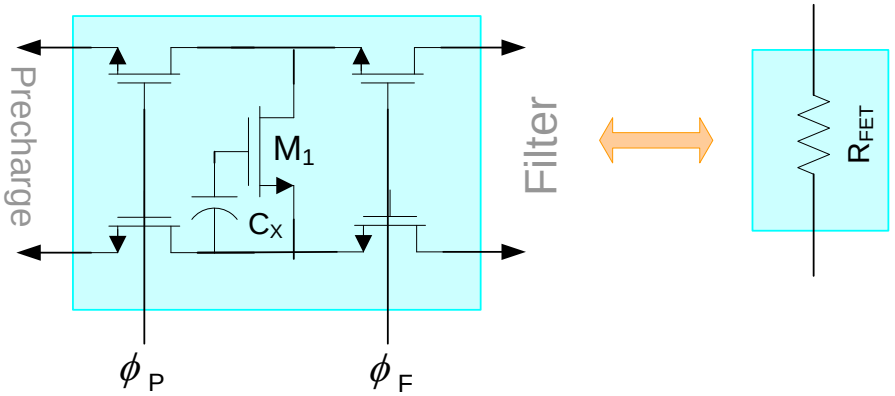
Sometimes termed “current mode”

- Switched Capacitor
- Switched Resistor

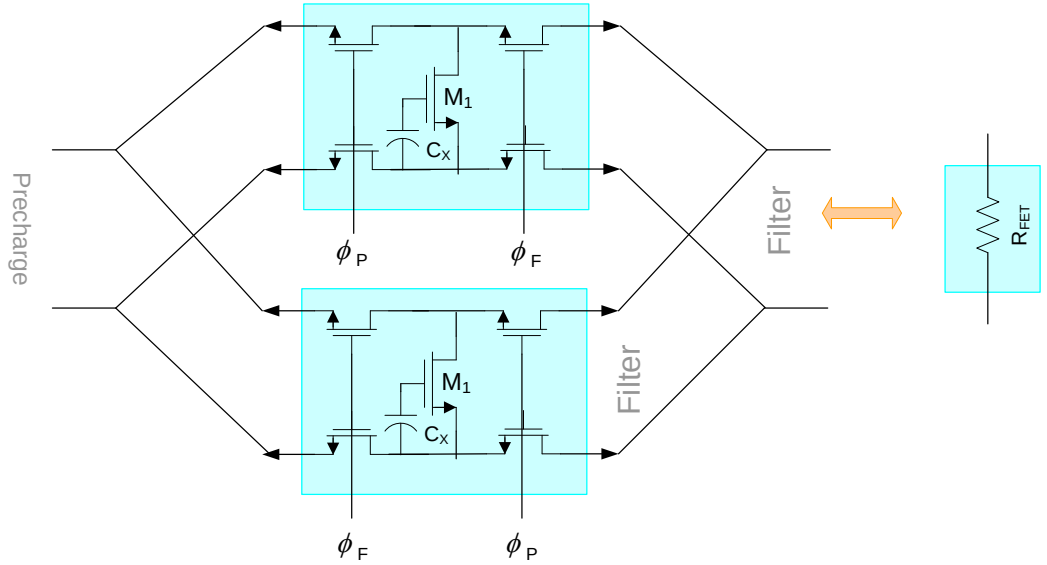
Will discuss later

- Other Structures

Switched-Resistor Voltage Mode Integrators



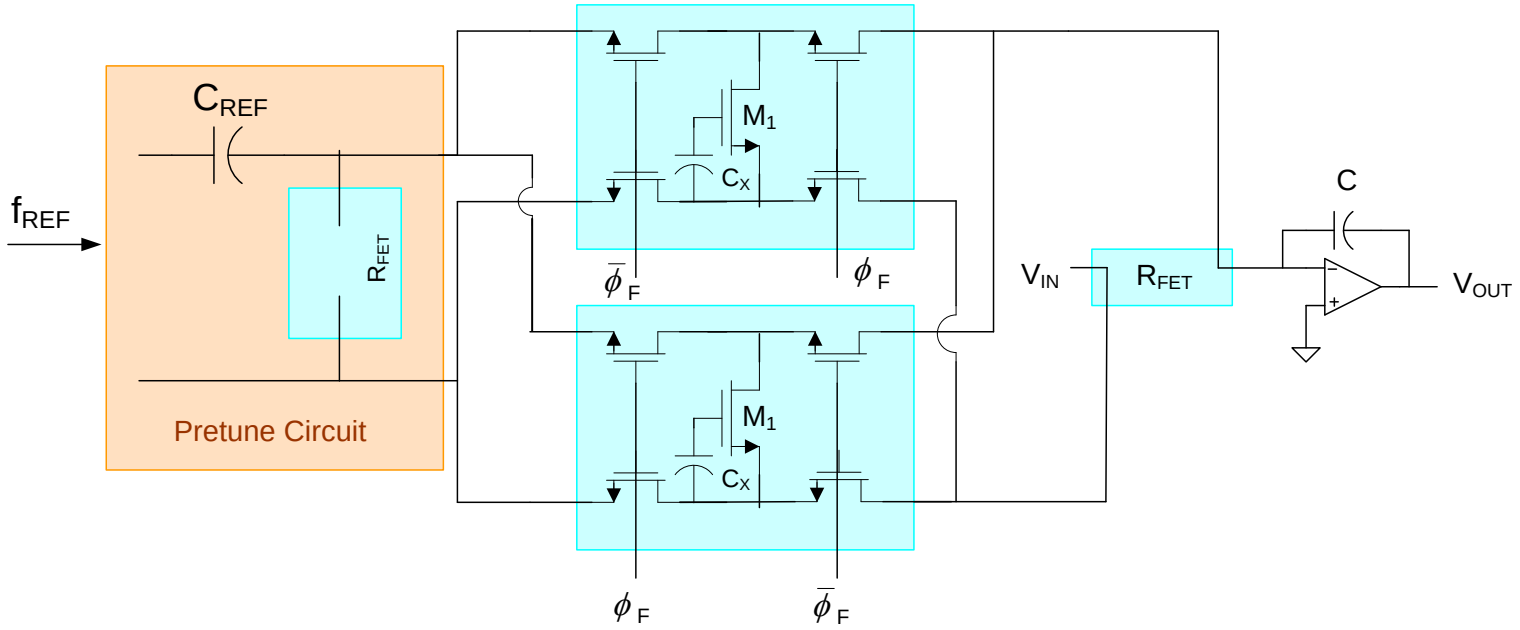
Observe that if a triode-region MOS device is switched between a precharge circuit and a filter circuit (or integrator) and V_{GS} is held constant, It will behave as a resistor while in the filter circuit



$$R_{FET} \simeq \frac{L}{\mu C_{OX} W (V_{GS} - V_T)}$$

Observe that if two such circuits are switched between a precharge circuit and a filter circuit (or integrator) and V_{GS} is held constant, It will behave as a resistor in the filter circuit at all times

Switched-Resistor Voltage Mode Integrators



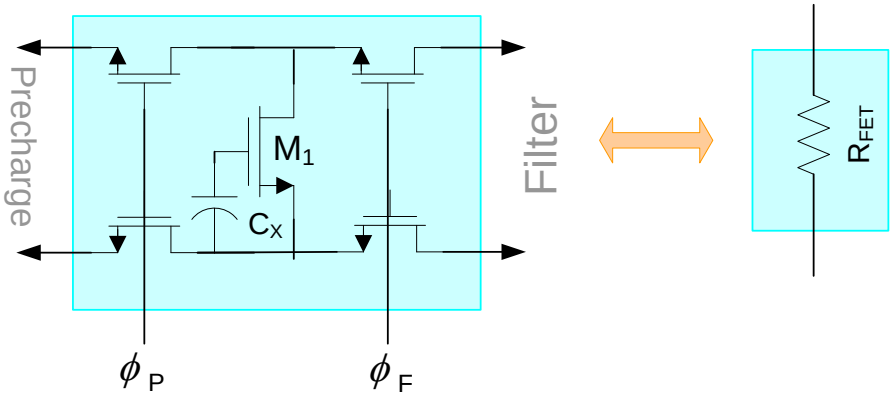
Switched-resistor integrator

- Clock frequency need only be fast enough to prevent droop on C_X
- Minor overlap or non-overlap of clock plays minimal role in integrator performance
- Switched-resistors can be used for integrator resistor or to replace all resistors in any filter
- Pretune circuit can accurately establish $R_{FET}C_{REF}$ product proportional to f_{REF}
- $R_{FET}C$ product is given by accurately controlled

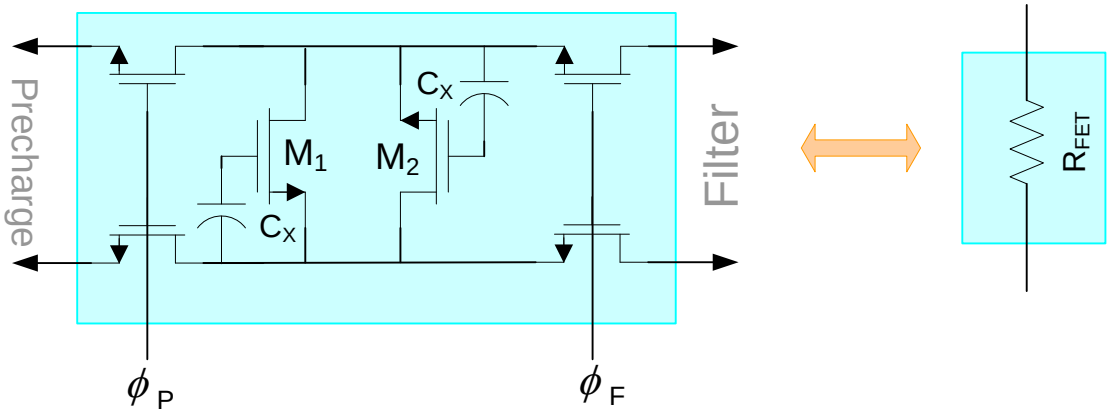
$$R_{FET}C = R_{FET}C\frac{C_{REF}}{C_{REF}} = [R_{FET}C_{REF}]\bullet\left[\frac{C}{C_{REF}}\right]$$

and is thus

Switched-Resistor Voltage Mode Integrators

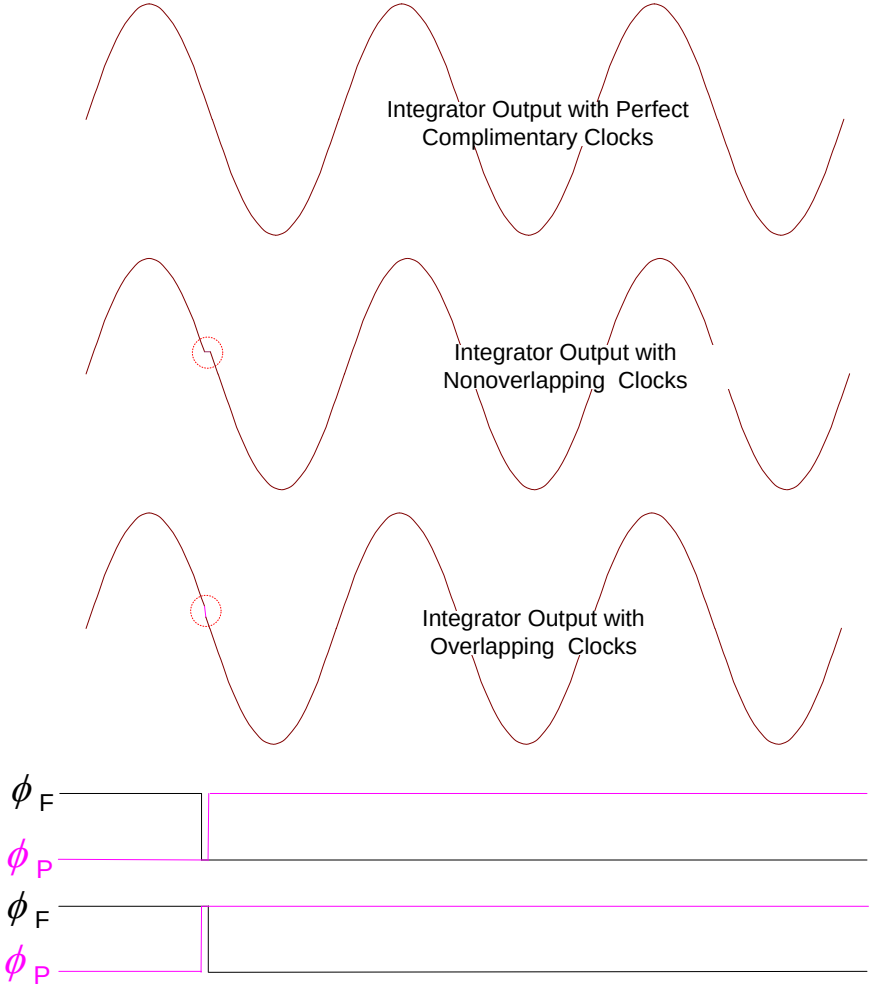


There are some modest nonlinearities in this MOSFET when operating in the triode region



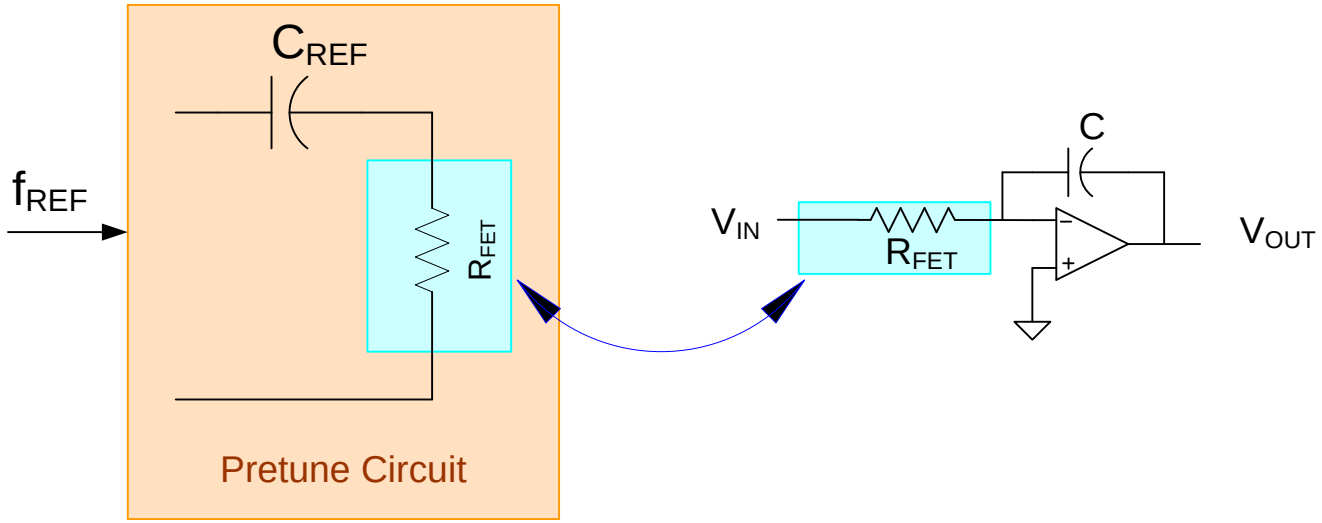
- Significant improvement in linearity by cross-coupling a pair of triode region resistors
- Perfectly cancels nonlinearities if square law model is valid for M_1 and M_2
- Only modest additional complexity in the Precharge circuit

Switched-Resistor Voltage Mode Integrators



- Aberrations are very small, occur very infrequently, and are further filtered
- Play almost no role on performance of integrator or filter

Switched-Resistor Voltage Mode Integrators



Switched-resistor integrator

- Accurate CR_{FET} products is possible
- Area reduced compared to Active RC structure because R_{FET} small
- Single pretune circuit can be used to “calibrate” large number of resistors
- Clock frequency not fast and not critical (but accuracy of f_{REF} is important)
- Since resistors are memoryless elements, no transients associated with switching
- Since filter is a feedback structure, speed limited by BW of op amp