EE 508
Lecture 39_2

• What filter architectures are really being used today?

• Basic Filter Components
  • All Pass Networks
  • Arbitrary Transfer Function Synthesis
  • Impedance Transformation Circuits
  • Equalizers
A 30-MHz–2.4-GHz CMOS Receiver With Integrated RF Filter and Dynamic-Range-Scalable Energy Detector for Cognitive Radio Systems

Masaki Kitsunezuka, Hiroshi Kodama, Naoki Oshima, Kazuaki Kunihiro, Tadashi Maeda, Member, IEEE, and Muneo Fukaishi, Member, IEEE
To enable a wide tuning range (30 to 800 MHz) to be covered, 4-bit binary-weighted load-capacitor arrays are used to vary the filter characteristics. In addition, transconductance gain $g_m$ is controlled by tuning the gate bias voltage of M1. Fig. 5
The transfer functions of the BPF and LPF are expressed as

\[
H_{\text{BPF}}(s) = \frac{V_{\text{BPF}}}{V_{\text{in}}} = \frac{s \frac{g_{m1}}{C_1}}{s^2 + s \frac{g_{m1}}{C_1} + \frac{g_{m2}g_{m3}}{C_1C_2}}
\] (1)

and

\[
H_{\text{LPF}}(s) = \frac{V_{\text{LPF}}}{V_{\text{in}}} = \frac{\frac{g_{m1}g_{m3}}{C_1C_2}}{s^2 + s \frac{g_{m1}}{C_1} + \frac{g_{m2}g_{m3}}{C_1C_2}},
\] (2)

respectively, where \(g_{m_i}\) is the transconductance gain of transistor \(M_i\). The cut-off (or center) frequency and quality factor are respectively written as

\[
\omega_c = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}}
\] (3)

and

\[
Q = \frac{\sqrt{g_{m2}g_{m3}}}{g_{m1}} \sqrt{\frac{C_1}{C_2}}.
\] (4)
Fig. 5. Simulated frequency characteristics of RF filter.
A 4\textsuperscript{th}-Order 84dB-DR CMOS-90nm Low-Pass Filter for WLAN Receivers

M. De Matteis\textsuperscript{1}, A. Pezzotta\textsuperscript{2}, A. Baschirotto\textsuperscript{2}

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Fig. 1 - WLAN 4th Order Filter Block/Circuital Scheme
Fig. 5 – 4th Order WLAN Filter – Top-View Schematic
The uncertainty on the passive components nominal value due to the fabrication process and temperature variations can reach the 45%, affecting the filter frequency response. Any process variation and temperature dependencies can be compensated by tuning either the R’s or the C’s values. The in the Fig. 6. The array value is, then, set by the external using a proper digital code.

![Capacitor Array](image)

**Fig. 6 – Capacitor Array**
Fig. 7 – Opamp Schematic
Fig. 8 – Filter Frequency Response

(-3.01 dB, 10.6 MHz) (-3.01 dB, 11.7 MHz)
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G[\text{dB}]$</td>
<td>0</td>
</tr>
<tr>
<td>$f_{-3\text{dB}}[\text{MHz}]$</td>
<td>11</td>
</tr>
<tr>
<td>$avdd[\text{V}]$</td>
<td>1.2</td>
</tr>
<tr>
<td><strong>CMOS Technology</strong></td>
<td>90nm</td>
</tr>
<tr>
<td><strong>Power Consumption[\text{mW}]</strong></td>
<td>14</td>
</tr>
<tr>
<td><strong>Output Integrated Noise[\mu V_{rms}] - (100kHz ÷ 20MHz)</strong></td>
<td>48</td>
</tr>
<tr>
<td><strong>IRN Spectral Density@2MHz [nV/\sqrt{Hz}]</strong></td>
<td>5</td>
</tr>
<tr>
<td><strong>THD[\text{dBc}] – v_{out}=1.05V_{zero-peak}@4\text{MHz}</strong></td>
<td>40</td>
</tr>
<tr>
<td><strong>DR@THD=40dBc - [\text{dB}]</strong></td>
<td>84</td>
</tr>
<tr>
<td><strong>IIP3 [\text{dBm}] – v_{in}=v_{in1}+v_{in2} - v_{in1}@4\text{MHz}, v_{in2}@5\text{MHz}</strong></td>
<td>10</td>
</tr>
</tbody>
</table>

Tab. IV – Filter Performance Resume
A 23.4 mW 68 dB Dynamic Range Low Band CMOS Hybrid Tracking Filter for ATSC Digital TV Tuner Adopting RC and Gm-C Topology

Kuduck Kwon, Member, IEEE, and Kwyro Lee, Senior Member, IEEE

Fig. 3. Proposed third-order Chebyshev hybrid tracking low-pass filter.
A 23.4 mW 68 dB Dynamic Range Low Band CMOS Hybrid Tracking Filter for ATSC Digital TV Tuner Adopting RC and Gm-C Topology

Kuduck Kwon, Member, IEEE, and Kwyro Lee, Senior Member, IEEE

Fig. 1. Block diagram of RF front-end for ATSC terrestrial digital TV tuner.
Fig. 2. Third-order elliptic transconductor-C low-pass filter based on ladder filter structure.
Fig. 3. Proposed third-order Chebyshev hybrid tracking low-pass filter.

<table>
<thead>
<tr>
<th>COMPONENTS VALUES AND TRANSISTOR SIZES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Components</td>
</tr>
<tr>
<td>Transistor</td>
</tr>
<tr>
<td>Sizes [W/L]</td>
</tr>
</tbody>
</table>

*C₁, C₂, and C₃ in Table II are values for 100MHz -1dB cut-off frequency.
ST transistors operating in weak inversion provide linearization of basic transconductance stage. Transistor biasing not shown but described in [11].
<table>
<thead>
<tr>
<th></th>
<th>[1]</th>
<th>[18]</th>
<th>[19]*</th>
<th>[25]</th>
<th>[26]</th>
<th>[27]</th>
<th>[28]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18μm CMOS</td>
<td>0.13μm CMOS</td>
<td>0.18μm CMOS</td>
<td>0.25μm CMOS</td>
<td>0.25μm CMOS</td>
<td>0.35μm CMOS</td>
<td>0.13μm CMOS</td>
<td>0.18μm CMOS</td>
</tr>
<tr>
<td>Cut-off freq.(f) [MHz]</td>
<td>50-300</td>
<td>50-300</td>
<td>50-300</td>
<td>80-200</td>
<td>30-120</td>
<td>200</td>
<td>200</td>
<td>50-200</td>
</tr>
<tr>
<td>OIP3 [dBm]</td>
<td>14</td>
<td>11</td>
<td>16.9</td>
<td>18.8</td>
<td>10.1</td>
<td>17</td>
<td>14</td>
<td>17.3</td>
</tr>
<tr>
<td>NF [dB]</td>
<td>17</td>
<td>20</td>
<td>14</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>32</td>
<td>15</td>
</tr>
<tr>
<td>Filter order (N)</td>
<td>4</td>
<td>4</td>
<td>3</td>
<td>7</td>
<td>8</td>
<td>7</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Single (S) or Differential (D)</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>S</td>
<td></td>
</tr>
<tr>
<td>Pdc [mW]</td>
<td>72</td>
<td>7.6</td>
<td>72</td>
<td>210</td>
<td>120</td>
<td>60</td>
<td>20.8</td>
<td>23.4</td>
</tr>
<tr>
<td>FOM</td>
<td>51</td>
<td>120</td>
<td>152</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.3</td>
<td>193</td>
</tr>
<tr>
<td>(FOM2**)</td>
<td>(2511)</td>
<td>(11926)</td>
<td>(3673)</td>
<td>(1264)</td>
<td>(327)</td>
<td>(1170)</td>
<td>(483)</td>
<td>(5901)</td>
</tr>
<tr>
<td>(FOM3***)</td>
<td>(51)</td>
<td>(120)</td>
<td>(152)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>(0.3)</td>
<td>(96.5)</td>
</tr>
</tbody>
</table>

*[19] is our previous work of the tracking filter utilized for both ATSC terrestrial and Cable digital TV standards

**FOM2 is the equation excluding the (F-1) term in the FOM of equation (14) because [25]-[27] do not indicate the noise performance
Fig. 7. Microphotograph of the hybrid tracking low-pass filter.
Design and Implementation of Low-Power ANSI S1.11 Filter Bank for Digital Hearing Aids

Yu-Ting Kuo, Tay-Jyi Lin, Member, IEEE, Yueh-Tai Li, and Chih-Wei Liu

Diagram of the advanced hearing aid.
Fig. 14. Magnitude response of the proposed 18-band 1/3-octave filter bank.
This paper addresses the low-power filter bank design for advanced digital hearing aids. In the literature, the standard ANSI S1.11 1/3-octave filter bank is rarely adopted in hearing aids due to high computation complexity even though it has the advantage of well matching the human hearing characteristics. We develop an efficient multirate filter bank algorithm to implement an 18-band ANSI S1.11 1/3-octave FIR filter bank. The proposed architecture needs only 4% of multiplications and additions of a straightforward parallel FIR filter bank design. We also investigate and apply several lower-power

The test chip consumes only $87 \mu W$, 
Most existing ANSI S1.11 filter banks are implemented by infinite-impulse response (IIR) filters [8], [9]. Indeed, the researches in psychoacoustics had shown that human ear is not sensitive to phase-distortion. The filter bank with IIR filters may be a good design with low computation complexity; however, FIR filters are still preferred and adopted in [3]–[7], not only for their linear phase but also for the stability and regular structure. The round-off error of FIR filters is easier to analyze and
Simple quadrature oscillator for BIST

J. Raman, P. Rombouts and L. Weyten

ELECTRONICS LETTERS  18th February 2010  Vol. 46  No. 4

Two integrator loop oscillators – different methods for controlling the loss
A 0.6-V Zero-IF/Low-IF Receiver With Integrated Fractional-N Synthesizer for 2.4-GHz ISM-Band Applications

Ajay Balankutty, Student Member, IEEE, Shih-An Yu, Student Member, IEEE, Yiping Feng, Student Member, IEEE, and Peter R. Kinget, Senior Member, IEEE
filter is only 2. To reduce the number of OTAs required for implementing the filter, a lower-order filter transfer function would be preferred. However, biquad-based filters have the drawback that the filter characteristics are more easily affected by parasitics and OTA non-idealities and this sensitivity of the filter characteristics typically is a function of the Q of the filter poles [24]. To make the biquad more tolerant to parasitics and OTA non-idealities, a Tow–Thomas implementation for the biquad is used [25]. To further reduce the sensitivity to parasitics, low Q biquads are preferred. The 6th-order Butterworth filter is chosen for the channel select filter and is implemented as a cascade of three biquads with pole Qs of 0.515, 0.707 and 1.93. The ordering of the biquads has a significant impact on the baseband performance and is discussed in the next section. Even though
Fig. 5. Simulated frequency response for the different complex biquad stages. The ordering of the biquads is determined by their blocker attenuation. For maximal out-of-channel attenuation as early as possible, the biquads are ordered such that the biquad with $Q = 0.517$ is followed by the biquad with $Q = 0.707$ and biquad with $Q = 1.93$. 
Analogue wavelet transform with single biquad stage per scale

M.A. Gurrola-Navarro and G. Espinosa-Flores-Verdad

ELECTRONICS LETTERS 29th April 2010 Vol. 46 No. 9
The OTAs are biased in the subthreshold region.
Design of a K-Band Chip Filter With Three Tunable Transmission Zeros Using a Standard 0.13-\(\mu\)m CMOS Technology

Chin-Lung Yang, Shin-Yi Shu, and Yi-Chyun Chiang, Member, IEEE

is presented for 24-GHz automotive ultrawideband (UWB) radar systems. The filter combines a second-order asymmetrically compact resonator filter with a source–load coupling mechanism to realize three transmission zeros; two zeros are arranged in the lower stopband, and one zero is located in the upper stopband. To achieve a compact layout size and a low insertion loss, a semi-lumped approach, which is accomplished with mixed utilization of high-impedance coplanar waveguide lines and lumped capacitors, is used to construct the chip filter. A K-band experimental proto-
Power-Efficient and Cost-Effective 2-D Symmetry Filter Architectures

Pei-Yu Chen, Student Member, IEEE, Lan-Da Van, Member, IEEE, I-Hung Khoo, Member, IEEE, Hari C. Reddy, Fellow, IEEE, and Chin-Teng Lin, Fellow, IEEE

Abstract—This paper presents two-dimensional (2-D) VLSI digital filter structures possessing various symmetries in the filter magnitude response. For this purpose, four Type-1 and four Type-2 power-efficient and cost-effective 2-D magnitude sym-
Fig. 11. Proposed multimode 2-D filter architecture with four symmetries for $N = 3$. 
area size of $718.95 \, \mu m \times 711.05 \, \mu m$. The corresponding power consumption of the proposed multimode 2-D filter is 29.34 mW on average. In terms of power comparison, the DSM, FRSM,

Fig. 18. Layout of the proposed multimode symmetry filter for $N = 3$. 
A Subharmonic Receiver in SiGe Technology for 122 GHz Sensor Applications

Klaus Schmalz, Wolfgang Winkler, Johannes Borngräber, Wojciech Debski, Bernd Heinemann, and J. Christoph Scheytt, Member, IEEE

Fig. 1. Topology of the subharmonic receiver.

is fabricated in SiGe:C BiCMOS technology with $f_T/f_{\text{max}}$ of 255 GHz/315 GHz. The receiver was optimized by an
Fig. 4. Schematic of 5 GHz polyphase filter

\[ R = 67 \, \Omega \] and \[ C = 40 \, \text{fF} \]

1 unsalicided, p-doped gate polysilicon as resistor

MIM capacitors with 1 fF/\mu m^2.
Low-Power and Widely Tunable Linearized Biquadratic Low-Pass Transconductor-C Filter

Armin Tajalli, Member, IEEE, and Yusuf Leblebici, Fellow, IEEE

Abstract—A sixth-order low-pass transconductor-C filter with a very wide tuning range ($f_c = 100$ Hz to 10 MHz) is presented. The wide tuning range has been achieved without using switchable components or programmable building blocks.

In 0.18-$\mu$m CMOS technology

the input devices are biased in the subthreshold regime
Fig. 2. Biquadratic $g_m$-C filter. (a) Conventional topology. (b) Modified topology with improved linearity performance.
Fig. 4. Schematic of the folded cascode transconductor used to implement the widely tunable filter.
CMOS on-chip active RF tracking filter for digital TV tuner ICs

Y. Sun, C.J. Jeong, S.K. Han and S.G. Lee

ELECTRONICS LETTERS 17th March 2011 Vol. 47 No. 6

The fabricated tracking filter based on a 0.13 μm CMOS process shows 48–780 MHz tracking range with 15–60 MHz bandwidth, 50 dB attenuation and a tuning time of 14 Ts.
Fig. 1 Proposed RF tracking filter design

a Schematic of unit $G_m$-cell used in proposed RF tracking filter
b RF tracking filter architecture
c Biquad architecture
d $G_M$-cell in biquad
Fig. 2 *Measured frequency tuning and rejection performance*
Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification

Amir Ghaffari, Student Member, IEEE, Eric A. M. Klumperink, Senior Member, IEEE, Michiel C. M. Soer, Student Member, IEEE, and Bram Nauta, Fellow, IEEE

Fig. 1. Architecture of an N-path filter [5] (p and q are the mixing functions and T is the period of the mixing frequency).
Fig. 2. (a) Switched-RC N-path filter. (b) Single port, single ended N-path filter. (c) Multiphase clocking. (d) Typical (in-band) input and output signal.
<table>
<thead>
<tr>
<th>Performance</th>
<th>This Work</th>
<th>[9]</th>
<th>[4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>65nm CMOS</td>
<td>0.35um CMOS</td>
<td>0.18um CMOS</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.07mm²</td>
<td>1.9mm²</td>
<td>0.81mm²</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>2 to 16mW</td>
<td>63mW</td>
<td>17mW</td>
</tr>
<tr>
<td>Frequency Tuning Range</td>
<td>0.1 to 1GHz</td>
<td>240 to 530MHz</td>
<td>2 to 2.06GHz</td>
</tr>
<tr>
<td>-3dB Band Width</td>
<td>35MHz</td>
<td>1.75 to 4.6MHz</td>
<td>130MHz</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>-2dB</td>
<td>-2dB</td>
<td>0dB</td>
</tr>
<tr>
<td>Quality Factor (Q)</td>
<td>3 to 29</td>
<td>301 to 114</td>
<td>15.4 to 15.8</td>
</tr>
<tr>
<td>$P_{1dB}$</td>
<td>2dBm</td>
<td>-5dBm</td>
<td>-6.6dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>14dBm</td>
<td>NA</td>
<td>2.5dBm</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>3-5dB</td>
<td>9dB</td>
<td>15dB</td>
</tr>
</tbody>
</table>
A 400 $\mu$W Hz-Range Lock-In A/D Frontend Channel for Infrared Spectroscopic Gas Recognition

Stepan Sutula, Student Member, IEEE, Carles Ferrer, and Francisco Serra-Graells, Member, IEEE
Fig. 3. Proposed sub-Hz programmable MOS-C high-pass preamplifier.
Fig. 6. (a) Proposed linear transconductor and (b) equivalent built-in limiter
9. Experimental transfer function of the high-pass preamplifier stage for pendent gain (top) and corner frequency (bottom) digital programming.
An Electronically Fine-Tunable Multi-Input–Single-Output Universal Filter

Indrit Myderrizi, Member, IEEE, Shahram Minaei, Senior Member, IEEE, and Erkan Yuce, Member, IEEE

Fig. 1. CMOS realization of the proposed VM MISO universal filter.
Fig. 3. Magnitude frequency responses of the MISO multifunctional filter.

For a high-$Q$ BP response of the filter. In this case, $Q = 5$, and the component values are selected as $C_1 = 0.457$ pF, $C_2 = 2$ pF, $R_1 = 6.5$ k$\Omega$, and $R_2 = 37.2$ k$\Omega$. 
A 16-Channel Low-Noise Programmable System for the Recording of Neural Signals

Carolina Mora López, Dries Braeken, Carmen Bartic, Robert Puers*, Georges Gielen* and Wolfgang Eberle
Imec, Leuven, Belgium

Figure 1. Architecture of the 16-channel neural recording system.
The high-pass filtering characteristic in each channel is achieved by the parallel combination of the feedback capacitors and the feedback MOS-bipolar pseudoresistors (formed by a NMOS and a PMOS transistors). These voltage-controlled pseudoresistor elements [7] can achieve very high resistance values in the order of $10^{12} \ \Omega$, providing an area-efficient way to implement very low frequency filters. The cutoff frequency can be tuned via a current-mode digital-to-analog converter (Fig. 3) that changes the gate voltages of the transistors (i.e. the resistance), in order to accept or reject the LFP signal frequencies. This circuit consists of a wide-swing cascode current mirror that copies the selected current to the transistors $Mn$ and $Mp$, which are diode-connected and sized with large $W/L$. A similar method was previously described by Yin et al [8].
The fourth-order low-pass filter characteristic is implemented by the cascade of first-order voltage integrators, consisting of an OTA and a load capacitor. The load capacitor is implemented as a capacitor array that allows the selection of two different frequency ranges: one for the LFP signals and another for the AP signals. Also, for low-frequency LFP recordings, the supply current of the amplifiers is lowered to save power.
Figure 5. Transfer function of one channel, measured for different bandwidths and gains.
Figure 4. Die photo of the 16-channel neural recording system. The total area is $5.6 \text{ mm} \times 4.5 \text{ mm}$ and the core area is $4.1 \text{ mm} \times 3.8 \text{ mm}$.

The 16-channel neural recording system in Fig.1 has been implemented and fabricated in a 0.35 $\mu$m On Semiconductor CMOS technology. The capacitors are implemented as metal-insulator-metal capacitors and the resistors as polysilicon resistors. The die (Fig. 4) occupies a core area of $4.1 \times 3.8 \text{ mm}^2$ and a total area of $5.6 \times 4.5 \text{ mm}^2$. The area of one channel is $0.76 \text{ mm}^2$. 
A High-Performance PLL With a Low-Power Active Switched-Capacitor Loop Filter

Yu Song, Student Member, IEEE, and Zeljko Ignjatovic, Member, IEEE

Fig. 1. Proposed SC PLL loop filter with complimentary charge pumps, single-ended shown.
A low-power low-noise differential SC loop filter is designed based on the above analysis, with another filter, as shown in Fig. 1, sharing the complimentary charge pumps. The input reference frequency is selected to be 10 MHz, and the loop bandwidth is around 350 kHz. The discrepancy between the
<table>
<thead>
<tr>
<th></th>
<th>[1]</th>
<th>[3]</th>
<th>[4]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq. (GHz)</td>
<td>2.4</td>
<td>2.4</td>
<td>3.6</td>
<td>2.5</td>
</tr>
<tr>
<td>Technology CMOS</td>
<td>0.25µm</td>
<td>0.18µm</td>
<td>0.18µm</td>
<td>0.18µm</td>
</tr>
<tr>
<td>Loop Filter Structure</td>
<td>Passive SC</td>
<td>Passive SC</td>
<td>Hybrid</td>
<td>Active SC</td>
</tr>
<tr>
<td>Reference Frequency</td>
<td>1MHz</td>
<td>12MHz</td>
<td>50MHz</td>
<td>10MHz</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>?</td>
<td>48.8 (core)</td>
<td>110 (core)</td>
<td>16</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>?</td>
<td>4.8</td>
<td>2.7 (active)</td>
<td>0.36</td>
</tr>
<tr>
<td>Reference Spur</td>
<td>-62dBc</td>
<td>-70dBc</td>
<td>-45dBc</td>
<td>-64dBc</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-126dBc/Hz @2MHz</td>
<td>-125dBc/Hz @3MHz</td>
<td>-155dBc/Hz @20MHz</td>
<td>-124dBc/Hz @3MHz</td>
</tr>
</tbody>
</table>
Power-Scalable, Complex Bandpass/Low-Pass Filter With I/Q Imbalance Calibration for a Multimode GNSS Receiver

Yang Xu, Baoyong Chi, Member, IEEE, Xiaobao Yu, Nan Qi, Patrick Chiang, Member, IEEE, and Zhihua Wang, Senior Member, IEEE

Fig. 1. Low-IF/zero-IF multimode GNSS receiver.
Fig. 2. Architecture of the reconfigurable fifth-order CBPF/third-order LPF.
Fig. 3. Simplified op-amp cell of the FLOA.
Fig. 7. Measured ac response of the LPF and the CBPF.
Basic Filter Components

• All Pass Networks
• Arbitrary Transfer Function Synthesis
• Impedance Transformation Circuits
• Equalizers
All-Pass Circuits

- Magnitude of Gain is Constant
- Phase Changes with Frequency
- Used to correct undesired phase characteristics of a filter
First-Order All Pass

\[ T(s) = \frac{s - \frac{1}{RC}}{s + \frac{1}{RC}} \]
First-Order All Pass

\[ T(s) = \frac{s - \frac{1}{RC}}{s + \frac{1}{RC}} \]

\[ T(j\omega) = \frac{1}{RC} \]

\[ \angle T(j\omega) \]

\[ \omega \]

\[ \text{s-plane} \]

\[ \text{Im} \]

\[ \text{Re} \]
First-Order All Pass

\[ T(s) = -\frac{s - \frac{1}{RC}}{s + \frac{1}{RC}} \]
First-Order All Pass

\[ T(s) = -\frac{s - \frac{1}{RC}}{s + \frac{1}{RC}} \]

\[ T(j\omega) \]

\[ \angle T(j\omega) \]
Second-Order All Pass

Based upon Bridged-T Feedback Structure

\[
\frac{V_O}{V_{IN}} = \frac{s^2 - s \left( \frac{2}{R2C} \right) + \frac{1}{R1R2C^2}}{s^2 + s \left( \frac{2}{R2C} \right) + \frac{1}{R1R2C^2}}
\]
Second-Order All Pass

\[
\frac{V_O}{V_{IN}} = \frac{s^2 - s \left( \frac{2}{R_2 C} \right) + \frac{1}{R_1 R_2 C^2}}{s^2 + s \left( \frac{2}{R_2 C} \right) + \frac{1}{R_1 R_2 C^2}}
\]
Basic Filter Components

- All Pass Networks
- Arbitrary Transfer Function Synthesis
- Impedance Transformation Circuits
- Equalizers
Arbitrary Transfer Function Synthesis

• Based upon coefficient derivation
• Can be used to implement/solve an arbitrary differential equation
• Versatile
• Basic concept of Analog Computer
Applications of integrators to solving differential equations

Standard Integral form of a differential equation

\[ X_{OUT} = b_1 \int X_{OUT} + b_2 \int \int X_{OUT} + b_3 \int \int \int X_{OUT} + \ldots + a_0 X_{IN} + \int X_{IN} + \int \int X_{IN} + \ldots \]

Standard differential form of a differential equation

\[ X_{OUT} = \alpha_1 X'_{OUT} + \alpha_2 X''_{OUT} + \alpha_3 X'''_{OUT} + \ldots + \beta_1 X_{IN} + \beta_2 X'_{IN} + \beta_3 X''_{IN} + \ldots \]

Initial conditions not shown

Can express any system in either differential or integral form
Applications of integrators to solving differential equations

Consider the standard integral form

\[ X_{OUT} = b_1 \int X_{OUT} + b_2 \int \int X_{OUT} + b_3 \int \int \int X_{OUT} + \ldots + a_0 X_{IN} + \int X_{IN} + \int \int X_{IN} + \ldots \]

This circuit is comprised of summers and integrators

One Implementation (direct and intuitive)

This circuit can solve an arbitrary linear differential equation

This concept was used in Analog Computers in the past
Applications of integrators to solving differential equations

Consider the standard integral form

\[ X_{OUT} = b_1 \int X_{OUT} + b_2 \int \int X_{OUT} + b_3 \int \int \int X_{OUT} + \ldots + a_0 X_{IN} + \int X_{IN} + \int \int X_{IN} + \ldots \]

Take the Laplace transform of this equation

\[ \mathcal{X}_{OUT} = b_1 \frac{1}{s} \mathcal{X}_{OUT} + b_2 \frac{1}{s^2} \mathcal{X}_{OUT} + b_3 \frac{1}{s^3} \mathcal{X}_{OUT} + \ldots + b_n \frac{1}{s^n} + a_0 \mathcal{X}_{IN} + a_1 \frac{1}{s} \mathcal{X}_{IN} + a_2 \frac{1}{s^2} \mathcal{X}_{IN} + a_3 \frac{1}{s^3} \mathcal{X}_{IN} + \ldots + a_m \frac{1}{s^m} \]

Multiply by \( s^n \) and assume \( m=n \) (some of the coefficients can be 0)

\[ s^n \mathcal{X}_{OUT} = b_1 s^{n-1} \mathcal{X}_{OUT} + b_2 s^{n-2} \mathcal{X}_{OUT} + b_3 s^{n-3} \mathcal{X}_{OUT} + \ldots + b_n s^n \mathcal{X}_{IN} + a_1 s^{n-1} \mathcal{X}_{IN} + a_2 s^{n-2} \mathcal{X}_{IN} + a_3 s^{n-3} \mathcal{X}_{IN} + \ldots + a_n \]

\[ \mathcal{X}_{OUT} (s^n - b_1 s^{n-1} - b_2 s^{n-2} - b_3 s^{n-3} - \ldots - b_n) = \mathcal{X}_{IN} (a_0 s^n + a_1 s^{n-1} + a_2 s^{n-2} + a_3 s^{n-3} + \ldots + a_n) \]

\[ T(s) = \frac{\mathcal{X}_{OUT}}{\mathcal{X}_{IN}} = \frac{a_0 s^n + a_1 s^{n-1} + a_2 s^{n-2} + a_3 s^{n-3} + \ldots + a_n}{s^n - b_1 s^{n-1} - b_2 s^{n-2} - b_3 s^{n-3} - \ldots - b_n} \]
Applications of integrators to solving differential equations

Consider the standard integral form

\[ X_{OUT} = b_1 \int X_{OUT} + b_2 \int \int X_{OUT} + b_3 \int \int \int X_{OUT} + \ldots + a_0 X_{IN} + \int X_{IN} + \int \int X_{IN} + \ldots \]

\[ T(s) = \frac{X_{OUT}}{X_{IN}} = \frac{a_0 s^n + a_1 s^{n-1} + a_2 s^{n-2} + a_3 s^{n-3} + \ldots + a_n}{s^n - b_1 s^{n-1} - b_2 s^{n-2} - b_3 s^{n-3} - \ldots - b_n} \]

This can be written in more standard form

\[ T(s) = \frac{\alpha_n s^n + \alpha_{n-1} s^{n-1} + \ldots \alpha_1 s + \alpha_0}{s^n + \beta_{n-1} s^{n-1} + \ldots + \beta_1 s + \beta_0} \]
Applications of integrators to filter design

\[ T(s) = \frac{\alpha_n s^n + \alpha_{n-1} s^{n-1} + \ldots + \alpha_1 s + \alpha_0}{s^n + \beta_{n-1} s^{n-1} + \ldots + \beta_1 s + \beta_0} \]

Can design (synthesize) any \( T(s) \) with just integrators and summers!

Integrators are not used “open loop” so loss is not added

Although this approach to filter design works, often more practical methods are used.
Applications of integrators to filter design

$$T(s) = \frac{\alpha_n s^n + \alpha_{m-1} s^{n-1} + \ldots + \alpha_1 s + \alpha_0}{s^n + \beta_{n-1} s^{n-1} + \ldots + \beta_1 s + \beta_0}$$

What are some other architectural implementations?

**Cascaded Biquads**

**Leapfrog**

Though these other implementations may have better performance, not as easily programmable to realize different functions.
Basic Filter Components

• All Pass Networks
• Arbitrary Transfer Function Synthesis
• Impedance Transformation Circuits
• Equalizers
Impedance Synthesis

• Focus on synthesizing impedance rather than transfer function
• Gyrators will provide inductance simulation
• Capacitance Multiplication
• Synthesis of super components
Impedance Converters

Note these circuits are strictly one-ports and have no output node.
Impedance Converters

\[ V_1(G_1 + G_2) = V_x G_2 \]
\[ I_1 = (V_1 - V_x) G_3 \]

\[ Z_{IN} = -\frac{Z_1 Z_3}{Z_2} \]

Observe this input impedance is negative!
Impedance Converters

\[ Z_{IN} = - \frac{Z_1 Z_3}{Z_2} \]

If \( Z_1 = R_1 \), \( Z_2 = R_2 \) and \( Z_3 = R_3 \),
\[ Z_{IN} = - \frac{R_1 R_3}{R_2} \]
This is a negative resistor!

If \( Z_2 = 1/sC \), \( Z_1 = R_1 \) and \( Z_3 = R_3 \),
\[ Z_{IN} = -sCR_1 R_3 \]
This is a negative inductor!

If \( Z_2 = R_2 \), \( Z_1 = 1/sC \) and \( Z_3 = R_3 \),
\[ Z_{IN} = - \frac{R_3}{sCR_2} \]
This is a negative capacitor!

This is termed a Negative Impedance Converter.
Impedance Converters

If $Z_2 = 1/sC$, $Z_1 = R_1$ and $Z_3 = R_3$, then

$$Z_{IN} = -\frac{Z_1 Z_3}{Z_2}$$

Modification of NIC to provide a positive inductance:

Replace $Z_1$ itself with a second NIC that has a negative input impedance.
Negative Impedance Converter

One application of NIC

If select components so that \( R_S = \frac{R_2}{R_1 R_3} \)
Impedance Converters

This circuit is often called a Gyrator

\[ Z_{IN} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \]
Gyrator Analysis

\[ I_X = V_1 G_3 \]
\[ V_X = V_1 + \frac{V_1 G_3}{G_4} = V_1 \left( 1 + \frac{G_3}{G_4} \right) \]
\[ I_Y = (V_1 - V_X) G_1 = V_1 \left( -\frac{G_3}{G_4} \right) G_1 \]
\[ V_Y = V_1 + \frac{I_Y}{G_2} = V_1 \left( 1 - \frac{G_3 G_1}{G_4 G_2} \right) \]
\[ I_1 = (V_1 - V_Y) G_5 = V_1 \left( \frac{G_3}{G_4} \left( \frac{G_1}{G_2} \right) \right) G_5 \]
\[ Z_{IN} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \]
Gyrator Applications

\[ Z_{IN} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \]

If \( Z_1 = Z_3 = Z_4 = Z_5 = R \) and \( Z_2 = 1/sC \)

\[ Z_{IN} = (R^2C)s \]

This is an inductor of value \( L = R^2C \)

If \( Z_2 = R_2, Z_3 = R_3, Z_4 = R_4, Z_5 = R_5 \) and \( Z_1 = 1/sC \)

\[ Z_{IN} = \frac{R_3 R_5}{sCR_2 R_4} \]

This is a capacitor of value \( C_{EQ} = C \frac{R_2 R_4}{R_3 R_5} \) (can scale capacitance up or down)

If \( Z_2 = Z_4 = Z_5 = R \) and \( Z_1 = Z_3 = 1/sC \)

\[ Z_{IN} = (R^3C^2)s^2 \]

This is a “super” capacitor of value \( R^3C^2 \)
Impedance Converters

If $Z_3 = R_3$, $Z_2 = R_2$ and $Z_1 = 1/sC$

$$Z_{IN} = R_3 + s\left(CR_2R_3\right)$$

$$I_1 = \left(V_1 - \left(\frac{Z_1}{Z_1 + Z_2}\right)V_1\right)G_3$$

$$Z_{IN} = Z_3\left(1 + \frac{Z_2}{Z_1}\right)$$

$$L_{EQ} = CR_2R_3$$
Basic Filter Components

• All Pass Networks
• Arbitrary Transfer Function Synthesis
• Impedance Transformation Circuits
• Equalizers
Shelving Equalizers

- Widely used in audio applications
- User-programmable filter response
Shelving Equalizers

(A) High frequency.
Shelving Equalizers

Fig. 6-37. Shelving equalizers.
Shelving Equalizers

- The expressions for $f_L$ and $f_H$ for the previous two circuits show a small movement with the potentiometer position in contrast to the fixed point location depicted in this figure.

- The OTA-C filters discussed earlier in the course can be designed to have fixed values for $f_L$ and $f_H$ when cut or boost is used.
End of Lecture 39_2